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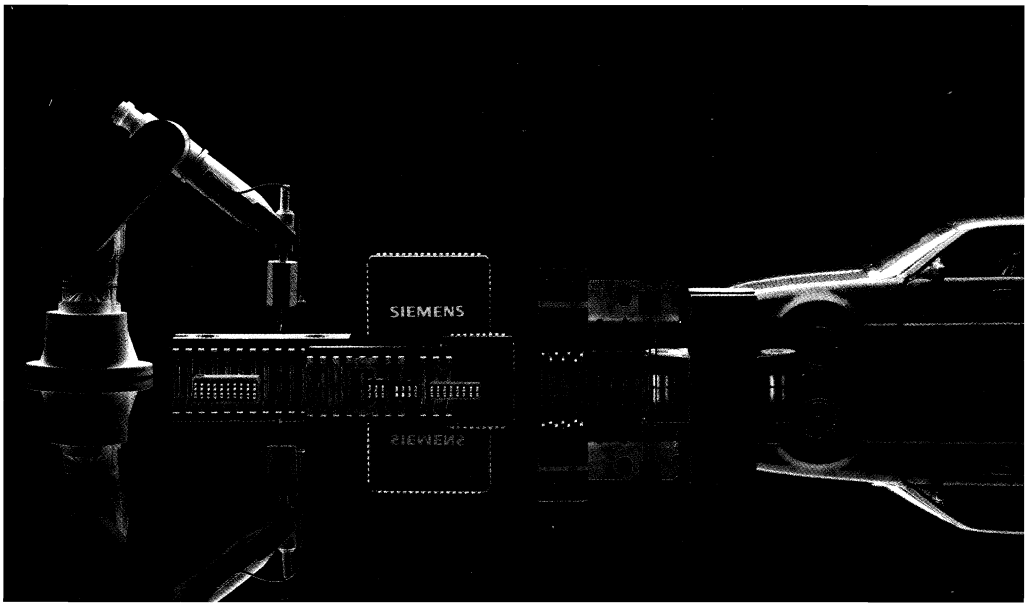

Industrial and Automotive ICs

IC für Industrie- und Autoelektronik

Data Book

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S FZL 4145 D	Q67000-H8437	Quad Driver incl. Short-Circuit Signalling	289
S HKZ 101	Q67000-A9002-A401	Hall-Effect Vane Switch	792
S ■ SAB 0529	Q67000-H2176	Programmable Digital Timer	485
S ■ SAB 0529 G	Q67000-H2952	Programmable Digital Timer	485
S SAB 0600	Q67000-H1948	Three-Tone Chime	525
■ SAB 0601	Q67000-H2312	Single-Tone Chime	525
■ SAB 0602	Q67000-H2313	Dual-Tone Chime	525
S SAE 0530	Q67000-H8403	Programmable Timer, 50 Hz	501
S SAE 0531	Q67000-H8431	Programmable Timer, 60 Hz	501
S SAE 0532 G	Q67000-H8432	Programmable Timer, 50/60 Hz	501
S SAE 0700	Q67000-A2445	Audible Signal Device	534
S SAE 81C52 G	Q67100-H9015	256 x 8-Bit Static CMOS RAM	833
S SAE 81C52 P	Q67100-H9017	256 x 8-Bit Static CMOS RAM	833
SAE 81C54 P	Q67100-H8486	CMOS RAM	840
S ▼ SAE 81C80 A	Q67100-H8706	Dual-Port RAM	846
S SDA 0808 B	Q67100-A8129	Microprocessor-Compatible 8-Bit Analog/ Digital Converter with 8-Channel Multiplexer	424
SDA 0808 N	Q67100-A8206	Microprocessor-Compatible 8-Bit Analog/ Digital Converter with 8-Channel Multiplexer	424
S SDA 0810 B	Q67100-A8144	Microprocessor-Compatible 10-Bit Analog/ Digital Converter with 8-Channel Multiplexer	437
SDA 0810 N	Q67100-A8207	Microprocessor-Compatible 10-Bit Analog/ Digital Converter with 8-Channel Multiplexer	437
S ▼ SDA 0812 A	Q67100-A8233	Microprocessor-Compatible 12-Bit Analog/ Digital Converter with 4-Channel Multiplexer	452
▼ SDA 0812 AN	Q67100-A8300	Microprocessor-Compatible 12-Bit Analog/ Digital Converter with 4-Channel Multiplexer	452
SDA 1808 N	Q67100-A8254	Microprocessor-Compatible 8-Bit Analog/ Digital Converter with 8-Channel Multiplexer	424
▼ SDA 1810 D	Q67100-H8730	Microprocessor-Compatible 10-Bit Analog/ Digital Converter with 8-Channel Multiplexer	437
SDA 1810 N	Q67100-A8230	Microprocessor-Compatible 10-Bit Analog/ Digital Converter with 8-Channel Multiplexer	437
▼ SDA 1810 DN	Q67100-H8735	Microprocessor-Compatible 10-Bit Analog/ Digital Converter with 8-Channel Multiplexer	437

▼ New type

■ Not for new design

SMD = Surface Mounted Device

1.1 Types in Alphanumerical Order (cont'd)

Types	Ordering Code	Function	Page
▼ SDA 1812 D	Q67100-A8291	Microprocessor-Compatible 12-Bit Analog/ Digital Converter with 4-Channel Multiplexer	452
▼ SDA 1812 DN	Q67100-A8301	Microprocessor-Compatible 12-Bit Analog/ Digital Converter with 4-Channel Multiplexer	452
S SDA 5200 N	Q67000-A2242	6-Bit Analog/Digital Converter, 100 MHz	368
S SDA 5200 S	Q67000-A2243	6-Bit Analog/Digital Converter, 100 MHz	368
S ■ SDA 6020	Q67000-Y584	6-Bit Analog/Digital Converter, 50 MHz	359
S SDA 8010	Q67000-A2566	8-Bit Analog/Digital Converter, 100 MHz	392
SDA 8020 N	Q67000-A8127	DASR Data Acquisition Shift Register for HSDA Systems	405
SDA 8200	Q67000-A8164	6-Bit Analog/Digital Converter, 300 MHz	375
SDE 2506 A2	Q67100-H9018	Nonvolatile Memory 1-Kbit E^2PROM	866
SDE 2526 A2	Q67100-H9020	Nonvolatile Memory with I^2C Bus Interface (8 Kbit)	874
S ▼ SLB 0586 A	Q67000-H8721	Dimmer IC	337
S ▼ SLB 0586 G	Q67000-H8720	Dimmer IC	337
S SLE 4520	Q67100-H8271	Pulse Width Modulator	677
S TAA 762 A	Q67000-A2271	Operational Amplifier	64
TAA 762 G	Q67000-A2273	Operational Amplifier	64
S TAA 765 A	Q67000-A524	Operational Amplifier	64
S TAA 765 G	Q67000-A599-G403	Operational Amplifier	64
S TAA 2762 A	Q67000-A2499	Dual Operational Amplifier	98
S TAA 2765 A	Q67000-A1031	Dual Operational Amplifier	98
S TAA 4762 A	Q67000-A2502	Quad Operational Amplifier	117
S TAA 4765 A	Q67000-A1033	Quad Operational Amplifier	117
S TAE 1453 A	Q67000-A2017	PNP Operational Amplifier	82
S TAE 1453 G	Q67000-A2106	PNP Operational Amplifier	82
S TAE 2453 A	Q67000-A2107	Dual PNP Operational Amplifier	107
S TAE 2453 G	Q67000-A2108	Dual PNP Operational Amplifier	107
S TAE 4453 A	Q67000-A2109	Quad PNP Operational Amplifier	126
S TAE 4453 G	Q67000-A2152	Quad PNP Operational Amplifier	126
S TAF 1453 A	Q67000-A2269	PNP Operational Amplifier	82
TAF 1453 G	Q67000-A2209	PNP Operational Amplifier	82
S TAF 2453 A	Q67000-A2210	Dual PNP Operational Amplifier	107
TAF 2453 G	Q67000-A2211	Dual PNP Operational Amplifier	107
S ■ TAF 4453 A	Q67000-A2212	Quad PNP Operational Amplifier	126
■ TAF 4453 G	Q67000-A2213	Quad PNP Operational Amplifier	126
▼ TAF 4463 A	Q67000-A8308	Quad PNP Operational Amplifier with Low Offset Drift	131

▼ New type
■ Not for new design
SMD = Surface Mounted Device

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▼ TAF 4463 G	Q67000-A8306	Quad PNP Operational Amplifier with Low Offset Drift	131
S TBA 221 B	Q67000-A281	Operational Amplifier	89
S TBA 222 B	Q67000-A2280	Operational Amplifier	89
TBA 222 BS1	Q67000-A8057	Operational Amplifier	89
▼ TBB 278 A	Q67100-H8705	Video Pulse Generator	882
S ■ TBB 741 G	Q67000-A1498	Operational Amplifier	89
S ■ TBB 742 G	Q67000-A2395-G403	Operational Amplifier	89
S ■ TBB 1458 B	Q67000-A1036	Dual Operational Amplifier	112
S ■ TBB 1458 G	Q67000-A1458	Dual Operational Amplifier	112
S TBC 2332 B	Q67000-A2500	Dual Operational Amplifier with Darlington Input	102
S TBC 4332 A	Q67000-A2503	Quad Operational Amplifier with Darlington Input	121
S TBE 2335 B	Q67000-A1165	Dual Operational Amplifier with Darlington Input	102
S TBE 4335 A	Q67000-A1167	Quad Operational Amplifier with Darlington Input	121
S TCA 105	Q67000-A527	Threshold Switch	137
S TCA 105 B	Q67000-A587	Threshold Switch	137
S TCA 105 G	Q67000-A988	Threshold Switch	137
S ■ TCA 205 A	Q67000-A1034	Proximity Switch	798
S TCA 305 A	Q67000-A2291	Proximity Switch	805
S TCA 305 G	Q67000-A2305	Proximity Switch	805
S TCA 312 A	Q67000-A2048	Comparator with Darlington Input, TTL-Compatible	161
TCA 312 G	Q67000-A2509	Comparator with Darlington Input, TTL-Compatible	161
S TCA 315 A	Q67000-A561	Comparator with Darlington Input, TTL-Compatible	161
S TCA 315 G	Q67000-A1005	Comparator with Darlington Input, TTL-Compatible	161
S ■ TCA 322 A	Q67000-A2501	Comparator, TTL-Compatible	162
■ TCA 322 G	Q67000-A2508	Comparator, TTL-Compatible	162
S ■ TCA 325 A	Q67000-A562	Comparator, TTL-Compatible	162
S ■ TCA 325 G	Q67000-A1012	Comparator, TTL-Compatible	162
S ■ TCA 332 A	Q67000-A2272	Operational Amplifier with Darlington Input	75
■ TCA 332 G	Q67000-A2270	Operational Amplifier with Darlington Input	75
S ■ TCA 335 A	Q67000-A563	Operational Amplifier with Darlington Input	75
S ■ TCA 335 G	Q67000-A1018-G403	Operational Amplifier with Darlington Input	75
S ■ TCA 345 A	Q67000-A564	Threshold Switch	143
S TCA 355 B	Q67000-A2443	Proximity Switch	805
S TCA 355 G	Q67000-A2444	Proximity Switch	805
S TCA 365 B	Q67000-A8189	Power Operational Amplifier	543
S ▼ TCA 505 A	Q67000-A8278	IC for Proximity Switch with Short-Circuit Protection	812

▼ New type
■ Not for new design
SMD = Surface Mounted Device

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Type	Ordering Code	Function	Page
S ▼ TCA 505 G	Q67000-A8279	IC for Proximity Switch with Short-Circuit Protection	812
S TCA 671	Q67000-T1	Transistor Array with 5 NPN Transistors	297
S TCA 671 G	Q67000-A2366	Transistor Array with 5 NPN Transistors	297
S TCA 785	Q67000-A2321	Phase Control	305
S TCA 871	Q67000-T2	Transistor Array with 5 NPN Transistors	297
S TCA 871 G	Q67000-A2367	Transistor Array with 5 NPN Transistors	297
S ■ TCA 955	Q67000-A983	Speed Controller	688
S ▼ TCA 965 A	Q67000-A8227	Window Discriminator	147
S ▼ TCA 965 G	Q67000-A2368	Window Discriminator	147
S TCA 971	Q67000-T11	Transistor Array with 5 NPN Transistors	297
S TCA 971 G	Q67000-A8075	Transistor Array with 5 NPN Transistors	297
S TCA 991	Q67000-T12	Transistor Array with 5 NPN Transistors	297
S TCA 991 G	Q67000-A8076	Transistor Array with 5 NPN Transistors	297
S TCA 1365 B	Q67000-A8190	Power Operational Amplifier	553
S TCA 1560 B	Q67000-A8208	Stepper Motor Driver	641
S ▼ TCA 1560 G	Q67000-A8272	Stepper Motor Driver	641
S TCA 1561 B	Q67000-A8209	Stepper Motor Driver	641
S TCA 2365	Q67000-A1876	Dual Power Operational Amplifier	563
S TCA 2365 A	Q67000-A8017	Dual Power Operational Amplifier	563
S TCA 2465	Q67000-A8109	Dual Power Operational Amplifier	573
S TCA 2465 A	Q67000-A8110	Dual Power Operational Amplifier	573
▼ TCA 2465 G	Q67000-A8334	Dual Power Operational Amplifier	573
▼ TCA 3727	Q67000-A8302	Dual Stepper Motor Driver	660
▼ TCA 3727 G	on request	Dual Stepper Motor Driver	660
TDA 4700	Q67000-Y595	Control IC for Single-Ended and Push Pull Switched-Mode Power Supplies (SMPS)	188
S TDA 4700 A	Q67000-Y594	Control IC for Single-Ended and Push Pull Switched-Mode Power Supplies (SMPS)	188
TDA 4714 C	Q67000-A8312	IC for Switched-Mode Power Supplies (SMPS)	203
TDA 4716 C	Q67000-A8313	IC for Switched-Mode Power Supplies (SMPS)	203
S TDA 4718	Q67000-Y638	Control IC for Single-Ended and Push Pull Switched-Mode Power Supplies (SMPS)	188
S TDA 4718 A	Q67000-Y639	Control IC for Single-Ended and Push Pull Switched-Mode Power Supplies (SMPS)	188
S TDA 4814 A	Q67000-A8163	IC for Sinusoidal Line-Current Consumption	216

▼ New type
■ Not for new design
SMD = Surface Mounted Device

1.1 Types in Alphanumerical Order (cont'd)

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▼ TDA 4816 G	Q67000-A8290	IC for Sinusoidal Line-Current Consumption	216
▼ TDA 4817	Q67000-A8298	IC for Sinusoidal Line-Current Consumption	229
▼ TDA 4817 G	Q67000-A8299	IC for Sinusoidal Line-Current Consumption	229
S TDA 4918 A	Q67000-A8021	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
S TDA 4918 G	Q67000-A8142	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
S TDA 4919 A	Q67000-A8143	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
S TDA 4919 G	Q67000-A8018	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
S TLE 3101	Q67000-A2337	Phase Control	320
S ■ TLE 3102	Q67000-A2338	Phase Control	320
S ■ TLE 3103	Q67000-A2339	Phase Control	320
S TLE 3104	Q67000-A2312	Phase Control	320
S TLE 4201 A1	Q67000-A8080	DC Motor Driver	590
S TLE 4201 S1	Q67000-A2285	DC Motor Driver	590
S ■ TLE 4202	Q67000-A8007	2 A DC Motor Driver	599
S TLE 4202 B	Q67000-A8225	2 A DC Motor Driver	608
S TLE 4203	Q67000-A8121	4 A DC Motor Driver	617
S TLE 4204	Q67000-A8182	3 A DC Motor Driver	625
▼ TLE 4205	Q67000-A9025	1 A DC Motor Driver	633
S TLE 4211	Q67000-A8118	Intelligent Double Low-Side Driver 2 x 2 A	695
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▼ TLE 4215	Q67000-A8184	Intelligent Double High-Side Driver 2 x 0.5 A	716
▼ TLE 4216	Q67000-A8237	Intelligent 6 Times Low-Side Driver	726
▼ TLE 4220	Q67000-A9010	Intelligent 4 A Low-Side Driver	737
S TLE 4258	Q67000-A8238	5-V Low Drop Voltage Regulator	255
S TLE 4260	Q67000-A8187	5-V Low Drop Voltage Regulator	265
S ▼ TLE 4261	Q67000-A9003	5-V Low Drop Voltage Regulator	275
S TLE 4901 F	Q67000-A2518	Integrated Hall-Effect Switch for Alternating Magnetic Field	752
S TLE 4902 F	Q67000-A8048	Integrated Hall-Effect Switch for Alternating Magnetic Field	758
*) ▼ TLE 4303 F	Q67000-A9032	Intelligent Relay Driver	—
*) ▼ TLE 4304	Q67000-A9030	Intelligent Relay Driver with Logic-Level Input	—

*) Ordering No. of Data Sheet: B112-B6303-X-X-7600

▼ New type

■ Not for new design

SMD = Surface Mounted Device

1.1 Types in Alphanumerical Order (cont'd)

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S TLE 4903 F	Q67000-A8047	Integrated Hall-Effect Switch for Unipolar Magnetic Field	763
TLE 4910 G	Q67000-A9009	Hall-Effect IC with Analog Output	768
▼ TLE 4920 F	Q67000-A9023	Gear Wheel Sensor IC	779
S ▼ TLE 4920 G	Q67000-A9000	Gear Wheel Sensor IC	779
S ■ TLE 4951	Q67000-A8266	Current-Monitoring IC	176
S ■ TLE 4951 G	Q67000-A8267	Current-Monitoring IC	176

▼ New type
■ Not for new design
SMD = Surface Mounted Device

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Operational Amplifiers

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TDA 4816 G	IC for Sinusoidal Line-Current Consumption	216
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TDA 4918 A; G	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
TDA 4919 A; G	IC for Switched-Mode Power Supplies with SIPMOS Driver Output	236
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*) Ordering no. of the relay driver data sheet: B112-B6303-X-X-7600

1. Typenbezeichnungssystem für integrierte Schaltungen

Für die Typenbezeichnungen der ICs wird das europäische System nach Pro Electron verwendet. Der Bezeichnungsschlüssel ist in der Pro Electron-Broschüre D15*) Ausgabe 1988 erläutert.

*) Bezugsadresse: Pro Electron
Rue d'Arlon, 69-71
B-1040 Bruxelles, Belgique

2. Einbauhinweise

Kunststoff-Gehäuse

Die Anschlüsse der Gehäuse sind um 90° nach unten abgebogen und passen in ein Lochraster von 2,54 mm, Lochkreisdurchmesser 9,7 bis 0,9 mm. Das Maß X ist der entsprechenden Gehäusebezeichnung zu entnehmen.

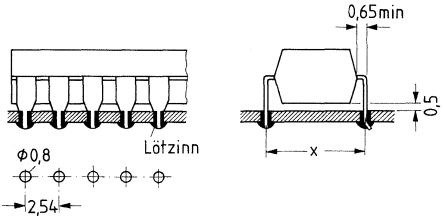
Der Gehäuseboden berührt nach dem Einsetzen die Leiterplatte nicht, weil die Anschlußfahnen kurz vor dem Gehäuse breiter werden **(siehe Bild 1)**.

Nach dem Einsetzen des Gehäuses in die Leiterplatte ist es vorteilhaft, zwei Anschlußenden in einem Winkel von ca. 30° zur Leiterplatte abzubiegen, während des Lötvorgangs braucht dann das Gehäuse nicht auf die Leiterplatte gepreßt werden.

Kunststoff-Steckgehäuse werden auf der dem Gehäuse abgewandten Plattenseite gelötet.

Die maximal zulässige Löttemperatur beträgt bei Handlötung 350 °C (max. 3 s) und bei Tauchlötung und Schwallötung 260 °C (max. 10 s).

Bild 1



Leistungs-Gehäuse mit 5, 7 und 9 Anschlüssen

Leistungsgehäuse weisen i.A. breitere Anschlüsse auf, so daß der erforderliche Lochkreisdurchmesser bei Leiterkarten 1,1 – 1,8 mm beträgt. Bei einem eventuellen Biegen der Anschlüsse darf keine mechanische Beanspruchung zwischen Anschlüssen und Gehäuse auftreten. Der Abstand vom Gehäuse zur Biegestelle ist min. 2 mm.

Löttemperatur siehe oben.

Kunststoff-Gehäuse (P-DSO und PL-CC) für die Oberflächenmontage (SMD)

Kolbenlötung:	Löttemperatur 350 °C max. 3 s. Abstand Gehäuse zur Lötstelle 1,5 mm min. Gehäusetemperatur max. 150 °C, keine mechanische Belastung der Anschlüsse zum Gehäuse
Dampfphasenlötung:	Löttemperatur 215 °C, Lötzeit max. 40 s, 2 x. (Vapor Phase Soldering)
Schwallötung:	Löttemperatur 260 °C, Lötzeit max. 8 s. (Anschlüsse und Gehäuse in das Zinnbad getaucht)

Lagerung, Vorbehandlung zur Weiterverarbeitung von ICs in PL-CC-Gehäusen

Die Bauelemente sind trocken zu lagern. Bei der Anwendung von Lötverfahren, die zu Hitzeschockbelastungen führen können, (z. B. Dampfphasenlöten) empfiehlt es sich ICs im PL-CC-Gehäuse 24 Stunden einem Trocknungsvorgang bei 125 °C zu unterziehen. PL-CC-68-Gehäuse sollten in diesem Fall trockenverpackt (Drypack) bezogen werden.

Sonstige Hinweise

Es ist darauf zu achten, daß zwischen Lötbad bzw. Lötkolben und Platine keine Ströme fließen können. Es wird daher empfohlen, die zu lötenden Anschlüsse und das Lötbad bzw. den Lötkolben an Masse zu legen.

Beim Vorbereiten und Einsetzen in die Platine sollen die Schaltungen vor statischer Aufladung geschützt werden. Auf keinen Fall dürfen die Bauteile bei eingeschalteter Betriebsspannung aus der Schaltung entnommen werden bzw. in die Schaltung eingefügt werden.

Die Erhöhung der Chiptemperatur beim Löten hat eine vorübergehend erhöhte elektrostatische Empfindlichkeit der integrierten Schaltungen zur Folge. Besondere Vorsicht ist daher vor Netztransienten, z. B. durch Schalten von Induktivitäten an Magnetrutschen usw. geboten.

3. Verarbeitungsrichtlinien für integrierte Schaltungen

Integrierte Schaltungen sind **e**lektrostatisch **g**efährdete **B**auelemente (**EGB**). Die Forderung nach immer größeren Integrationsdichten hat zu immer kleineren Strukturen auf den Halbleiterchips geführt, so daß heute grundsätzlich jede integrierte Schaltung bipolar, MOS und CMOS elektrostatisch geschützt werden muß.

MOS- und CMOS-Schaltungen enthalten meist in den Bausteinen integrierte Schutzschaltungen und sind durch rein statische Elektrizität kaum mehr zerstörbar. Andererseits besteht eine akuten Gefährdung durch elektrostatische Entladungen.

Von der Vielzahl möglicher Entladungsquellen sind neben aufgeladenen Personen vor allem aufgeladene Bausteine zu nennen. Bei niederohmigen Entladungen können Spitzenleistungen im kW-Bereich auftreten.

Zum Schutz der Bausteine sind folgende Grundsätze zu beachten:

- Verringerung der Aufladungsspannung – möglichst unter 220 V.
  Wirksame Mittel sind die Erhöhung der relativen Luftfeuchte auf ≧ 60% und das Ersetzen hochaufladbarer Kunststoffe durch antistatische Werkstoffe.
- Bei jeglicher Berührung der Bausteinanschlüsse ist mit einem Ladungsausgleich zu rechnen. Dieser soll stets hochohmig (ideal $R = 10^6$ bis $10^9\ \Omega$) erfolgen.

Zusammengefaßt heißt dies, daß integrierte Schaltungen eine besondere Handhabung erfordern, da unkontrolliert aufgebrachte Ladungen, Spannungen von nicht geerdeten Geräten oder Personen, Überspannungsspitzen oder andere ähnliche Einflüsse das Bauelement zerstören kann. Selbst wenn die Bauelemente Schutzschaltungen (z. B. Schutzdioden) an den Eingängen enthalten, müssen nachfolgende Handhabungsrichtlinien beachtet werden.

Kennzeichnung

Die Verpackung elektrostatisch gefährdeter Bauelemente wird mit folgendem Kennzeichen herstellerseitig versehen: 

Geltungsbereich:

Diese Richtlinie gilt für Lagerung, Transport, Prüfung und Verarbeitung aller Arten von integrierten Schaltungen, bestückten und gelöteten Leiterplatten, die mit solchen Bauelementen versehen sind.

Handhabung der Bauelemente

- Integrierte Schaltungen müssen bis zu ihrer Verarbeitung in der Verpackung bleiben.
- Die Handhabung von integrierten Schaltungen darf nur an speziell eingerichteten Arbeitsplätzen erfolgen. Diese Plätze müssen hochohmig leitende Beläge in der Größenordnung von 10^6 bis 10^9 Ω/cm haben.
- Bei Luftfeuchten > 50% genügt ein Arbeitsmantel aus reiner Baumwolle. Bei Verwendung von aufladbaren Kunstfasern soll die Kleidung enganliegend getragen werden. Das Handgelenkband muß fest an der Haut anliegen und über einen Ableitwiderstand von 50 kΩ bis 100 kΩ geerdet sein.
- Sind elektrisch leitende Fußböden $R_E = 5 \times 10^4$ bis 10^7 Ω vorhanden, dann kann durch Verwendung von sog. MOS-Stühlen und Schuhen mit elektr. leitender Sohle ($R_E \approx 10^5$ bis 10^7 Ω) ein weiterer Schutz erzielt werden.
- Alle Transporteinheiten für elektrostatisch gefährdete Bauelemente und bestückte Leiterplatten müssen zuerst durch Abstellen auf dem Arbeitsplatz bzw. Anfassen durch das beschäftigte Belegschaftsmitglied auf das gleiche Potential gebracht werden, bevor nach den einzelnen MOS-Bauelementen gegriffen wird. Der Potentialausgleich soll über einen Widerstand von 10^6 bis 10^8 Ω erfolgen.
- Beim Beschicken von Maschinen und Fertigungseinrichtungen ist zu beachten, daß die Bausteine aufgeladen aus der Verstandstange kommen und bei metallischer Berührung beispielsweise mit Maschinenteilen Schaden nehmen können.
- Bausteine können durch aufgeladene Personen u.U. in der Schiene zerstört werden, oder die Schiene aufgeladen verlassen, wenn diese von einer aufgeladenen Person entleert wird. Volumenleitende Schienen dürfen nur an EGB-Arbeitsplätzen (hochohmige Arbeitsplatz- und Personenerdung) gehandhabt werden.

Schädigungen können dadurch vermieden werden, daß die Bausteine über einen geerdeten Adapter aus hochohmigem Material (≈ 10^6 bis 10^8 Ω/cm) zwischen Schiene und Maschine entladen werden.

Von der Verwendung metallischer Schienen – insbesondere aus eloxiertem Alu – wird wegen der Gefahr hochohmiger Bausteinentladungen abgeraten.

Lagerung

Die Einlagerung von EGB nur an bestimmten, gekennzeichneten Lagerplätzen vornehmen.

Im Lager sollen die Bauelemente in der Anlieferverpackung verbleiben. Die Lagertemperatur sollte 60 °C nicht übersteigen.

Transport

EGB in zugelassenen Verpackungsschienen dürfen nur in geeigneten Behältern aus hochohmig leitenden bzw. langzeitantistatisch imprägnierten Kunststoffen, evtl. unlackiertem Holz transportiert werden. Behälter aus hochaufladbaren Kunststoffen oder aus sehr niederohmigen Materialien sind gleichermaßen ungeeignet.

Transportwagen und dessen Rollen sollen eine hinreichende elektrische Leitfähigkeit besitzen ($R < 10^6\ \Omega$). Schleifkontakte und Erdungsketten bieten keine zuverlässige Ladungsableitung.

Eingangsprüfung

Bei Eingangsprüfungen sind die Richtlinien zu beachten. Andernfalls erlischt ein evtl. Rückgaberecht bei Nichtbestehen der Eingangsprüfung.

Betriebsmittel und Montage

- Antriebsriemen von verarbeitenden Maschinen, soweit sie mit diesen Bauelementen in Berührung kommen (z. B. Biege- und Beschneidemaschinen, Transportbänder), sind mit Antistatikspray (z. B. Antistatikspray 100 der Fa. Kontaktchemie) zu behandeln. Besser ist es, solche Fälle ganz zu vermeiden.
- Müssen EGB von Hand ein- oder ausgelötet werden, sind nur Lötkolben ohne Thyristorregelung zu verwenden. Gegen Netztransienten haben sich Siemens Funkentstörkondensatoren vom Typ B 81711-A-B31...36 sehr gut bewährt.
- Mit EGB bestückte und gelötete Leiterplatten sind grundsätzlich als gefährdet zu betrachten.

Elektrische Prüfungen und Anwendungsschaltung

- Die Bauelemente sind unter Beachtung dieser Richtlinien zu verarbeiten. Vor dem Prüfen der bestückten und gelöteten Leiterplatten sind noch eventuell vorhandene Kurzschlußringe abzunehmen.
- Prüffassungen bzw. integrierte Schaltungen müssen beim Stecken oder Ziehen von Einzelbauelementen oder bestückten Leiterplatten spannungsfrei sein, wenn in den entsprechenden Werksunterlagen nichts anderes angegeben ist. Es ist sicherzustellen, daß die Prüfgeräte und Stromversorgungen keine Spannungsspitzen erzeugen, weder bei betriebsmäßigem Ein- und Ausschalten noch beim Ausfall der Netzsicherung oder beim Ansprechen anderer Sicherungen.
- Bei der Stromversorgung bipolarer integrierter Schaltungen ist immer zuerst die negative Spannung ($-U_S$ bzw. Masse) anzuschließen. Eine Unterbrechung dieses Potentials im Betrieb ist in der Regel nicht zulässig.
- Signalspannungen dürfen an Eingängen der integrierten Schaltungen erst mit oder besser nach dem Einschalten der Versorgungsspannung angelegt werden. Sie müssen mit oder möglichst vor dem Abschalten der Versorgungsspannung abgeschaltet werden.

- Stromversorgungen von integrierten Schaltungen sind möglichst nahe an den Versorgungsanschlüssen des ICs abzublocken. Bei bipolaren integrierten Schaltungen ist die Verwendung eines induktivitätsarmen Elektrolytkondensators, zumindest jedoch die Parallelschaltung eines Keramikkondensators von z. B. 100 nF bis 470 nF empfehlenswert.

  Bei integrierten Schaltungen mit hohen Ausgangsströmen muß der nötige Wert des Elektrolytkondensators der Prüf- bzw. Anwendungsschaltung angepaßt werden. Zu berücksichtigen sind Einschwingverhalten und dynamischer Ausgangswiderstand der Stromversorgungen, Leitungsinduktivitäten im Versorgungs- und Lastkreis und insbesondere induktive Lasten oder Motoren. Beim Abschalten von Leistungsinduktivitäten oder induktiver Lasten muß die gespeicherte Energie, wenn nicht anders angegeben, extern aufgenommen werden (z. B. durch einen Elektrolytkondensator, Dioden, Z-Dioden oder die Stromversorgung). Dabei ist auch ein Abschalten der Versorgungsspannung vor dem Zeitpunkt der Lastabschaltung zu beachten.
- Integrierte Schaltungen mit Tiefpasscharakter der Ausgangsstufen (z. B. PNP-Treiber oder PNP/NPN-Endstufen) benötigen in der Regel eine zusätzliche externe Kompensation am Ausgang. Dies gilt insbesondere bei komplexen Lasten. Bei NF-Leistungsverstärkern wird der Ausgang mit dem Boucherot-Glied kompensiert. Bei Brückenschaltungen genügt im Einzelfall die Überbrückung der Last mit einer Kapazität. Je nach Anwendung ist aber auch hier je ein Kondensator von jedem Ausgang gegen Masse zu empfehlen.
- Die Hinweise in den jeweiligen Datenblättern sind zu beachten.

Verpackung von bestückten Leiterplatten bzw. Flachbaugruppen

Das Verpackungsmaterial soll eine geringe Volumenleitfähigkeit besitzen:
$10^5\ \Omega/cm < p < 10^{10}\ \Omega/cm$.

In den meisten Fällen – insbesondere bei Luftfeuchten > 40% – wird diese Forderung von einfacher Wellpappe erfüllt.

Einen besseren Schutz erzielt man mit Beuteln aus hochohmig leitfähigem Polyäthylenschaum; (z. B. RCAS 1200 von Richmond, Redlands, Kalifornien; Vertreter Deutschland: Arno Marx, 7830 Emmendingen, Postfach 1129).

Grundsätzlich ist darauf zu achten, daß eine Berührung verschiedener Platinen ausgeschlossen wird.

In extremen Sonderfällen kann ein Schutz vor starken elektrischen Feldern notwendig sein, wenn sie beispielsweise von Transportbändern erzeugt werden können.

Hierfür wird eine Umhüllung mit Alu-Folie empfohlen, wobei eine direkte Berührung der Folie mit der Platine ausgeschlossen werden muß.

Pappschachteln mit innenliegender Alu-Folie, wie sie zum Versand unserer Bausteine verwendet werden, liefert z. B. Fa. Laber, München.

Ultraschallreinigung integrierter Schaltungen

Nachfolgende Empfehlung gilt für Kunststoffgehäuse. Für Hohlraumgehäuse (Metall und auch Keramik) sind gesonderte Vorschriften zu beachten.

Als Lösungsmittel kommen Freon und Isopropylalkohol (Handelsname Propanol) in Frage. Diese Lösungsmittel sind auch für Kunststoffgehäuse zulässig, da sie das Plastikmaterial nicht angreifen.

Ein Ultraschallbad in Doppel-Halbwellen-Betrieb ist aufgrund der geringen Bauteilebeanspruchung zu empfehlen.

Folgende Ultraschalleinwirkungen sind zulässig:

Schallfrequenz	$f >$ 40 kHz
Einwirkungszeit	$t <$ 2 min
Schallwechseldruck	$p <$ 0,3 atü
Schalleistung	$N <$ 0,5 W/cm²/Liter

4. Beschreibung der Datenangaben

Grenzdaten

Die Grenzdaten sind absolute Grenzwerte, bei deren Überschreitung auch nur eines Wertes die integrierte Schaltung zerstört werden kann.

Kenndaten

Die Kenndaten umfassen den garantierten Streubereich der Werte, die im angegebenen Betriebsbereich von der integrierten Schaltung eingehalten werden.

Unter den typischen Kenndaten werden Mittelwerte angegeben, die fertigungsmäßig erwartet werden. Wenn nicht anders vermerkt, gelten die typischen Kenndaten bei $T_A = 25\,°C$ und angegebener Speisespannung.

Funktionsdaten

Im Funktionsbereich werden die in der Schaltungsbeschreibung angegebenen Funktionen erfüllt.

5. Qualität

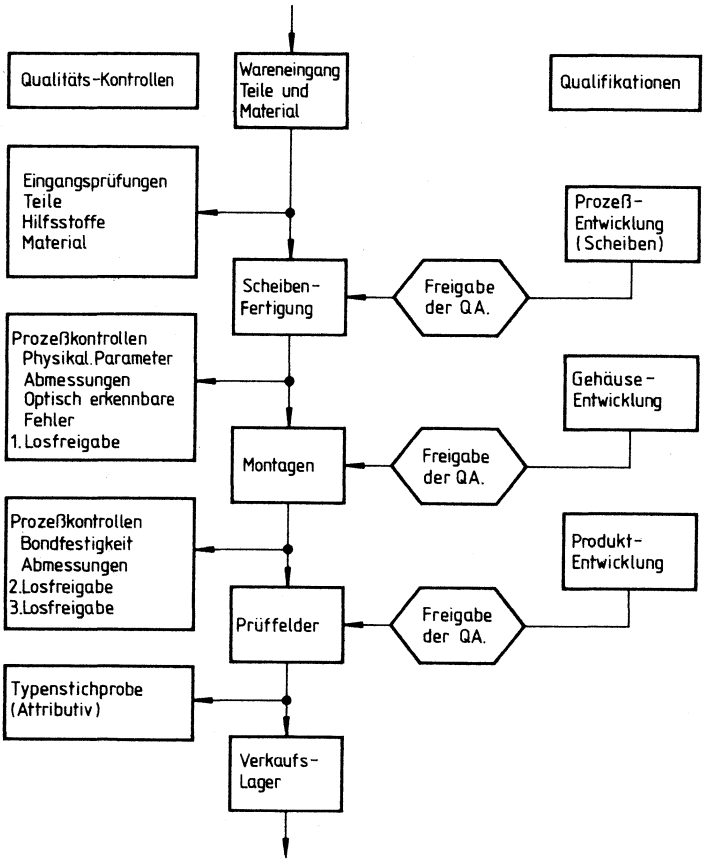
Qualitätssicherungssystem

Der hohe Qualitätsstandard der integrierten Schaltungen von Siemens ist das Ergebnis eines sorgfältigen Herstellungsprozesses, der in jeder Phase systematisch überwacht wird. Dazu dient ein Qualitätssicherungssystem, das in der Druckschrift „SIEMENS Qualitätssicherung bei integrierten Schaltungen", kurz „SQS-IC", ausführlich beschrieben ist.

Die wichtigsten Aspekte des „SQS-IC" sind in **Bild 2** dargestellt. Für die ausgewählten Kontrollmaßnahmen, Freigaben und Informationsrückkopplungsschleifen ist eine, von der Entwicklung und Fertigung unabhängige Qualitätssicherungsabteilung (QA) verantwortlich. Diese Abteilung verfügt über modernste Prüf- und Meßeinrichtungen, sie arbeitet mit den bewährten Methoden der statistischen Qualitätskontrolle, und sie ist mit Einrichtungen für beschleunigte Lebensdauer- und Umweltkontrolltests ausgestattet, die zu Eignungs- und Routineüberwachungsprüfungen eingesetzt werden.

Zur ständigen Weiterentwicklung von Qualität und Zuverlässigkeit werden modernste Präparationsmethoden und Analysegeräte eingesetzt.

Bild 2


Qualitäts-Kontrollen
Wareneingang Teile und Material
Qualifikationen
Eingangsprüfungen Teile Hilfsstoffe Material
Prozeß-Entwicklung (Scheiben)
Scheiben-Fertigung
Freigabe der Q.A.
Prozeßkontrollen Physikal. Parameter Abmessungen Optisch erkennbare Fehler 1. Losfreigabe
Gehäuse-Entwicklung
Montagen
Freigabe der QA.
Prozeßkontrollen Bondfestigkeit Abmessungen 2.Losfreigabe 3.Losfreigabe
Produkt-Entwicklung
Prüffelder
Freigabe der QA.
Typenstichprobe (Attributiv)
Verkaufs-Lager

Auslieferungsqualität

Jede integrierte Schaltung wird als Abschluß des Fertigungsprozesses einer Endprüfung unterzogen. Da diese Prüfung häufig Hunderttausende von Betriebszuständen, viele statische und dynamische Parameter zu berücksichtigen hat, wird sie von rechnergesteuerten Prüfautomaten durchgeführt. Diese Automaten sind äußerst zuverlässig. Die Qualitätssicherungsabteilung führt schließlich eine losweise Stichprobenprüfung der ICs durch, um so diese minimale Fehlerquote sowie die Herstellungsgrenzqualität (AQL) zu gewährleisten. Die Stichprobenprüfung bedient sich der Stichprobenpläne der DIN 40 080 oder der identischen MIL-STD-105 oder IEC 410.

Die Ergebnisse solcher Stichprobenprüfungen, die an Millionen von ICs im Jahre 1989 durchgeführt wurden, sind in der nachfolgenden Tabelle wiedergegeben. Diese Ergebnisse entsprechen der mittleren Auslieferungsqualität (Average Outgoing Quality, kurz: AOQ) und werden in „**d**efectives **p**er **m**illion" (DPM) angegeben.

	Summe elektr. Fehler AOQ (DPM)	Summe mech. Fehler AOQ (DPM)
SSI/MSI/LSI/VLSI	107	203

Zuverlässigkeit

Maßnahmen bei der Entwicklung

Die Zuverlässigkeit der ICs wird bereits während der Entwicklung wesentlich beeinflußt. Deshalb hat Siemens für die Entwicklung der Schaltungen und Layouts Entwurfsregeln festgelegt, die u.a. die minimalen Breiten und Abstände von Leitbahnen auf dem Chip festlegen, die Abmessungen und elektrischen Parameter von Schutzschaltungen gegen elektrostatische Aufladungen angeben, und ähnliches mehr. Ausgefeilte Überprüfungsprogramme, die auf Großrechnern laufen, garantieren eine umgehende Lokalisierung und Behebung unbeabsichtigt eingetretener Verstöße gegen diese Entwurfsregeln.

Prozeßkontrolle in der Fertigung

Die Herstellung integrierter Schaltungen umfaßt mehrere hundert Fertigungsschritte. Da jeder Schritt fehlerfrei ausgeführt sein soll, kommt der Prozeßkontrolle eine überragende Bedeutung zu. Manche Prozesse enthalten mehr als hundert Kontrollmaßnahmen. Die Kontrollen sind so angelegt, daß die Stabilität der Prozeßparameter der Fertigungsschritte gesichert ist.

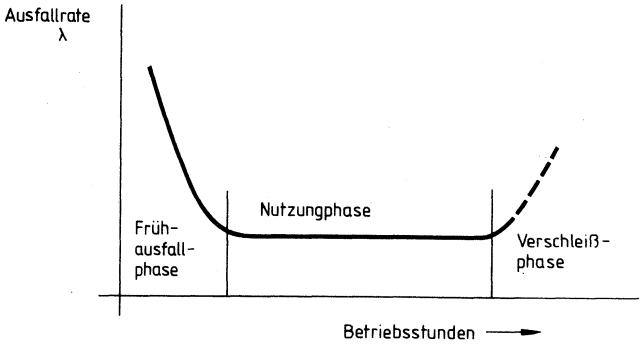
In den ständig sinkenden Ausfallraten zeigen sich die Erfolge dieser Bemühungen; im Laufe der Jahre wurde die Ausfallrate wesentlich reduziert, und dies trotz der erheblich gestiegenen Komplexität der ICs.

Beispielsweise konnte im Jahre 1989 bei beschleunigten Lebensdauertests an etwa 80 000 ICs mit verschiedener Komplexität eine durchschnittliche Langzeitausfallrate von etwa 60 FIT abgeschätzt werden.

Zuverlässigkeitsüberwachung

Der allgemeine Verlauf der Ausfallrate bei ICs über die Zeit wird durch die sogenannte Badewannenkurve beschrieben **(s. Bild 3)**. Die Ausfallrate ist in den ersten Betriebsstunden am höchsten (Frühausfallphase). Nach Abklingen der Frühausfallphase beginnt die „konstante" Ausfallphase, während der Ausfälle in einer nahezu gleichbleibenden Anzahl auftreten können. Diese Phase endet mit einem Wiederanstieg der Kurve während der Verschleißphase. Für integrierte Schaltungen liegt diese Phase in aller Regel weit über der praktischen Betriebszeit der Geräte.

Bild 3



Zuverlässigkeitsuntersuchungen an ICs sind in der Regel zerstörende Untersuchungen. Sie werden daher in Stichproben durchgeführt. Die meisten Ausfallmechanismen laufen bei höheren Temperaturen schneller ab. Auf Grund dieser Temperaturabhängigkeit, kann die zur Simulation späterer Betriebsverhalten geforderte Zeit durch Anwenden höherer Temperaturen verkürzt werden; hierunter versteht man den Lebensdauertest.

Der Beschleunigungsfaktor F im Lebensdauertest errechnet sich aus der Arrheniusschen Gleichung

$$F = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

wobei T_2 die Temperatur ist, bei welcher der Lebensdauertest durchgeführt wird, T_1 die angenommene Betriebstemperatur und k die Boltzmann-Konstante ist.

Maßgebend für den Faktor F ist die Aktivierungsenergie E_A, die für Ausfallmechanismen sehr unterschiedlich ist und zwischen 0,3 und 1,3 eV liegt.

Für alle Siemens ICs werden Zuverlässigkeitsangaben aus Lebensdauertestuntersuchungen mit einer mittleren Aktivierungsenergie von 0,5 eV auf eine Betriebstemperatur von $T_A = 55\,°C$ umgerechnet. Damit ergibt sich ein Beschleunigungsfaktor für den Lebensdauertest von 24 gegenüber dem Betriebsverhalten. So werden auch Ausfallmechanismen berücksichtigt, die eine geringe Aktivierungsenergie haben, d. h. in geringer Weise durch die Temperaturauswirkung beschleunigt werden.

An Typen von integrierten Schaltungen, die repräsentativ sind für die Fertigungslinien, werden – wie in der „SQS-IC" beschrieben – routinemäßig verschiedene Zuverlässigkeitsprüfungen durchgeführt. Solche Prüfungen sind u.a. Feuchtklima-Tests bei 85 °C und 85% Feuchte, Dampfdruck-Test, sowie Lebensdauerprüfungen bis 1000 Stunden und mehr. Die Untersuchungsergebnisse liegen in Form zusammenfassender Berichte vor.

6. Logikpegel und Symbole

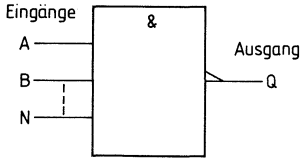
nach DIN 40900, Teil 12

Logikpegel

Für digitale Mikroschaltungen werden die zwei möglichen Bereiche der binären elektrischen Größe mit L (low) und H (high) bezeichnet. Dabei liegen die Werte des L-Bereichs näher bei $-\infty$ und die Werte des H-Bereichs näher bei $+\infty$. Entsprechend gelten die Indizes A für die Angabe des oberen Wertes (näher bei $+\infty$) und B für die untere Grenze (näher bei $-\infty$).

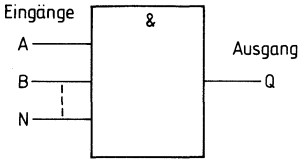
Schaltzeichen

NAND-Element



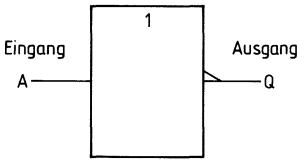
Logische Funktion: $Q = \overline{A \wedge B .. \wedge N}$
Definition: Der Ausgang zeigt nur dann L-Signal, wenn A und B und ... und N auf H-Signal liegen.

UND-Element



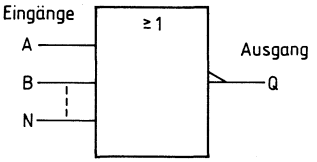
Logische Funktion: $Q = A \wedge B \; . . \wedge N$
Definition: Der Ausgang zeigt nur dann H-Signal, wenn A und B und ... und N auf H-Signal liegen.

Inverter



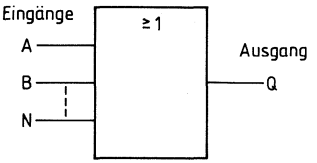
Logische Funktion: $Q = \overline{A}$

NOR-Element



Logische Funktion: $Q = \overline{A \vee B .. \vee N}$
Definition: Der Ausgang zeigt nur dann H-Signal, wenn A und B und ... und N auf L-Signal liegen.

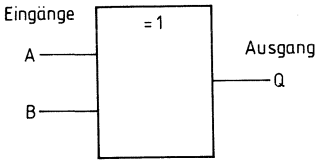
ODER-Element



Logische Funktion: $Q = A \vee B \; . . \vee N$
Definition: Der Ausgang zeigt nur dann L-Signal, wenn A und B und ... und N auf L-Signal liegen.

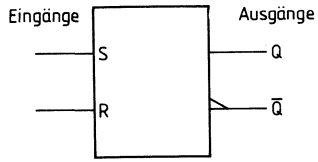
Schaltzeichen (Fortsetzung)

Exklusiv-ODER-Element

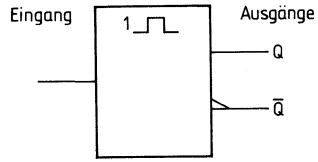


Logische Funktion: $Q = (A \wedge \overline{B}) \wedge (\overline{A} \wedge B)$
Definition: Der Ausgang zeigt nur dann H-Signal, wenn entweder nur A oder nur B auf H-Signal liegen.

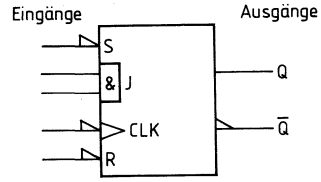
Symbole für Bistabile Schaltungen



Bistabile Schaltung (Flipflop)



Monostabile Schaltung (Monoflop)



J1, J2 und K sind Informationseingänge
J1 und J2 sind UND-verknüpft
J- und K-Eingänge werden vom CLK-Eingang (Takt) gesteuert
S und R sind direkt wirkende Eingänge (Setzen, Rücksetzen)

7. Alphabetische Zusammenstellung der verwendeten Kurzzeichen (siehe S. 50).

Definition

Integrierte Operationsverstärker sind Gleichspannungsverstärker mit einem sehr breiten Anwendungsfeld in der Regelungstechnik, der industriellen Elektronik sowie in der NF-Technik.

Schaltzeichen und Bezeichnungen

Im Schaltzeichen „Operationsverstärker" werden nur Eingangs- und Ausgangsanschlüsse gezeichnet. **Bild 1** zeigt das verwendete Schaltzeichen, wobei Anschluß 1 den „invertierenden Eingang", Anschluß 2 den „nicht invertierenden Eingang" und Anschluß 3 den Ausgang kennzeichnet. Dabei hat ein positives Signal an 1 ein negatives Signal an 3 zur Folge.

Bild 1

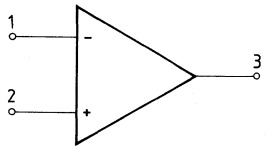


Bild 2

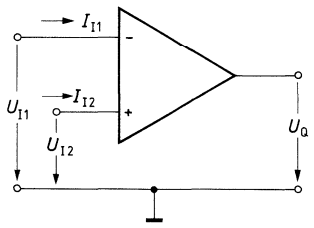


Bild 3

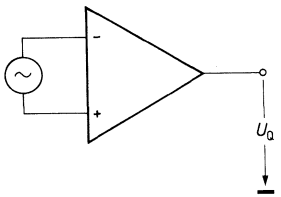
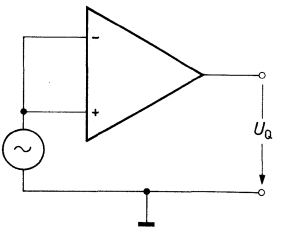


Bild 4



Die Definition der wichtigsten Bezeichnungen, die einen Operationsverstärker im allgemeinen ausreichend charakterisieren, sind im folgenden zusammengestellt. Alle Angaben beziehen sich auf symmetrische Versorgungsspannungen.

a) Eingangs-Null-Spannung (Eingangs-Offset-Spannung) U_{I0} ist diejenige Spannungsdifferenz, die an den Eingängen angelegt werden muß, damit der Ausgang auf 0 V liegt **(Bild 2)**.
$U_{I0} = U_{I1} - U_{I2}$ bei $U_Q = 0$
und Gesamtwiderstand $R_G = 50\ \Omega$.

b) I_I ist der mittlere statische Eingangsstrom, der für die Funktion des OP notwendig ist **(Bild 2)**.

$$I_I = \frac{I_{I1} + I_{I2}}{2}$$

c) Eingangs-Null-Strom (Eingangs-Offset-Strom) I_{I0S} ist die Differenz der Eingangsströme im Arbeitsbereich. Er kann bei hohem Generatorwiderstand störend wirken **(Bild 2)**.

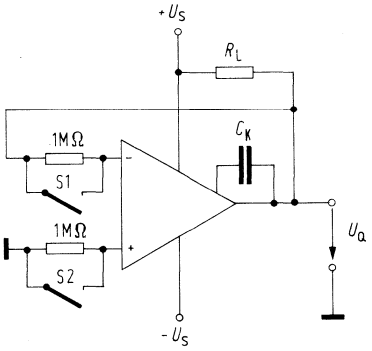
d) Leerlauf (-Spannungs) Verstärkung V_{U0} ist die Verstärkung ohne Gegenkopplung **(Bild 3)**.

$$V_{U0} = \frac{U_Q}{U_I}$$

e) Gleichtaktverstärkung V gibt die Verstärkung eines an beiden Eingängen gleichphasig eingespeisten Signals an **(Bild 4)**.

Prüfschaltungen für Operationsverstärker

Eingangsstrom, Eingangsnullstrom

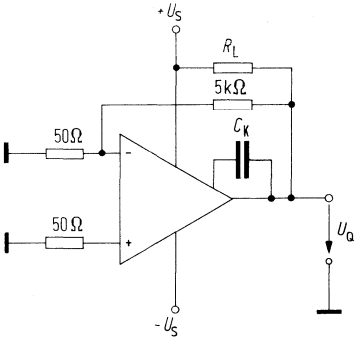


S1 offen – S2 geschlossen: $I_{I-} = \frac{U_Q}{1\,M\Omega}$

S2 offen – S1 geschlossen: $I_{I+} = \frac{U_Q}{1\,M\Omega}$

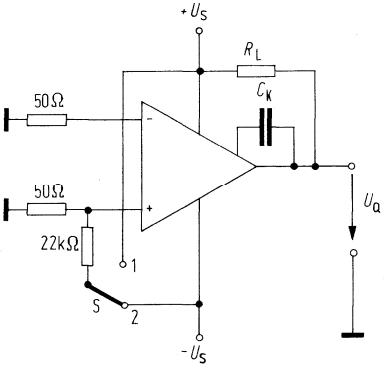
S1 + S2 offen: $I_{IO} \approx \frac{U_Q}{1\,M\Omega}$

Eingangsnullspannung



$-U_{IO} = U_{QO}/V_{UO}$; $V_{UO} = 100$; $-U_{IO} = \frac{U_{QO}}{100}$

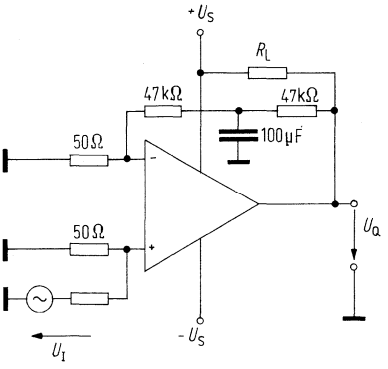
Ausgangsspannung, Aussteuerfähigkeit



S in Stellung 1: $U_Q = U_{QL}$;

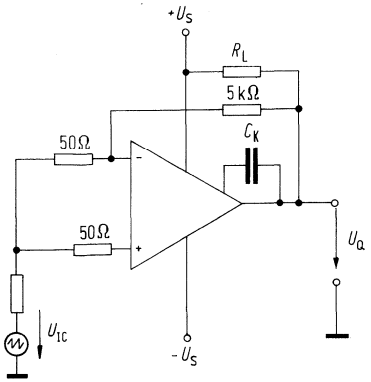
S in Stellung 2: $U_Q = U_{QO}$

Leerlaufspannungsverstärkung bei $f = 1$ kHz



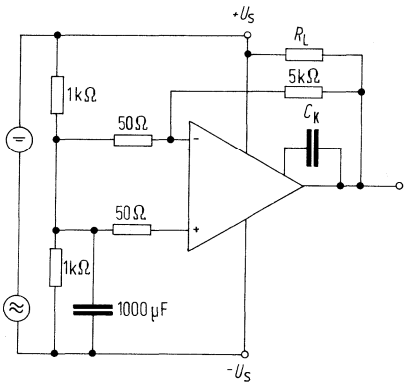
$V_{UO} = 20\ \text{lg}\ \frac{U_Q}{U_I}$ [dB]

Gleichtaktunterdrückung



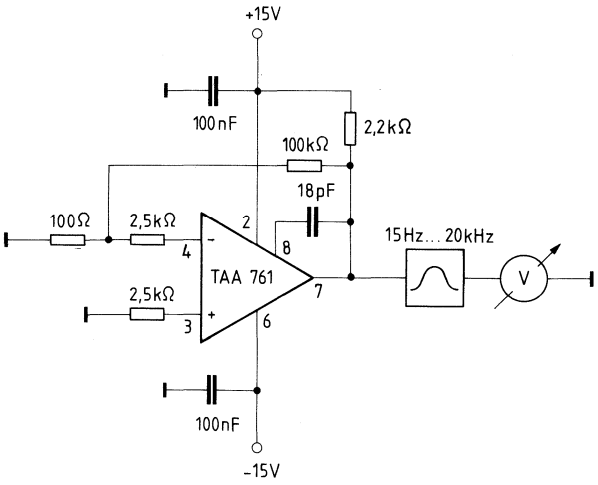
$$V_{UC} = \frac{\Delta U_Q}{\Delta U_{I_C}}; k_{CMR} = 20\ \lg\ \frac{V_{U0}}{V_{UC}}\ [dB]$$

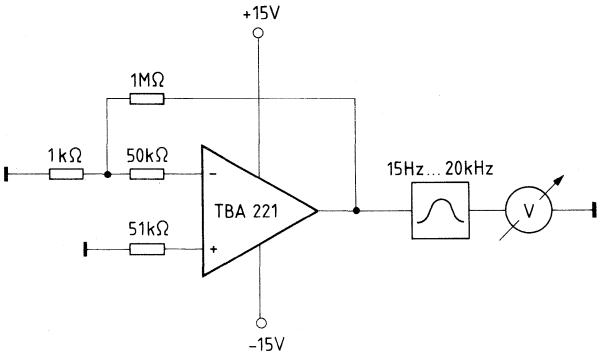
Betriebsspannungsunterdrückung



$$\frac{\Delta U_{IO}}{\Delta U_S} = \frac{\Delta U_Q}{100 \cdot \Delta U_S}$$

Rauschspannung nach DIN 45 405 – Psophometer U 2033 (Fa. Siemens)
Stellung: Geräuschspannung, Bewertung Spitze/Null





Zusammenhang von max. Anstiegsgeschwindigkeit (Slew-Rate *S*) und Sinus-Aussteuerbarkeit bei höheren Frequenzen (Leistungsbandbreite f_p)

Die maximale Anstiegsgeschwindigkeit eines Operationsverstärkers wird durch die Umladung eines Kondensators in der Schaltung bestimmt. Für einen Kondensator gilt:

die Ladung $Q = C \cdot U$ bzw. $Q = \int I \cdot dt$

Die Änderung der Spannung am Kondensator erfolgt entsprechend: $\Delta U/\Delta t \approx du/dt = I/C$.

Bei gegebenem Strom ist eine schnellere Umladung des Kondensators nicht möglich. Diese maximale Umladegeschwindigkeit ist für Operationsverstärker als Faktor *S* in V/µs angegeben.

Übliche Werte liegen in der Größenordnung von 0,3 bis 20 V/µs.

Die maximal unverzerrt übertragene Frequenz eines Sinussignals wird bestimmt durch die maximale Anstiegsgeschwindigkeit im Nulldurchgang ($t = 0$).

Das Sinussignal der Amplitude U_{QS} und der Kreisfrequenz ω ($= 2\pi f$) hat eine Anstiegsgeschwindigkeit, die durch die erste Ableitung dieser Funktion beschrieben wird:

Signal: $U_q = U_{QS} \cdot \sin(\omega t)$	für $t = 0$: $\cos(\omega t) = 1$
erste Ableitung: $du_q/dt = U_{QS} \cdot \omega \cdot \cos(\omega t)$	daher: $du_q/dt_{max} = U_{QS} \cdot \omega \cdot 1 = U_{QS} \cdot 2\pi f$

Dieser Wert muß für eine verzerrungsfreie Aussteuerung kleiner/gleich der maximalen Anstiegsgeschwindigkeit des Operationsverstärkers sein.

$$S \geq U_{QS} \cdot 2\pi f; \text{ daraus folgt: } f_p = \frac{S}{2 \cdot \pi \cdot U_{QS}} = \frac{S}{2 \cdot \pi \cdot \sqrt{2} \cdot U_{Qeff}}; \quad U_{Qeff} = \frac{S}{2 \cdot \pi \cdot \sqrt{2} \cdot f_p}$$

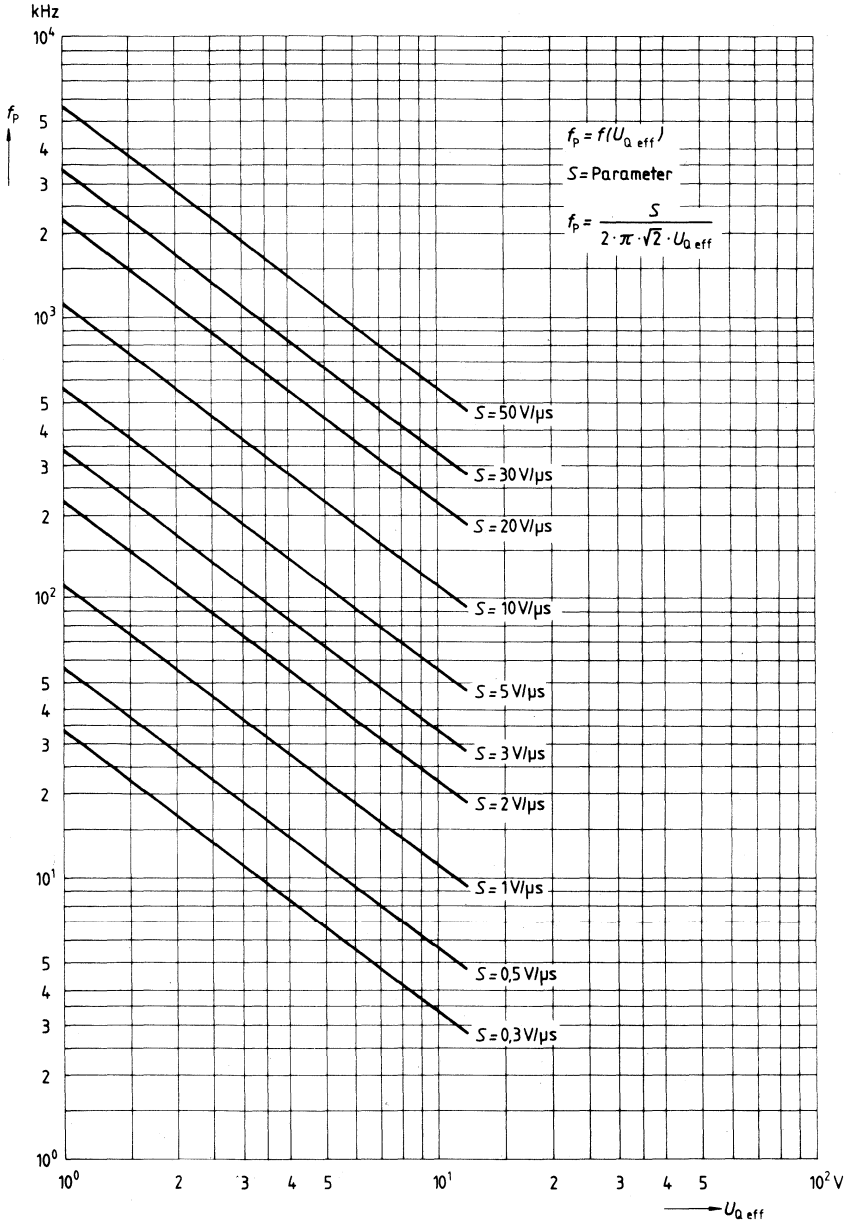
Beispiel 1: $S = 0{,}5$ V/µs ($\triangleq$ 500 000 V/s); $U_{Qeff} = 10$ V; $f_p = \dfrac{500000}{2 \cdot \pi \cdot \sqrt{2} \cdot 10} = 5{,}62$ kHz

Soll ein 10-kHz-Signal übertragen werden, so ist dies verzerrungsfrei bis effektiv 5,62 V möglich.

Beispiel 2: $S = 10$ V/µs; $U_{Qeff} = 10$ V; $f_p = 112$ kHz

Die Bandbreite kann natürlich nicht (wie lt. Rechnung möglich) unendlich werden. Zusätzlich gilt die Begrenzung durch die Kleinsignal-Grenzfrequenz (f_T).

Slewrate und Leistungsbandbreite



Hinweise für den Einsatz integrierter Operationsverstärker

Bei fast allen integrierten OPs sind Schutzmaßnahmen realisiert, um eine gewisse Stör- und Zerstörsicherheit zu erreichen.

Dennoch kann es bei gleichzeitigem Erreichen mehrerer Grenzbedingungen (max. Ausgangsströme, max. T_U, Kurzschlüsse etc.) zu Fehlfunktionen oder Ausfällen kommen.

Das gilt ebenfalls, wenn die Ausgänge stark induktiv und kapazitiv belastet sind, denn induktive Lasten erzeugen Rückschlagspannungen und kapazitive Lasten >1 nF extreme Stromspitzen.

Große kapazitive Lasten ($\geq$ 100 pF) können bei OPs mit hohen Anstiegsgeschwindigkeiten und hohen Ausgangsströmen (z. B. TAE 2453/4453) zu Stabilitätsproblemen führen.

Es sind hierfür allgemein 2 Abhilfemaßnahmen bekannt:

- Begrenzung der Ausgangsspitzenströme **(Bild 1, 3, 4)**
- Stärkere – oder zusätzliche Frequenzkompensation **(Bild 2)**

Dieses Problem wird auch dann entschärft, wenn man vermeidet, den Ausgang hart in die Sättigung zu steuern, d. h. Ruhearbeitspunkteinstellung in der Mitte des Aussteuerbereiches, analoges Ausgangssignal kleiner als der mögliche Aussteuerbereich.

Der Minimalwert für die Frequenzkompensationskapazität ist im Datenbuch angegeben für

Generatorwiderstände	>10 kΩ
Streukapazitäten	<5 pF auf den Summierpunkt
Lasten	<100 pF

In Fällen, die davon abweichen, kann es erforderlich sein, eine stärkere Frequenzkompensation zu verwenden und/oder eine Vorwärtskompensation von Eingang zu Ausgang (siehe auch TAA 762 Meßschaltung 2 und **Bild 1**).

Für Präzisionsanwendungen bzw. Betrieb im Leerlauf empfehlen wir auf der Druckplatine beide Eingänge mit einem Schirmschutzring zu umgeben, sowie die Leitungen zu den Eingängen mit geschirmter Litze auszuführen.

Eine solche Schirmung empfielt sich ebenfalls bei Anwendungen mit kleinen Eingangsströmen (bzw. äußerst hohem Gegenkopplungswiderstand). Sie verhindert parasitäre Ströme auf der Druckplatine, die z. B. durch unsaubere Oberflächen zustande kommen können.

Bild 1

Verbesserung der Stabilität bei großen kapazitiven Lasten ≥ 100 pF durch Begrenzung der Stpitzenströme mit *R*.

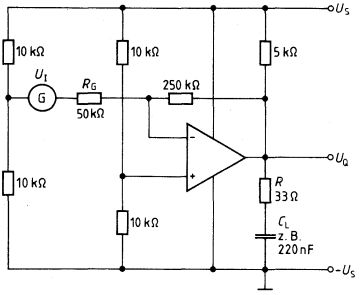


Bild 2

Kompensation am Eingang mit ca. 220 Ω und 10 nF, wenn kein Kompensationspunkt am OP verfügbar ist, z. B. bei Verstärkung 1, Integratoren und hohen kapazitiven Lasten.

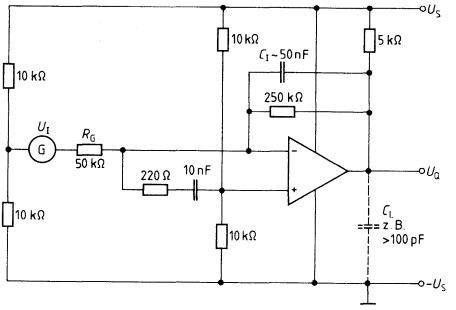


Bild 3

Schutz der Eingänge und Ausgänge und Kompensation der Streukapazität C_S

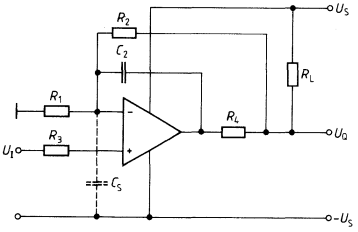
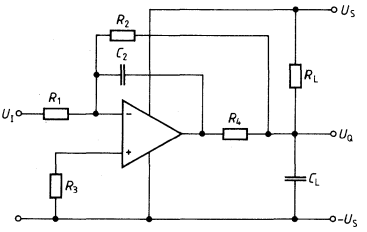


Bild 4

Beschaltung bei großen kapazitiven Lasten



Verstärkung

$$V = \frac{R_1 + R_2}{R_1}$$

Kompensation

$$C_2 = \frac{R_1}{R_2} \; C_S$$

Verstärkung

$$V = \frac{R_2}{R_1}$$

R_3: Schutz für Eingang
R_4: Schutz für Ausgang
R_L: Kollektorwiderstand
(bei OPs mit offenem Kollektorausgang immer erforderlich)

1. Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained to the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron, Avenue Louise, 430 (B. 12); B-1050 Brussels, Belgium.

2. Mounting Instructions

Plastic Package

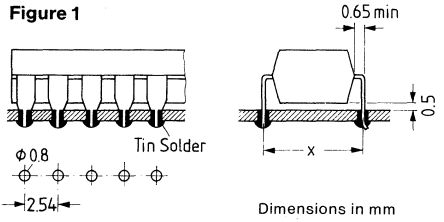
The pins are bent downwards by an angle of 90° and fit into holes with a diameter of 0.7 to 0.9 mm spaced 2.54 mm apart. The dimension x is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see Figure 1)**

After insertion of the package into the printed circuit board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for manual soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Power Package with 5, 7 or 9 Pins

Power packages generally have wider pins, meaning that the hole diameter on the PCB must be 1.1 to 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

See above for soldering temperatures.

Plastic Packages (P-DSO and PL-CC) for Surface Mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm; package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s, 2 x.
Wave soldering:	soldering temperature 260 °C, max. soldering time 8 s. (pins and package are dipped into the tin bath)

Storage, Pretreatment for Processing of ICs in PL-CC Packages

The components are to be stored in a dry place. For soldering methods which may lead to a thermal shock stress (e.g. vapor phase soldering) it is recommended to dry the ICs in PL-CC package at 125 °C for a period of 24 hours. PL-CC-68 packages are also available in drypack.

Other Points to Note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted when the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through switching of inductances on magnetic chutes, etc.

3. Processing Guidelines for ICs

Integrated circuits (ICs) are electrostatic-sensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from electrostatic discharges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

- Reduction of charging voltage, below 200 V if possible.
  Means which are effective here are an increase in relative humidity to $\geqq 60\%$ and the replacement of highly charging plastics by antistatic materials.
- With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^9\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons. Surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

Scope

The guidelines apply to the storage, transport, testing and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of Devices

- ICs must be left in their containers until they are processed.
- ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 Ω/cm.
- With humidity of > 50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn tightly on the skin and be grounded across a resistor of 50 to 100 kΩ.
- If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
- All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
- When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e. g. machine parts.
- The devices in the case may be destroyed by charged persons or come out of the case charged if this is emptied by a charged person. Conductive cases may only be handled at ESS work stations (high-resistance work-station and person grounding).

Damage can be avoided by discharging the devices across a grounded adaptor of high-resistance material ($\approx 10^6$ to 10^8 Ω/cm) between the case and the machine.

The use of metal case – especially of anodized aluminium – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing cases should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

- The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e. g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e. g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
- If ESS devices have to be soldered of desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ...-B36 have proven very effective against line transients.
- Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical Tests and Application Circuit

- The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
- The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
- When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has first to be connected. In general, an interuption of this potential during operation is not permissible.
- Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
- Power supplies of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.

  Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or appliction circuit. Transient behaviour and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered. When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e. g. by an electrolytic capacitor, diodes, Z-diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.
- ICs with low-pass characteristic of the output stages (e. g. PNP drivers or PNP/NPN end stages), normally need an additional external compensation at the output. This applies particulary to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.
- Observe any notes and instructions in the respective data sheets.

Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < p < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled by simple corrugated board. Better protection is optained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminium foil is recommended, although direct contact between the film and the PCB must be avoided Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz;	exposure	$t < 2$ min
alternating sound pressure	$p < 29$ kPa;	sound power	$N < 0.5$ W/cm²/liter

4. Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25$ °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5. Quality Assurance System

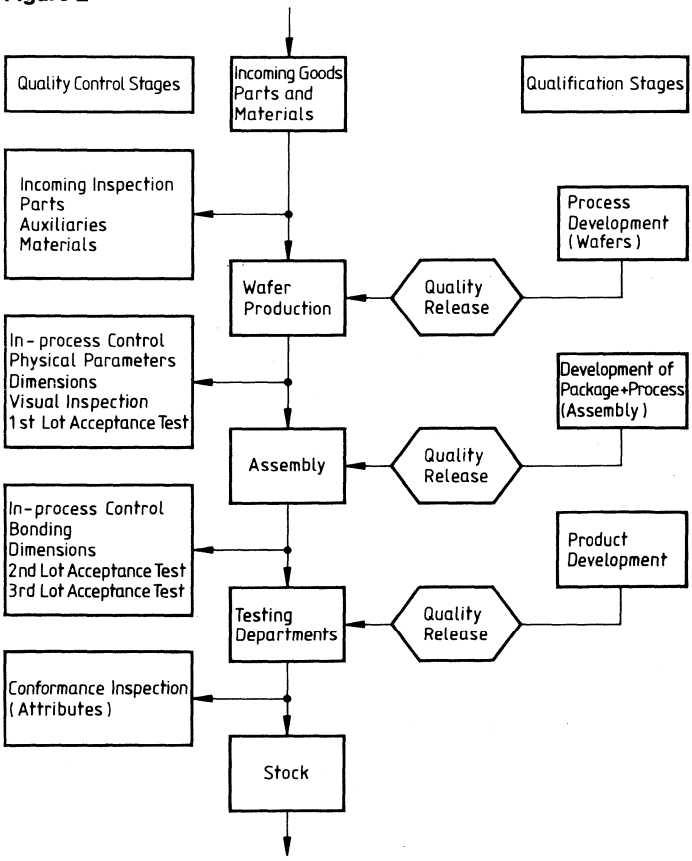
The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure 'Siemens Quality Assurance – Integrated Circuits' (SQS IC).

Figure 2 shows the most important stages of the "SQS IC". A quality assurance (QA) departement which is independent of producction and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achive continuity of quality and reliability.

Figure 2



Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40 080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with millions of ICs during 1989. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
SSI/MSI/LSI/VLSI	107	203

Reliability

Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e. g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-Process Control during Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

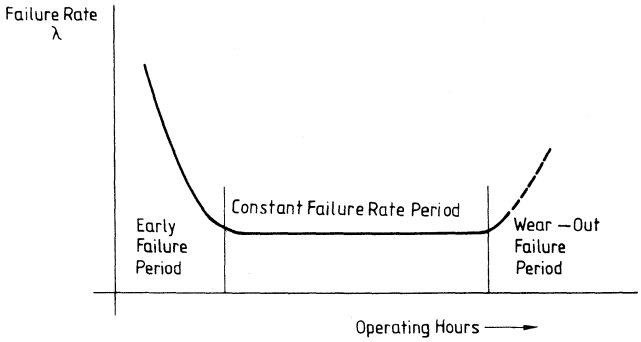
The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1989 the typical random failure rates estimated for accelerated life tests with almost 80 000 ICs of all complexities are found to be around 60 fit.

Reliability Monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve **(Figure 3)**. The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 3



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behaviour within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be optained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 55\,°C$, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behaviour. This method considers also failure mechanisms with low activation energy, i. e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS IC". Such tests are e. g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1 000 hours and more. Test results are available in the form of summary reports.

6. Logic Functions and Symbols

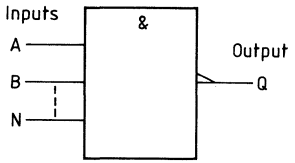
in accordance with DIN 40900, part 12

Logic Levels

For digital microcircuits, the two possible binary states are designated L (low) and H (high). The values of the L range are closer to $-\infty$ and those of the H range closer to $+\infty$. Similarly, the index A applies to the upper limit value (closer to $+\infty$) and index B to the lower limit value (closer to $-\infty$).

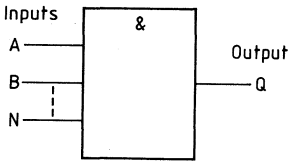
Gate Symbols

NAND



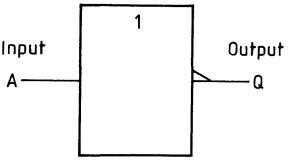
Logic function: $Q = \overline{A \wedge B \quad \ldots \wedge N}$
Definition: an L signal will only be present at the output if A and B and . . . and N show an H signal.

AND



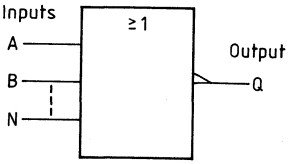
Logic function: $Q = A \wedge B \quad \ldots \wedge N$
Definition: an H signal will only be present at the output if A and B and . . . and N show an H signal.

Inverter



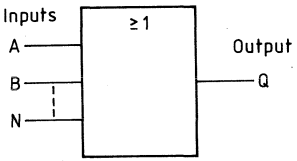
Logic function: $Q = \overline{A}$

NOR



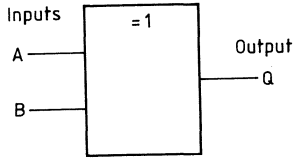
Logic function: $Q = \overline{A \vee B \vee \ldots \vee N}$
Definition: an H signal will only be present at the output if A and B and . . . and N show an L signal.

OR



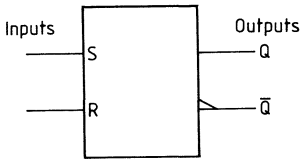
Logic function: $Q = A \vee B \vee \ldots \vee N$
Definition: an L signal will only be present at the output if A and B and . . . and N show an L signal.

Exclusive OR

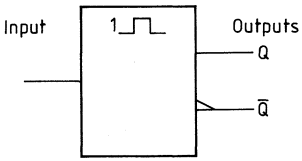


Logic function: $Q = (A \wedge \overline{B}) \wedge (\overline{A} \wedge B)$
Definition: an H signal will only be present at the output if either only A or only B shows an H signal.

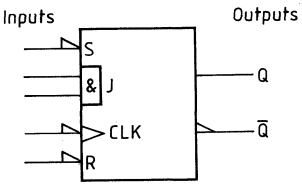
Symbols for Bistable and Monostable Elements



Bistable element (flipflop)



Monostable element (monoflop) with an input acting upon both outputs



J1, J2 and K are information inputs.
J1 and J2 are AND connected.
Inputs J and K are (clock-) controlled by the input CLK.
S and R are independent set and reset inputs.

7. Summary of Terms and Symbols in Alphabetical Order

A, B	Indices for limit value
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwith
C	Capacitance
C_i, C_f	Input capacitance
C_{CLK}, $C_\varnothing$	Clock capacitor
CLK	Clock
DC	Direct current
D	Differential
f	Frequency
Δf	Frequency deviation
FM	Frequency modulation
f_i, f_I	Input frequency
f_q, f_Q	Output frequency
G	Gain
G	giga (10^9)
GND	Ground
Hy	Hysteresis
Hz	Cycles per second (Hertz)
I	Input
I,	Current
I_S	Current consumption
IF	Intermediate frequency
k	kilo (10^3)
K	Kelvin
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Modulation factor
MW	Medium wave
N, n	Noise
o	Offset
OSC	Oscillator
P, P_V	Power dissipation
P_{tot}	Max. perm. power dissipation
pp	Peak-to-peak
Q	Output
Q, Q_B	Q-factor
R	Resistance
$R_{th\ JC}$	Thermal resistance (junction-case)
$R_{th\ SC}$	Thermal resistance (system-case)
$R_{th\ SA}$	Thermal resistance (system-air)
RF	Radio frequency
$\frac{S+N}{N}$	Signal-to-noise ratio
T	Cycle time
T	Temperature
TC	Temperature coefficient
t	Time
T_A	Ambient temperature in operation
T_{stg}	Storage temperature
T_j	Junction temperature
t_H	Hold time
t_I	Input pulse duration
t_n	Instant prior to clock pulse
t_{n+1}	Instant after clock pulse
t_P	Average pulse transit time
t_{pd}	Pulse delay time
$t_{P\ HL}$	HL pulse transit time
$t_{P\ LH}$	LH pulse transit time
t_{pI}	Input pulse duration
$t_{p\ Q}$	Output pulse duration
$t_{p\ R}$	Reset pulse duration
$t_{p\ S}$	Set pulse duration
$t_{p\ CLK}$	Clock pulse duration
$t_{p\ Z}$	Count pulse duration
t_s	Set-up time
t_T	Signal transition time
t_t	Dead time
t_Q	Output pulse duration
$t_{T\ HL}$	HL transition time
$t_{T\ LH}$	LH transition time
THD	Total harmonic distortion
V	Volt
V, v	Voltage, general
V_{Hy}	Hysteresis voltage
V_i, V_I	Input voltage
V_q, V_Q	Output voltage
V_R	Reverse voltage
V_S	Supply voltage
W	Watt
Z	Impedance
Z	Zener

Definition

Integrated operational amplifiers (op amps) are DC voltage amplifiers with a very broad scope of applications in control technology, industrial electronics, and in audio frequency engineering.

Graphical Symbols and Terms Used

The graphical symbol "operational amplifier" shows only signal inputs and outputs. **Figure 1** shows the graphical symbol used, with an "inverting" input 1, a "non-inverting" input 2, and an output 3. A positive signal at input 1 results in a negative signal at output 3.

Figure 1

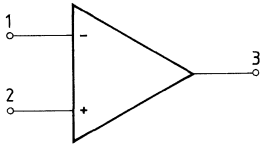


Figure 2

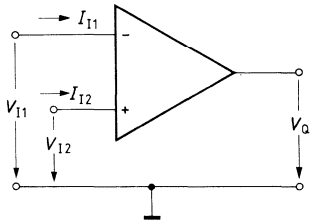


Figure 3

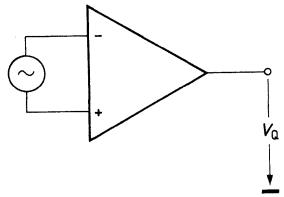
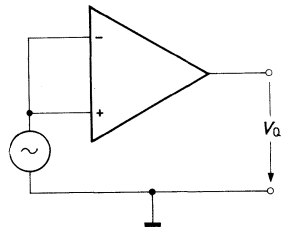


Figure 4



Definitions of the most important terms generally used to characterize an operational amplifier, are listed below. All definitions refer to symmetrical supply voltages.

a) Input offset voltage V_{IO} is that voltage difference which must be applied to the input terminals to achieve an output voltage of 0 V **(Figure 2)**.
$V_{IO} = V_{I1} - V_{I2}$ at $V_Q = 0$ and generator resistance $R_G = 50\ \Omega$.

b) Input current I_I is the average static input current required for op amp operation **(Figure 2)**.

$$I_I = \frac{I_{I1} + I_{I2}}{2}$$

c) Input offset current I_{IO} is the difference between the input currents in the operating range. At high values of generator resistance, I_{IO} may cause difficulties **(Figure 2)**.

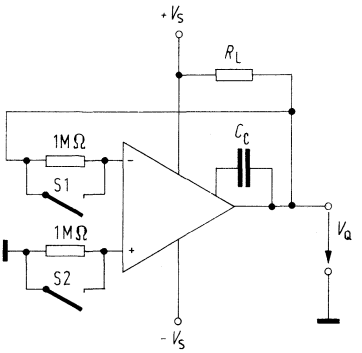
d) Open-loop voltage gain G_{V0} is the amplification without feedback **(Figure 3)**.

$$G_{V0} = \frac{V_Q}{V_I}$$

e) Common-mode voltage gain G_{VC} is the amplification of an in-phase signal applied to both inputs **(Figure 4)**.

Test Circuits for Operational Amplifiers

Input Current, Input Offset Current

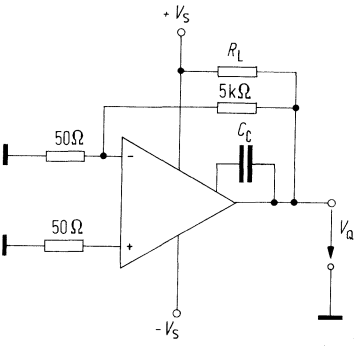


S 1 open – S 2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S 2 open – S 1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$;

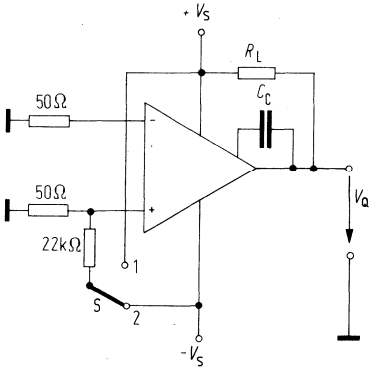
S 1 + S 2 open: I_{IO} approx. $\frac{V_Q}{1\,M\Omega}$

Input Offset Voltage



$-V_{IO} = V_{QO}/G_{VO}$; $G_{VO} = 100$; $-V_{IO} = \frac{V_{QO}}{100}$

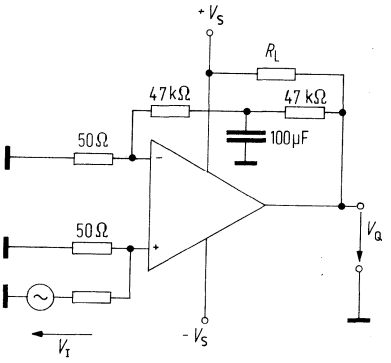
Output Voltage, Control Range



S in position 1: $V_Q = V_{QL}$;

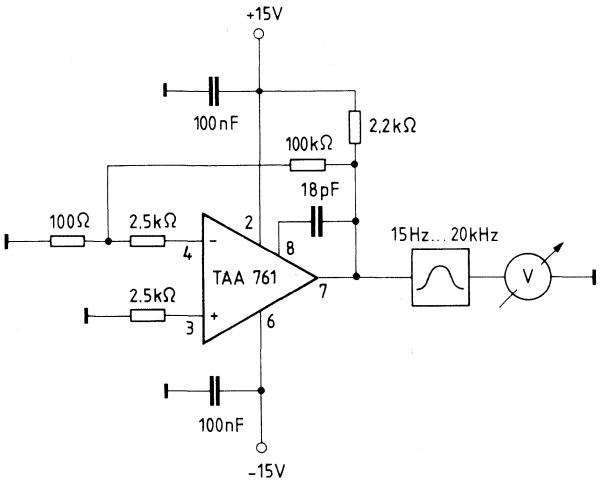
S in position 2: $V_Q = V_{QO}$

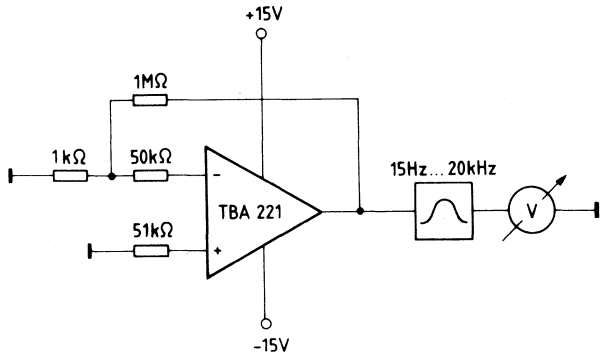
Open-Loop Voltage Gain at $f = 1$ kHz



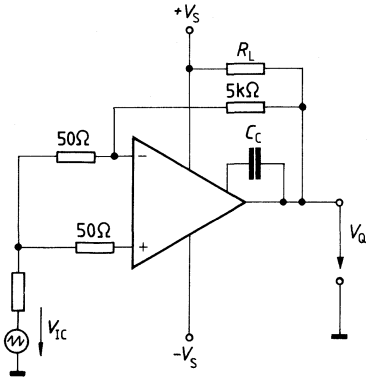
$G_{VO} = 20 \log \frac{V_Q}{V_I}$ [dB]

Noise Voltage in Accordance with DIN 45405; Psophometer U 2033 (from Siemens
Position: noise voltage; evaluation peak/zero



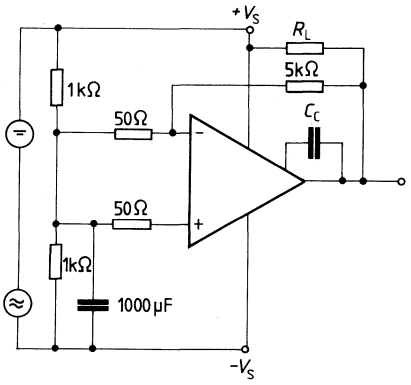


Common-Mode Rejection



$$G_{VC} = \frac{\Delta V_Q}{\Delta V_{IC}};\ k_{CMR} = 20 \log \frac{G_{V0}}{G_{VC}}\ [\text{dB}]$$

Supply Voltage Rejection



$$\frac{\Delta V_{IO}}{\Delta V_S} = \frac{\Delta V_Q}{100 \times \Delta V_S}$$

Relations between Slew Rate *SR* and Cutoff Frequency for High-Signal Output Voltage Swing (Power Bandwidth f_p)

The slew rate of an operational amplifier is determined by the charge/discharge of capacitors. For a capacitor the charge is $Q = C \cdot V$ or $Q = I \cdot dt$.

The voltage of capacitors changes as: $dv/dt \approx \Delta V/\Delta t = I/C$.

For the given current, faster charging or discharging of capacitors is not possible. This maximum speed of the voltage change is indicated for op amps by the factor *SR* (so-called slew rate) which is given in V/µs. Usual values are of the order of 3.0 to 20 V/µs.

The maximum frequency of a sinewave signal that is amplified without distortion is determined by the steepness of the sinewave signal at the zero crossover ($t = 0$). The sinewave signal of amplitude V_{QS} and angular frequency ω ($= 2\pi f$) has a steepness that is described by the first derivative of this function:

signal:	$V_q = V_{QS} \cdot \sin(\omega t)$
1st derivative:	$dvq/dt = V_{QS} \cdot \omega \cdot \cos(\omega t)$
for $t = 0$:	$\cos(\omega t) = 1$
thus:	$dvq/dt_{max} = V_{QS} \cdot \omega \cdot 1 = V_{QS} \cdot 2\pi f$

This value must be less than or equal to the slew rate of the op amp for a distortion-free output signal.

$$SR \geq V_{QS} \cdot 2\pi f$$

Therefore: $$f_p = \frac{SR}{2 \cdot \pi \cdot V_{QS}} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot V_{Qrms}} \qquad V_{Qrms} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot f_p}$$

Example 1: $SR = 0.5\ V/\mu s$ (corresponding to 500 000 V/s); $V_{Qrms} = 10\ V$

$$f_p = \frac{500\,000}{2 \cdot \pi \cdot \sqrt{2} \cdot 10} = 5.62\ kHz$$

If a signal of 10 kHz is to be transmitted, this is possible without distortion up to an rms voltage of 5.62 V.

Example 2: $SR = 10\ V/\mu s$; $V_{Qrms} = 10\ V$; $f_p = 112\ kHz$

The bandwidth cannot of course be infinite (as is possible in the equation). Additionally, there is a limitation due to the small-signal cutoff frequency (f_T).

Instructions for the Use of Integrated Operational Amplifiers

Preventive measures are implemented in most operational amplifiers, to reduce the risk of interference and failure.

Malfunctions or failure may however arise if several limiting conditions are simultaneously reached (e.g. max. output current, max. T_A, short circuits etc.)

This is also the case if the outputs are subject to high inductive and capacitive loads since inductive loads, flyback voltages and capacitive loads >1 nF generate extreme current surges.

High capacitive loads (≥100 pF) may lead to stability problems in op amps with high slew rates and high output currents (e.g. TAE 2453/TAE 4453).

There are two known remedies for this;

- Limitation of the output current surges **(figure 1, 3, 4)**
- Stronger or additional frequency compensation **(figure 2)**

Not driving the output hard into saturation i.e. setting the quiescent point in the middle of the control range, when the analogous output signal is smaller than the possible control range will also simplify this problem.

The minimum value for frequency compensation capacitance is given in the data book as follows:

Generator resistances	> 10 kΩ
Stray capacitances	< 5 pF at the summing point
Loads	< 100 pF

In other cases it may be necessary to use a stronger frequency compensation and/or a forward compensation from the input to the output (see TAA 762, test circuit 2 and **figure 1**).

For precision applications or open-loop operations, we recommend that both inputs on the PC board be protected by a guard ring and that the leads running to the inputs be manufactured with a shielded litz wire.

Shields of this kind are also recommended for applications with low input currents (or extremely high feedback resistance).

They prevent parasitic currents from occurring on the PC board – a phenomenon which might arise owing to soiled surfaces, for example.

Slew Rate and Power Bandwidth

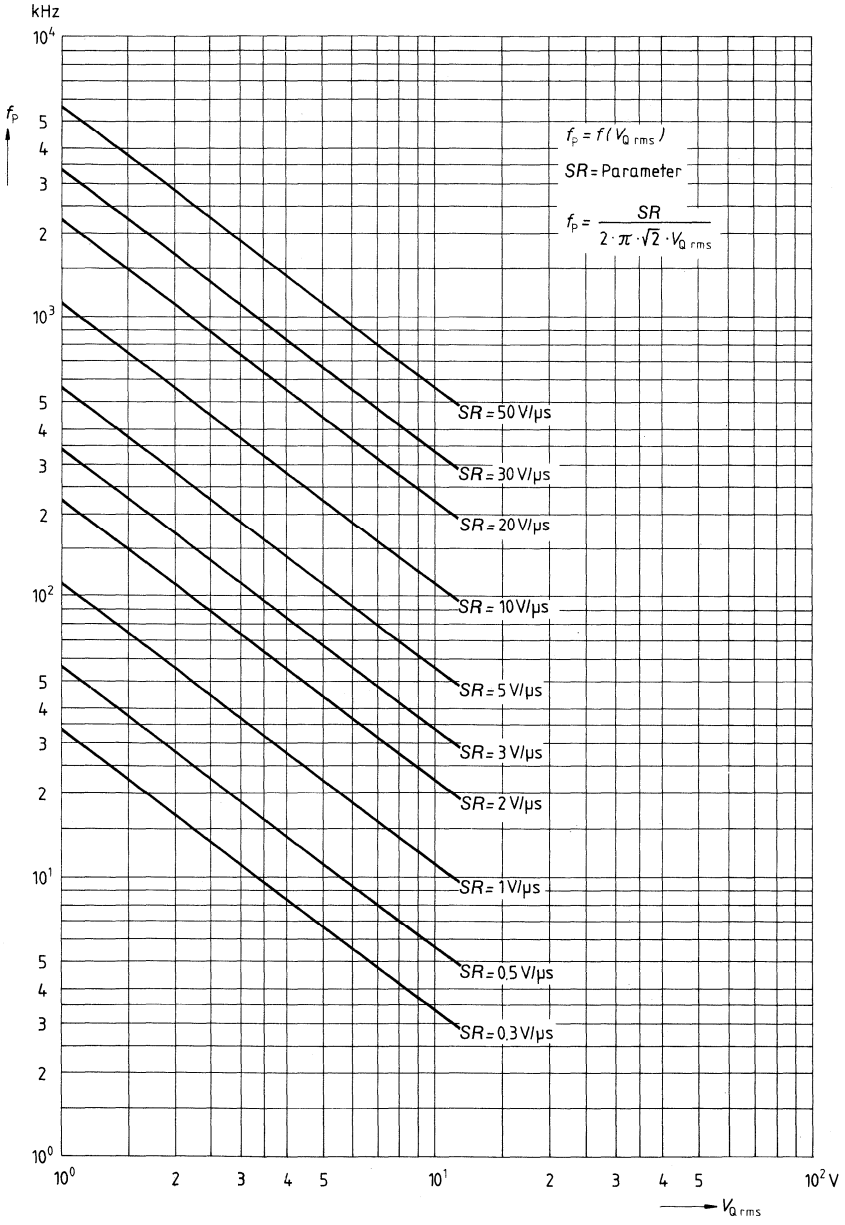


Figure 1

Improving the stability at high capacitive loads ≥ 100 pF by limiting the surge currents with *R*

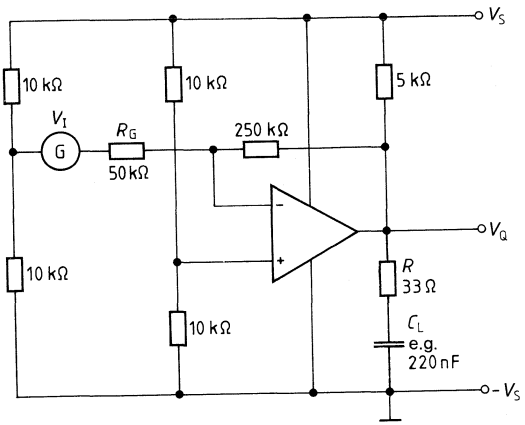


Figure 2

Compensation by means of approx. 220 Ω and 10 nF at input when no compensation point in the op amp is available, e.g. with gain 1, integrators and high capacitive loads.

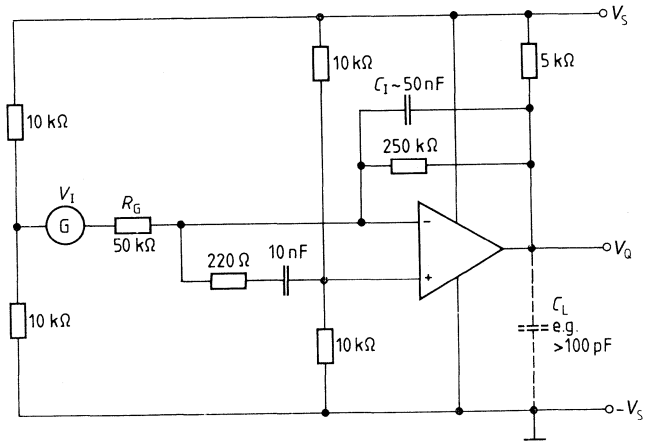
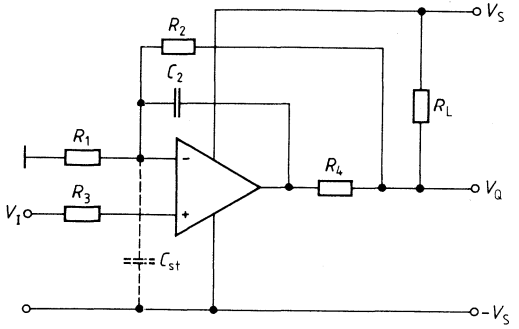


Figure 3

Protecting the inputs and outputs and compensation of the stray capacitance C_{st}



Gain

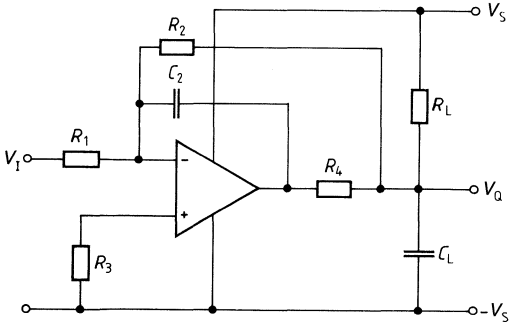
$$G = \frac{R_1 + R_2}{R_1}$$

Compensation

$$C_2 \approx \frac{R_1}{R_2} C_{st}$$

Figure 4

Wiring in the case of large capacitive loads



Gain

$$G = \frac{R_2}{R_1}$$

In figure 4 and 5:

R_3: Input protection

R_4: Output protection

R_L: Collector resistance (always required for op amps with open collector output).

Selector Guide

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C			Page
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA max.	Input offset voltage V_{IO} mV min./max.	Input current I_I µA typ.	Slew rate SR V/µs typ.	
Single Operational Amplifiers with NPN Input and Open Collector Output								
TAA 762 A	P-DIP-6	±1.5 to ±18	−55 to 125	70	±4	0.3	18	64
TAA 762 G	P-DSO-6	±1.5 to ±18	−55 to 125	70	±4	0.3	18	64
TAA 765 A	P-DIP-6	±1.5 to ±18	−25 to 85	70	±5.5	0.5	18	64
TAA 765 G	P-DSO-6	±1.5 to ±18	−25 to 85	70	±5.5	0.5	18	64
Dual Operational Amplifiers with NPN Input and Open Collector Output								
TAA 2762 A	P-DIP-8	±2 to ±15	−55 to 125	70	±4	0.3	0.5	98
TAA 2765 A	P-DIP-8	±2 to ±15	−25 to 85	70	±5.5	0.5	0.5	98
Quad Operational Amplifiers with NPN Input and Open Collector Output								
TAA 4762 A	P-DIP-14	±2 ro ±15	−55 to 125	70	±4	0.3	0.5	117
TAA 4765 A	P-DIP-14	±2 to ±15	−25 to 85	70	±5.5	0.5	0.5	117
Single Operational Amplifiers with Darlington Input and Open Collector Output								
TCA 332 A	P-DIP-6	±2 to ±15	−55 to 125	70	±10	5	9	75
TCA 332 G	P-DSO-6	±2 to ±15	−55 to 125	70	±10	5	9	75
TCA 335 A	P-DIP-6	±2 to ±15	−25 to 85	70	±15	5	9	75
TCA 335 G	P-DSO-6	±2 to ±15	−25 to 85	70	±15	5	9	75
Dual Operational Amplifiers with Darlington Input and Open Collector Output								
TBC 2332 B	P-DIP-8	±2 to ±15	−55 to 125	70	±10	5	0.5	102
TBE 2335 B	P-DIP-8	±2 to ±15	−25 to 85	70	±15	5	0.5	102
Quad Operational Amplifiers with Darlington Input and Open Collector Output								
TBC 4332 A	P-DIP-14	±2 to ±15	−55 to 125	70	±10	5	0.5	121
TBE 4335 A	P-DIP-14	±2 to ±15	−25 to 85	70	±15	5	0.5	121

= SMD (Surface Mounted Device)

Selector Guide (cont'd)

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C			Page
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA max.	Input offset voltage V_{IO} mV min./max.	Input current I_I µA typ.	Slew rate SR V/µs typ.	
Single Operational Amplifiers with NPN Input and Open Collector Output								
TAE 1453 A	P-DIP-6	±1.0 to ±18	−25 to 85	100	±5.5	0.04	20	82
TAE 1453 G	P-DSO-6	±1.0 to ±18	−25 to 85	100	±5.5	0.04	20	82
TAF 1453 A	P-DIP-6	±1.0 to ±18	−55 to 125	100	±4	0.04	20	82
TAF 1453 G	P-DSO-6	±1.0 to ±18	−55 to 125	100	±4	0.04	20	82
Dual Operational Amplifiers with PNP Input and Open Collector Output								
TAE 2453 A	P-DIP-8	±1.0 to ±18	−25 to 85	100	±5.5	0.04	1	107
TAE 2453 G	P-DSO-8	±1.0 to ±18	−25 to 85	100	±5.5	0.04	1	107
TAF 2453 A	P-DIP-8	±1.0 to ±18	−55 to 125	100	±4	0.04	1	107
TAF 2453 G	P-DSO-8	±1.0 to ±18	−55 to 125	100	±4	0.04	1	107
Quad Operational Amplifiers with PNP Input and Open Collector Output								
TAE 4453 A	P-DIP-14	±1.0 to ±18	−25 to 85	100	±5.5	0.04	1	126
TAE 4453 G	P-DSO-14	±1.0 to ±18	−25 to 85	100	±5.5	0.04	1	126
TAF 4453 A	P-DIP-14	±1.0 to ±18	−55 to 125	100	±4	0.04	1	126
TAF 4453 G	P-DSO-14	±1.0 to ±18	−55 to 125	100	±4	0.04	1	126
TAF 4463 A	P-DIP-14	±1.0 to ±18	−55 to 150	±50	±1	0.04	1	131
TAF 4463 G	P-DSO-14	±1.0 to ±18	−55 to 150	±50	±1	0.04	1	131
Single Operational Amplifiers with Push-Pull Output								
TBA 221 B	P-DIP-8	±4 to ±18	0 to 70	±20	±6	0.08	0.5	89
TBA 222 B	P-DIP-8	±4 to ±22	−55 to 125	±20	±4	0.08	0.5	89
TBA 222B/S1	P-DIP-8	±4 to ±22	−55 to 125	±20	±4	0.08	0.5	89
TBB 741 G	P-DSO-8	±4 to ±18	0 to 70	±20	±6	0.08	0.5	89
TBB 742 G	P-DSO-8	±4 to ±22	−55 to 125	±20	±4	0.08	0.5	89
Dual Operational Amplifiers with Push-Pull Output								
TBB 1458 B	P-DIP-8	±4 to ±18	0 to 70	±18	±6	0.08	0.5	112
TBB 1458 G	P-DSO-8	±4 to ±18	0 to 70	±18	±6	0.08	0.5	112

= SMD = Surface Mounted Device

SIEMENS

Single Operational Amplifiers

TAA 762
TAA 765

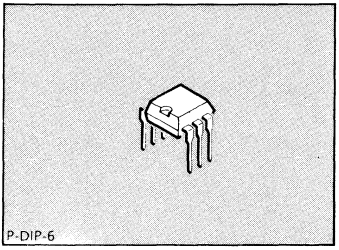
Bipolar IC

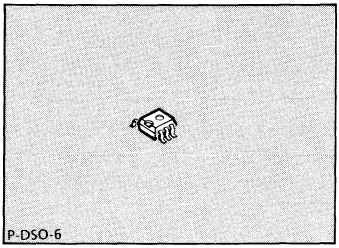
Features

- Wide common-mode range
- Large supply voltage range
- Large control range
- Wide temperature range (TAA 762)
- High output frequency compensation
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Driver



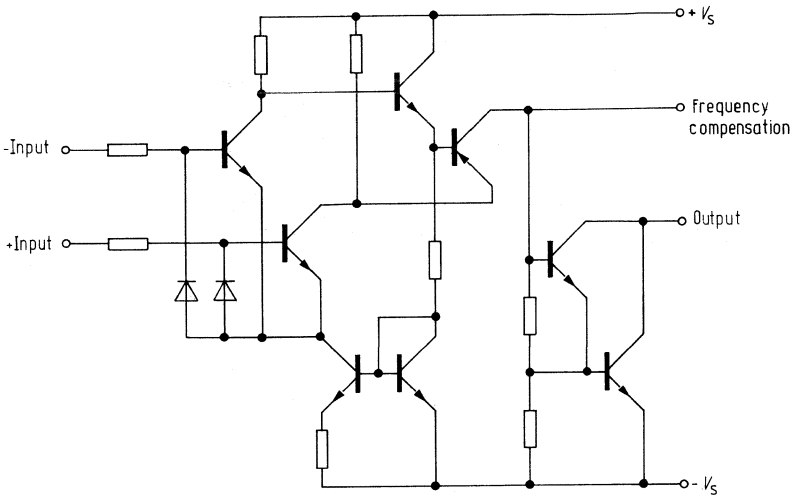


Type	Ordering Code	Package	Color Code
S TAA 762 A	Q67000-A2271	P-DIP-6	–
TAA 762 G	Q67000-A2273	P-DSO-6 (SMD)	white/yellow
S TAA 765 A	Q67000-A524	P-DIP-6	–
S TAA 765 G	Q67000-A599-G403	P-DSO-6 (SMD)	yellow/yellow

Particularly economic and versatile op amps. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

1

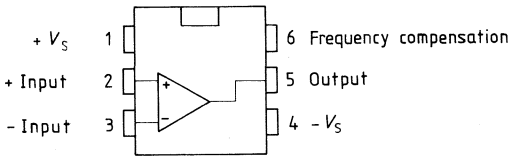
Circuit Diagram



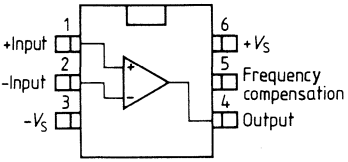
Pin Configurations

(top view)

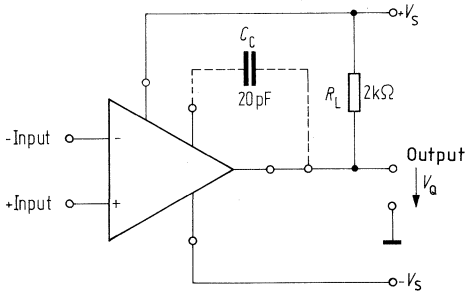
TAA 762 A
TAA 765 A



TAA 762 G
TAA 765 G



Connection Diagram



C_C = output frequency compensation;
R_L = load resistance (collector resistance)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAA 762 A	$R_{th\ SA}$	115	K/W
TAA 762 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	± 1.5 to ± 18	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	±50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V
$V_S = \pm 15$ V, $f = 100$ kHz	$U_{Q\ pp}$		±10				V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain							
$f = 1$ kHz	G_{V0}	85	87		80		dB
$R_L = 10$ kΩ, $f = 1$ kHz	G_{V0}		92				dB
$f = 1$ MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			1		5	µA

1

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_2-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_Q for non-inverting operation[1] (test circuit 1)	SR		9				V/µs
Slew rate of V_Q for inverting operation[1] (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ	V_n		3				µV

Characteristics

$V_S = \pm 2$ V; $R_L = 2$ kΩ

Input offset voltage $R_G = 50\ \Omega$)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0.2	0.5		0.8	µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	80			75		dB

[1] For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAA 765 A	$R_{th\ SA}$	115	K/W
TAA 765 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	± 1.5 to ± 18	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−200	± 80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V
$V_S = \pm 15$ V, $f = 100$ kHz	$U_{Q\ pp}$		± 10				V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain							
$f = 1$ kHz	G_{V0}	80	85		80		dB
$R_L = 10$ kΩ, $f = 1$ kHz	G_{V0}		90				dB
$f = 1$ MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			10		20	µA

1

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_Q for non-inverting operation[1] (test circuit 1)	SR		9				V/µs
Slew rate of V_Q for inverting operation[1] (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV

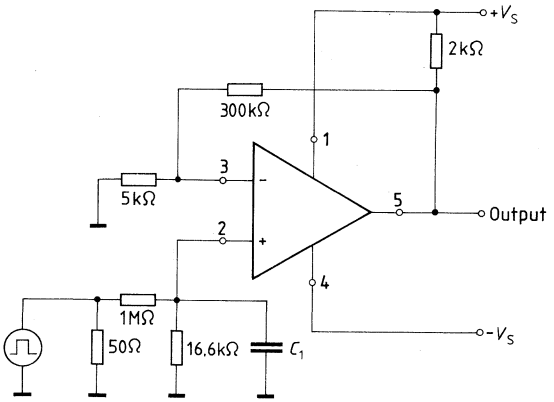
Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 30$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			75		dB

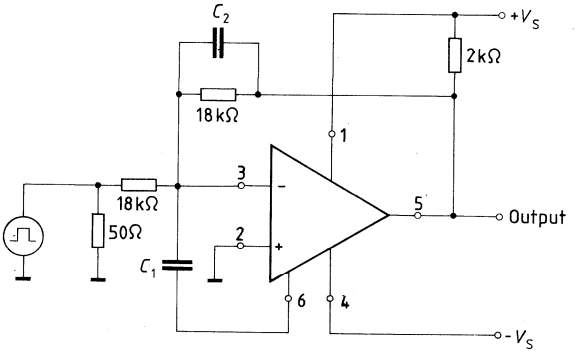
[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Test Circuit 1 for Slew Rate (non-inverting operation)



C_1 for min. overshoot (approx. 22 pF)

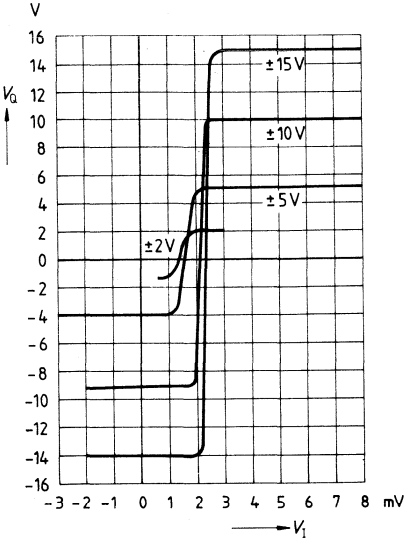
Test Circuit 2 for Slew Rate (inverting operation)



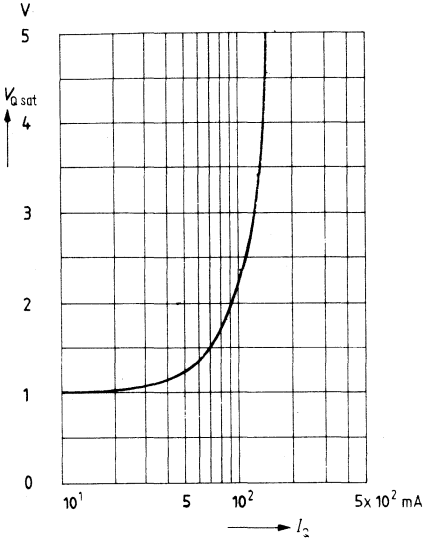
C_2 causes a frequency-dependent compensation to reduce rise times (approx. 390 pF)
C_1 for min. overshoot (approx. 3.9 pF)

1

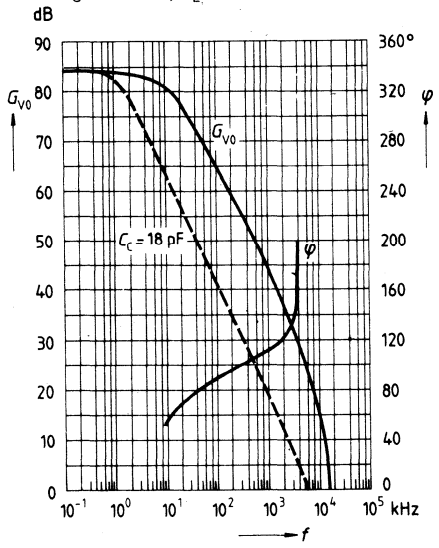
Transfer characteristic
Output voltage versus input voltage
V_S = parameter, $R_L = 2\ k\Omega$



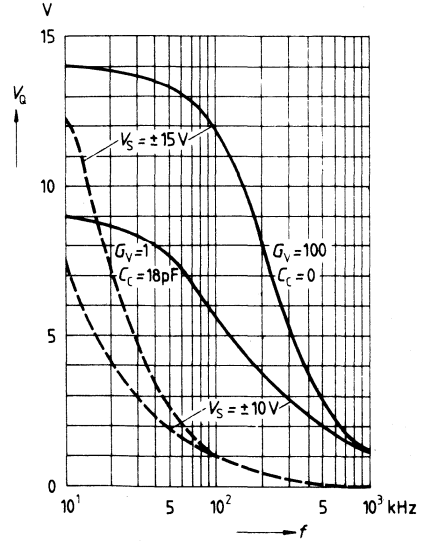
Saturation voltage versus output current
$T_A = 25\,°C$



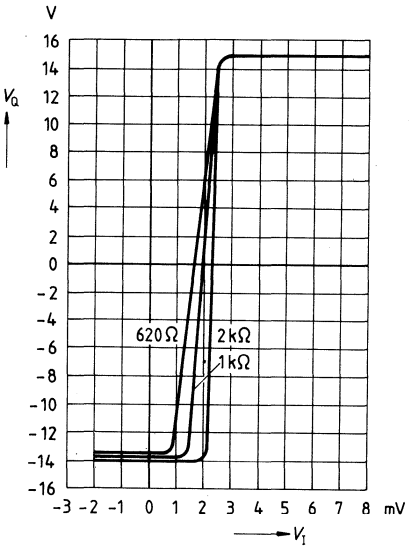
Open-loop voltage gain and phase versus frequency
$V_S = \pm 15\ V$; $R_L = 2\ k\Omega$



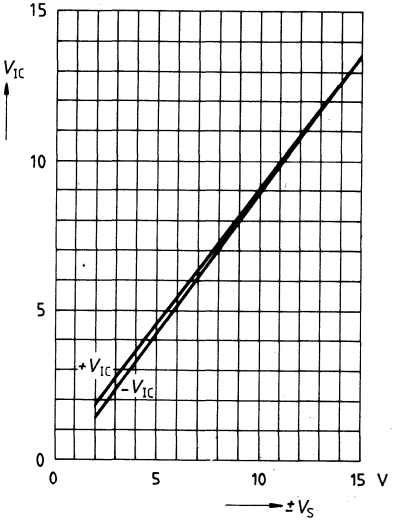
Frequency dependence of large signal modulation
Output voltage versus frequency



Transfer characteristic
Output voltage versus input voltage
$V_S = \pm$ 15 V; R_L = parameter

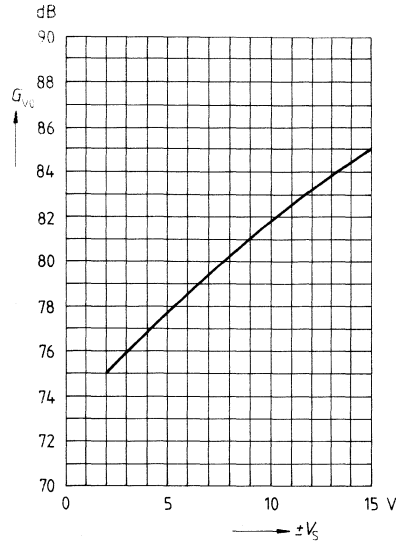


Common-mode voltage range
Common-mode input
voltage versus supply voltage

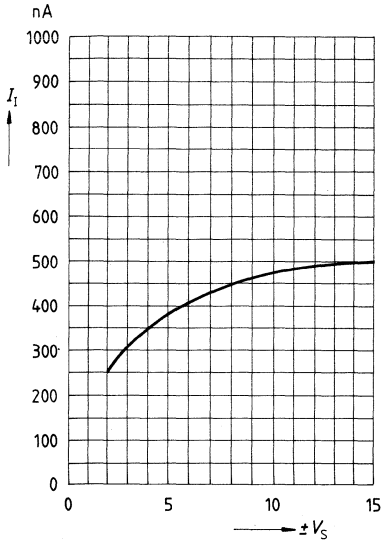


1

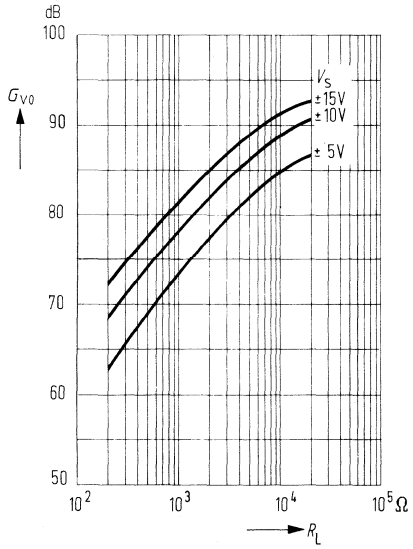
Open-loop voltage gain versus supply voltage
$T_A = 25\,°C$; $R_L = 2\,k\Omega$



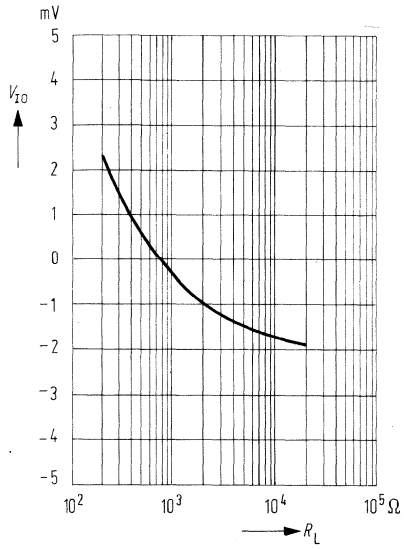
Input current versus supply voltage



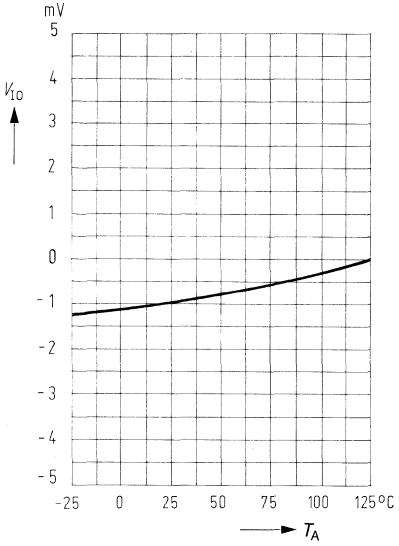
Open-loop voltage gain versus load resistance
$T_A = 25\,°C$



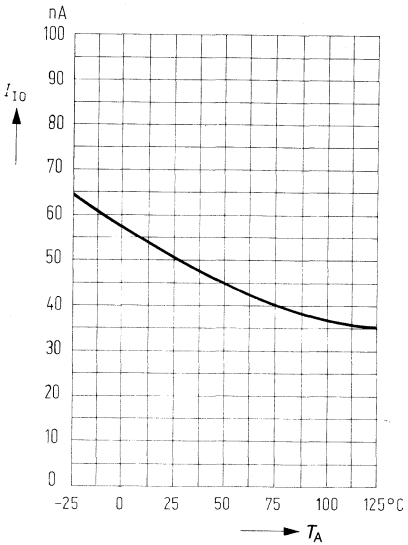
Input offset voltage versus load resistance
$V_S = \pm 15\,V$



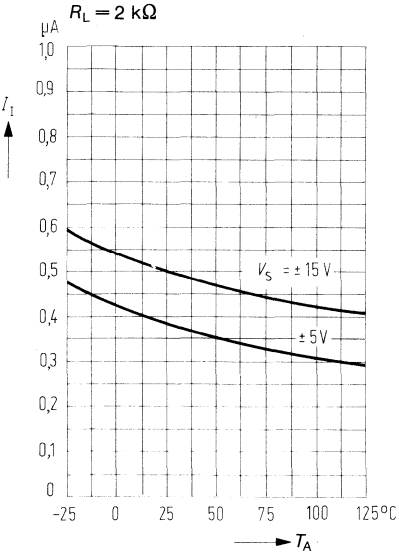
Input offset voltage versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



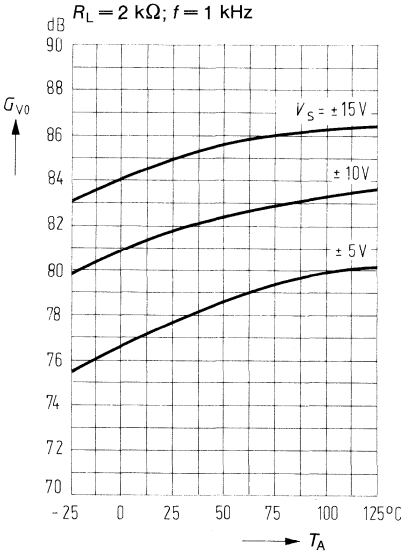
Input offset current versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



Input current versus ambient temperature
$R_L = 2\ k\Omega$



Open-loop voltage gain versus ambient temperature
$R_L = 2\ k\Omega$; $f = 1\ kHz$



SIEMENS

1

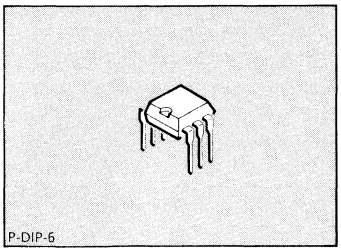
Single Operational Amplifier with Darlington Input

TCA 332
TCA 335

Bipolar IC

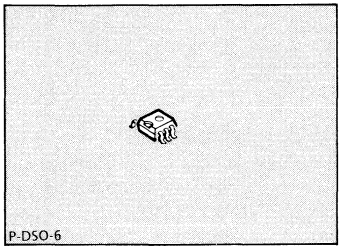
Features

- High input impedance
- Wide common-mode range
- Large supply-voltage range
- Large control range
- High output current
- Simple frequency compensation
- Wide temperature range (TCA 332)
- NPN Darlington input
- Open collector output



Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver



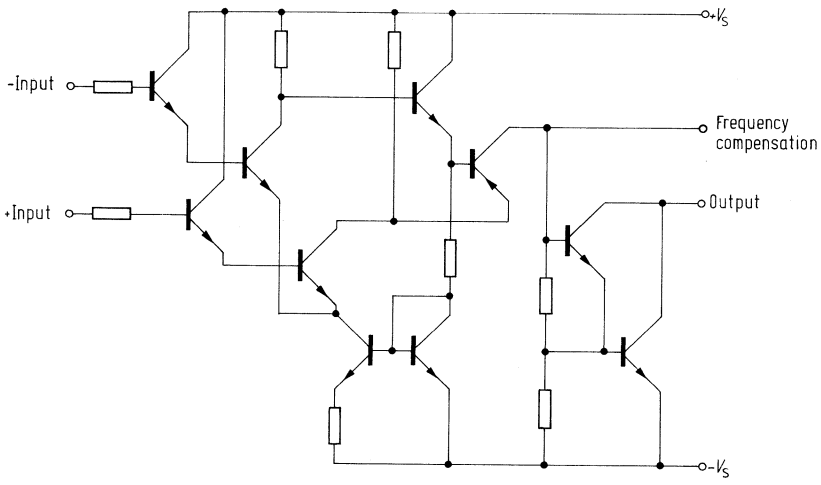
	Type	Ordering Code	Package	Color Code
■ S	TCA 332 A	Q67000-A2272	P-DIP-6	–
■	TCA 332 G	Q67000-A2270	P-DSO 6 (SMD)	orange/yellow
■ S	TCA 335 A	Q67000-A563	P-DIP-6	–
■ S	TCA 335 G	Q67000-A1018-G403	P-DSO-6	blue/yellow

■ = Not for new design

For TCA 315 and TCA 325 see **chapter "Comparators".**

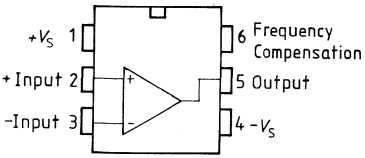
These op amps are particularly economic and versatile. Owing to their excellent performance characteristics they are well suited for a wide scope of applications, such as measuring and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in measuring and control systems.

Circuit Diagram

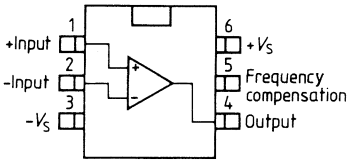


Pin Configurations
(top view)

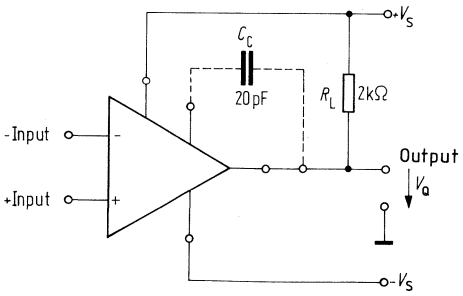
TCA 332 A
TCA 335 A



TCA 332 G
TCA 335 G



Connection Diagram



C_C = output frequency compensation
R_L = load resistance (collector resistance)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V Differential input voltage: V_S = 2 to 13 V	V_{ID} V_{ID}	± 13 ± V_S	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 332 A TCA 332 G	 $R_{th\,SA}$ $R_{th\,SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V
R_L = 2 kΩ, unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = −55 to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current Input current V_{ID} = ± 13 V	I_{IO} I_I I_I	−5	5	5 15 200	−10	10 25	nA nA nA
Control range V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V V_S = ± 15 V, f = 100 kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9	 ± 10	 −14.0 −12.5	 14.8 14.8	 −14.0 −12.0	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_I		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 83 88 43		 75		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50		50	μV/K pA/K
Slew rate of V_Q for non-inverting operation[1] (see TAA 765, test circuit 1) Slew rate of V_Q for inverting operation[1] (see TAA 765, test circuit 2)	SR SR		9 18				V/μs V/μs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Output reverse current	I_{QR}			1		5	μA

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V Differential input voltage: V_S = 2 to 13 V	V_{ID} V_{ID}	± 13 ± V_S	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 335 A TCA 335 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

V_S = ± 5 V to ± 15 V; R_L = 2 kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = −25 to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−15		15	−18	18	mV
Input offset current Input current Input current V_{ID} = ± 13 V	I_{IO} I_I I_I	−10	 5 	10 25 200	−20	20 35 	nA nA nA
Control range V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V V_S = ± 15 V, f = 100 kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9 	 ± 10	 −14.0 −12.5 	 14.8 14.8 	 −14.0 −12.0 	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_I		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 75	 80 85 43	 	 75	 	 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50		50	µV/K pA/K
Slew rate of V_Q for non-inverting operation[1]) (see TAA 765, test circuit 1) Slew rate of V_Q for inverting operation[1]) (see TAA 765, test circuit 2)	SR SR		9 18				V/µs V/µs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Output reverse current	I_{QR}			10		20	µA

Characteristics

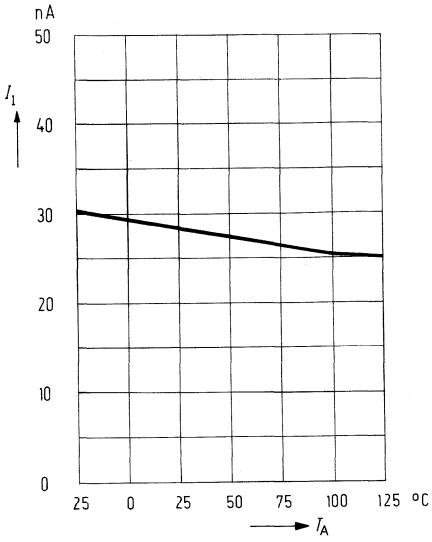
$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	70			70		dB

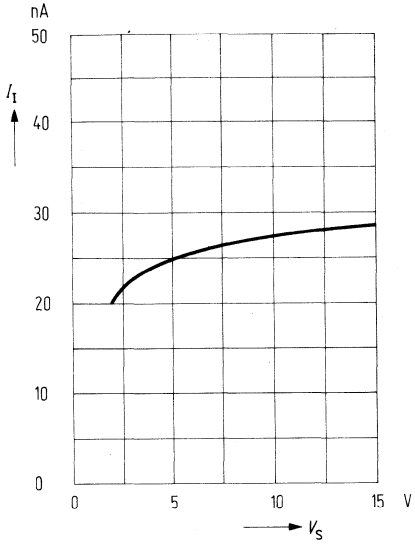
[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

1

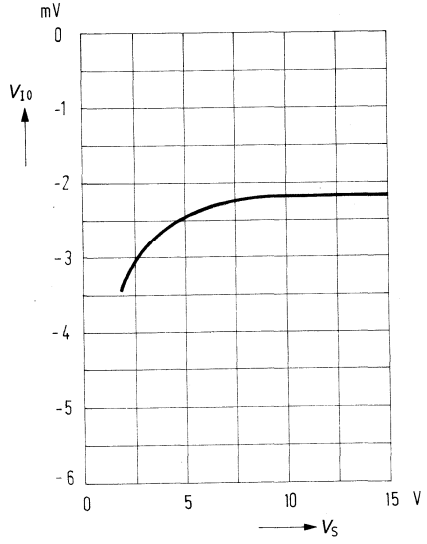
Input current versus ambient temperature
$R_L = 2\ k\Omega$



Input current versus supply voltage
$T_A = 25\,°C$; $R_L = 2\ k\Omega$



Input offset voltage versus supply voltage



SIEMENS

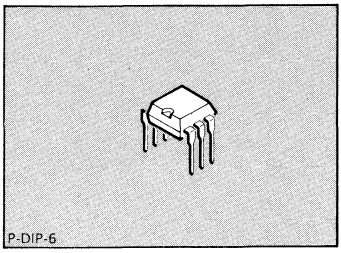
Single PNP Operational Amplifier

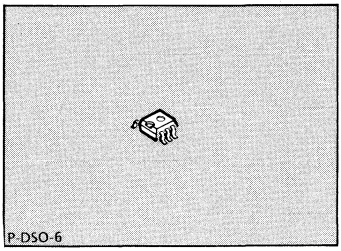
TAE 1453
TAF 1453

Bipolar IC

Features

- PNP input
- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.25 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Wide common-mode range
- Wide operating temperature range (TAF 1453)
- Pin-compatible to TAA 765
- Open collector output





Applications

- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

Type	Ordering Code	Package	Color Code
S TAE 1453 A	Q67000-A2017	P-DIP-6	–
S TAE 1453 G	Q67000-A2106	P-DSO-6 (SMD)	blue/white
S TAF 1453 A	Q67000-A2269	P-DIP-6	–
TAF 1453 G	Q67000-A2209	P-DSO-6 (SMD)	red/red

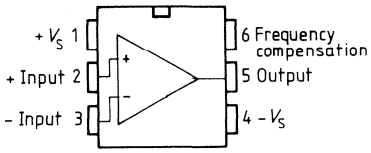
These operational amplifiers are circuits for universal applications having a PNP input differential stage and an open collector output. Apart from one resistor, only active components are used. The integrated regulator provides for all parameters a large degree of independence from the supply voltage.

1

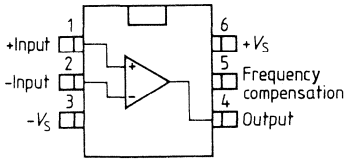
Pin Configurations

(top view)

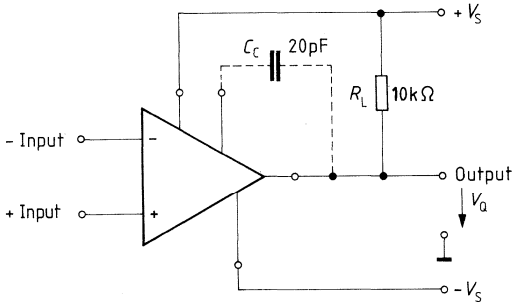
TAE 1453 A
TAF 1453 A



TAE 1453 G
TAF 1453 G



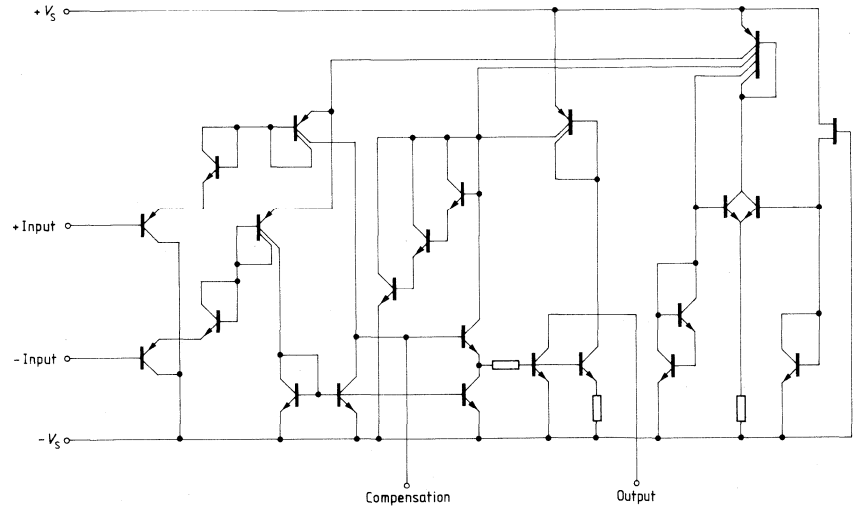
Connection Diagram



C_C = output frequency compensation (if required);

R_L = load resistance (collector resistance)

Circuit Diagram



Absolute Maximum Ratings (TAE 1453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance system – air TAE 1453 A	$R_{th\ SA}$	135	K/W
TAE 1453 G	$R_{th\ SA}$	200	K/W

Operating Range (TAE 1453)

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics (TAE 1453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop current consumption	I_S		0.25	0.4		0.45	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−15		15	−100	100	nA
Input current	I_I		40	150		200	nA
Control range							
$R_L = 2$ kΩ, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.7	14.9	−14.7	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.5	14.9	−14.4	V
$R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz	$V_{Q\ pp}$	10		−10			V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain	G_{V0}	78	85		78		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S$−0.2		V_S−1.8	$-V_S$	V_S−2.0	V
Common-mode rejection	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		120	µV/V

1

Characteristics (TAE 1453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		6				µV/K
Slew rate for non-inverting operation[1])	SR		20				V/µs
Slew rate for inverting operation[1])	SR		30				V/µs

Characteristics (TAE 1453)

$V_S = \pm 2$ V, $R_L = 10$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−15		15	−100	100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain	G_{VO}	70			70		dB

Absolute Maximum Ratings (TAF 1453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAF 1453 A	$R_{th\ SA}$	135	K/W
TAF 1453 G	$R_{th\ SA}$	200	K/W

Operating Range (TAF 1453)

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 with slightly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Characteristics (TAF 1453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop current consumption (Output in H state)	I_S		0.25	0.35		0.45	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset voltage	I_{IO}	−10		10	−75	75	nA
Input current	I_I		40	100		150	nA
Control range							
$R_L = 2$ kΩ, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−14.7	14.9	−14.7	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−14.5	14.9	−14.4	V
$R_L = 2$ kΩ, $V_S = 15$ V, $f = 100$ kHz	$V_{Q\,pp}$	10		−10			V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S$−0.3		V_S−1.5	$-V_S$	V_S−1.8	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.1	0.8			nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6	25			µV/K
Slew rate for non-inverting operation[1]	SR		20				V/µs
Slew rate for inverting operation[1]	SR		30				V/µs

Characteristics (TAF 1453)

$V_S = \pm 2$ V, $R_I = 10$ kΩ

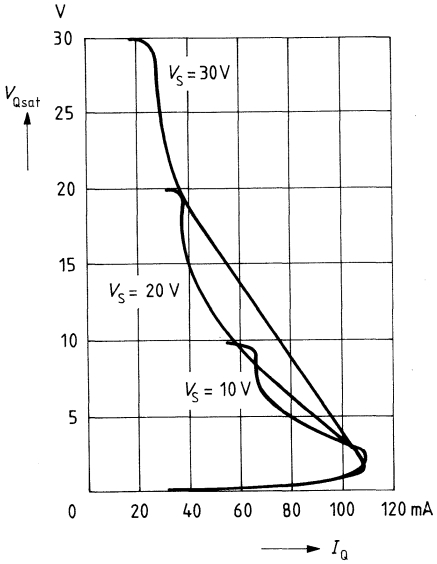
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−10		50	10	75	nA
Input current	I_I		40	100		150	nA
Open-loop voltage gain	G_{V0}	75			70		dB

[1] For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

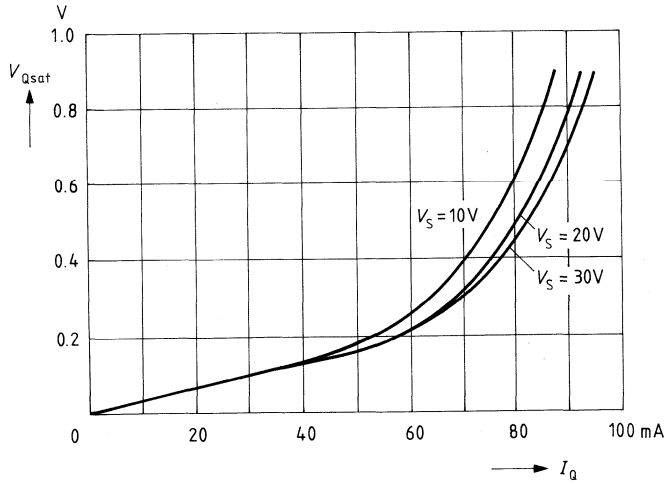
1

Typical Characteristics of Electrical Parameters

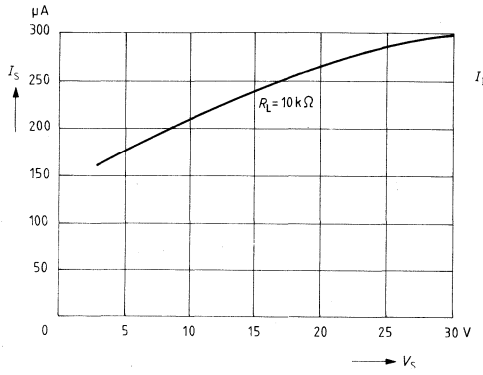
Load characteristics
Output saturation voltage versus output current



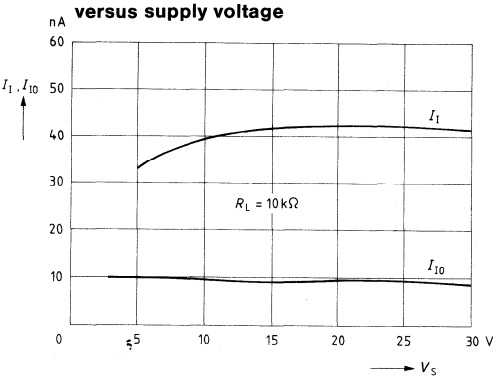
Output saturation voltage versus output current



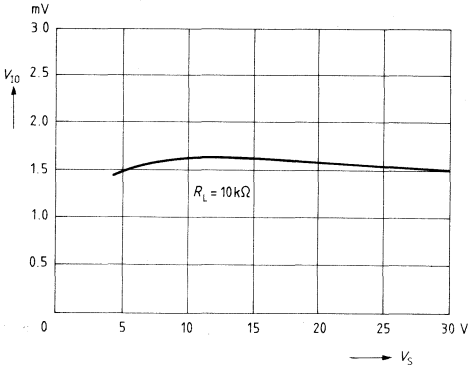
Supply current versus supply voltage



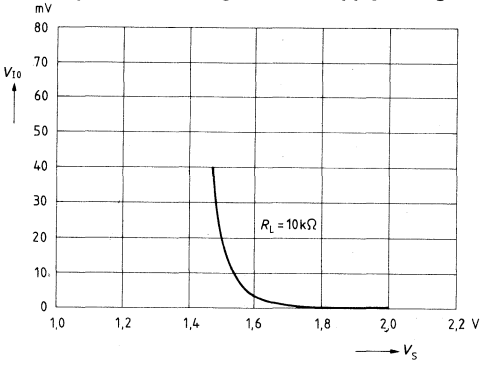
Input current and input offset current versus supply voltage



Input offset voltage versus supply voltage



V_{IO} behavior at low operating voltages
Input offset voltage versus supply voltage



Single Operational Amplifiers

TBA 221; TBB 741
TBA 222; TBB 742

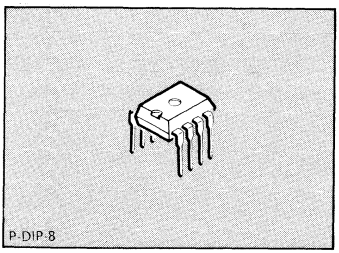
Bipolar IC

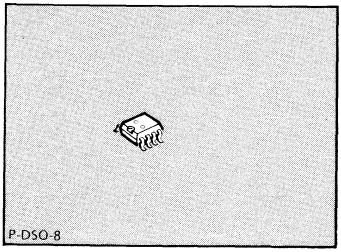
Features

- NPN input
- High differential input voltage
- Short-circuit proof
- High voltage gain
- High supply voltage 44 V
- Wide temperature range (TBA 222, TBB 742)
- Push-pull output
- B S1-version for high quality

Applications

- Amplifier
- Comparator



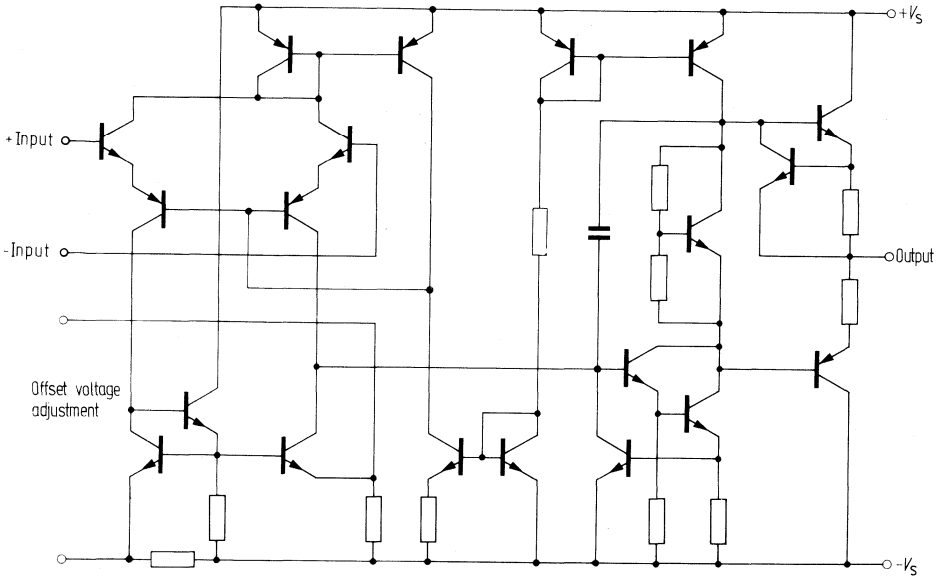


	Type	Ordering Code	Package	Color Code
S	TBA 221 B	Q67000-A281	P-DIP-8	–
S	TBA 222 B	Q67000-A2280	P-DIP-8	–
	TBA 222 B S1	Q67000-A8057	P-DIP-8	–
■ S	TBB 741 G	Q67000-A1498	P-DSO-8 (SMD)	blue/brown
■ S	TBB 742 G	Q67000-A2395-G403	P-DSO-8 (SMD)	red/green

■ = Not for new design

These op amps are short-circuit proof to $+V_S$, $-V_S$. The input offset voltage can be very easily compensated. Very few external components are required due to the internal frequency compensation. The gain reduction by 6 dB/octave yields a very good stability.

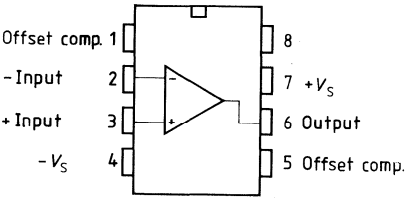
Circuit Diagram



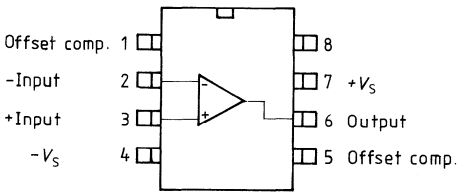
Pin Configurations

(top view)

TBA 221 B
TBA 222 B
TBA 222 B S1



TBB 741 G
TBB 742 G



Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		TBA 221 TBB 741	TBA 222 TBB 742	
Supply voltage	V_S	±18	±22	V
Input voltage: $V_S = \pm 4$ to ± 15 V $V_S \geq 15$ V	V_I V_I	$\pm V_S$ ±15	$\pm V_S$ ±15	V V
Differential input voltage	V_{ID}	±30	±30	V
Output short-circuit duration[1])	t_{QSC}	∞	∞	
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	150 −65 to 125	°C °C
Thermal resistance system – air TBA 221B/222B; BS1 TBB 741 G/742 G	 $R_{th\ SA}$ $R_{th\ SA}$	 100 200	 100 200	 K/W K/W

[1]) Short circuit may be to $+V_S$, $-V_S$, or 0, whereby maximum ratings like T_j must not be exceeded.

Operating Range

Supply voltage	V_S	±4 to ±18	±4 to ±22	V
Ambient temperature	T_A	0 to 70	−55 to 125	°C

Characteristics

$V_S = \pm 15$ V

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = 0$ °C to 70 °C		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−6		6	−7.5	7.5	mV
Setting range of V_{IO}	V_{IO}	6	±15	−6			mV
Input offset current	I_{IO}	−200	±20	200	−300	300	nA
Input current	I_I		80	500		800	nA
Supply current	I_S		1.7	2.8		2.8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1.4				pF
Output resistance	R_Q		75				Ω
Control range $R_G \geq 10$ kΩ $R_L \geq 2$ kΩ	 $V_{Q\ pp}$ $V_{Q\ pp}$	 13 11	 ±14 ±13	 −12.5 −11			 V V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V

Characteristics

$V_S = \pm 15$ V

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = 0$ °C to 70 °C min.	max.	Unit
Open-loop voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L \geq 2$ kΩ	G_{V0}	86	100		84		dB
Common-mode rejection ($R_G \leq 10$ kΩ)	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SVR}		30	150			μV/V
Transient response of output voltage at $G_V = 1$: Rise time, $V_I = 20$ mV, $R_L = 2$ kΩ; $C_L \leq 100$ pF	t_r		0.3				μs
Overshoot			5				%
Slew rate[1] $R_L \leq 2$ kΩ	SR		0.5				V/μs
Temperature coefficient of V_{IO} Temperature coefficient of I_{IO}	α_{VIO} α_{IIO}		3 0.4				μV/K nA/K

Characteristics (TBA 222, TBB 742)

$V_S = \pm 15$ V

Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−4		4	−5.5	5.5	mV
Setting range of V_{IO}	V_{IO}	6	±15	−6			mV
Input offset current	I_{IO}	−100	±20	100	−400	400	nA
Input current	I_I		80	350		1200	nA
Supply current	I_S		1.7	2.8		2.8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC-}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1.4				pF
Output resistance	R_Q		75				Ω
Control range $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	 $V_{Q\,pp}$ $V_{Q\,pp}$	 13 11	 ±14 ±13	 −12.5 −11			 V V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V
Open-loop voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L \geq 2$ kΩ	G_{V0}	94	106		88		dB
Common-mode rejection $R_G \leq 10$ kΩ	k_{CMR}	80	90				dB
Supply voltage rejection	k_{SVR}		30	100			μV/V

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction – Operational Amplifiers"**

Characteristics (TBA 222, TBA 742)

$V_S = \pm 15$ V

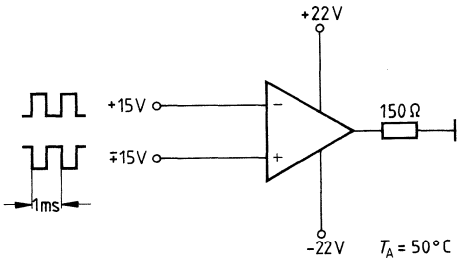
Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = 0$ °C to 70 °C min.	max.	Unit
Transient response of output voltage at $G_V = 1$: Rise time, $V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF	t_r		0.3				µs
Overshoot			5				%
Slew rate[1] $R_L \leq 2$ kΩ	SR		0.5				V/µs
Temperature coefficient of V_{IO}	α_{VIO}		3				µV/K
Temperature coefficient of I_{IO}	α_{IIO}		0.4				nA/K

TBA 222 B S1

The TBA 222 B S1 is similar to TBA 222 B, however, with special quality features.

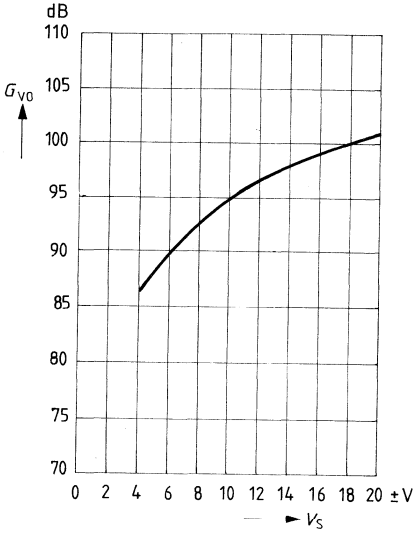
1. 72 hours electrically preaged at $T_A = 50$ °C, $V_S \pm 22$ V corresponding to the circuit shown below
2. Noise < 5 µVs in accordance with DIN 45405

Circuit, Preageing for TBA 222 B S1



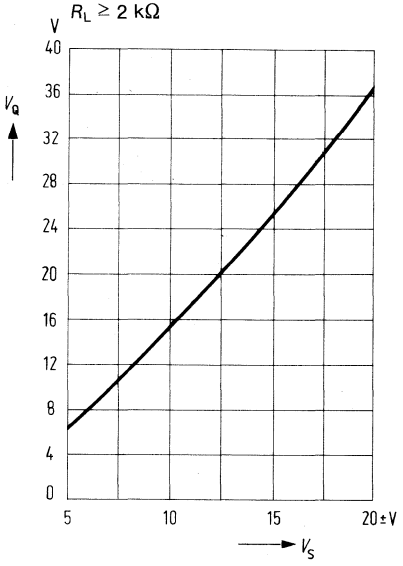
[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction – Operational Amplifier"**

Open-loop voltage gain versus supply voltage



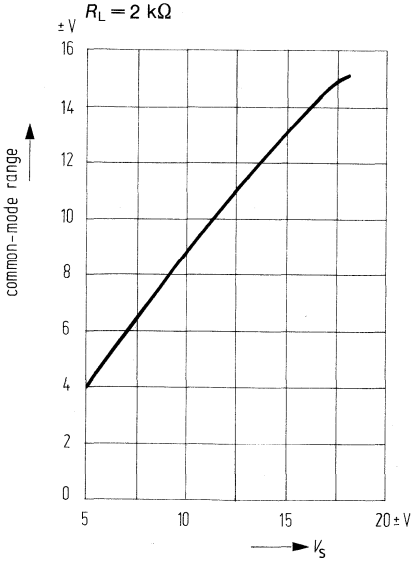
Output voltage versus supply voltage

$R_L \geq 2$ kΩ

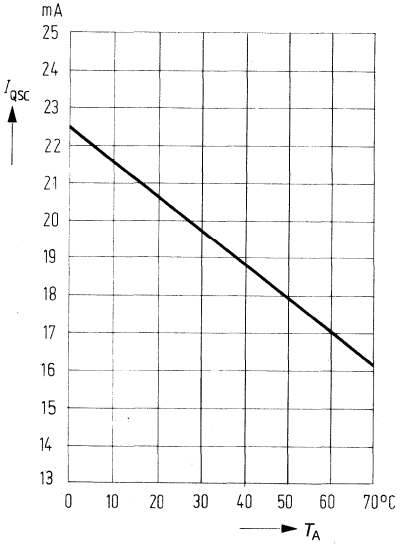


Common-mode range versus supply voltage

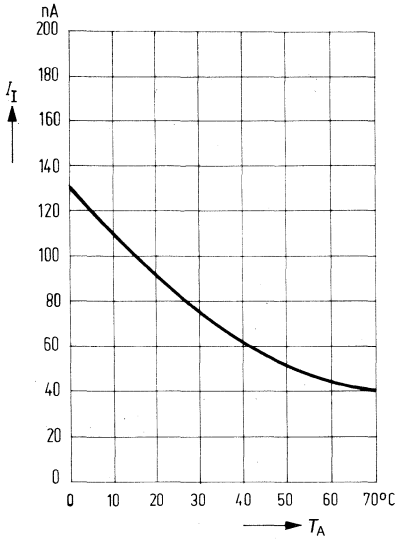
$R_L = 2$ kΩ



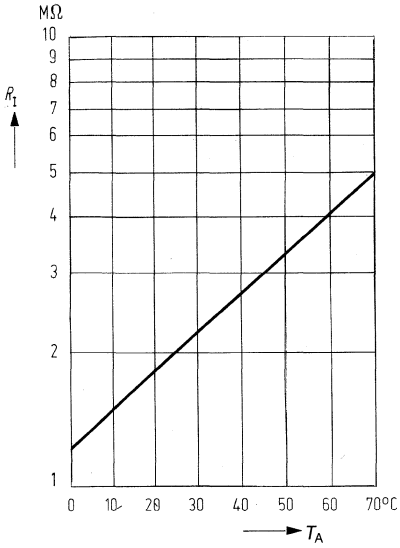
Output short-circuit current versus ambient temperature



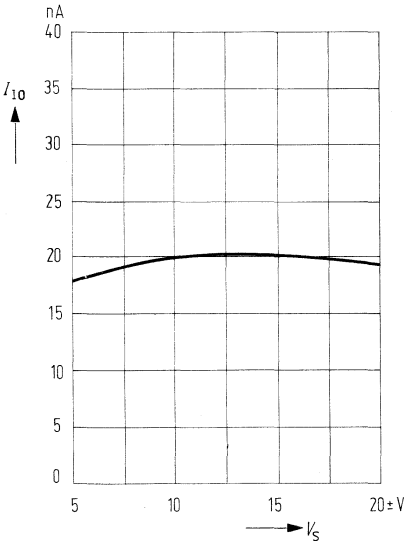
Input current versus ambient temperature
$V_S = \pm 15$ V



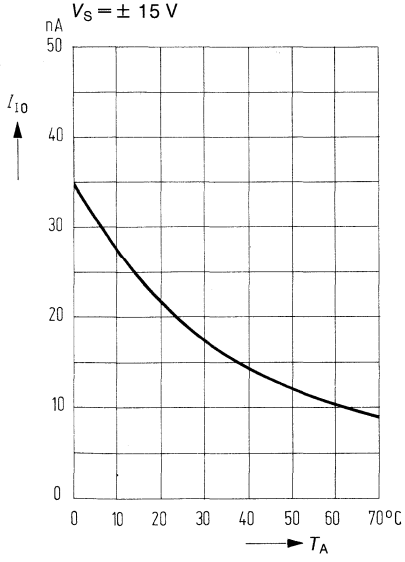
Input resistance versus ambient temperature
$V_S = \pm 15$ V



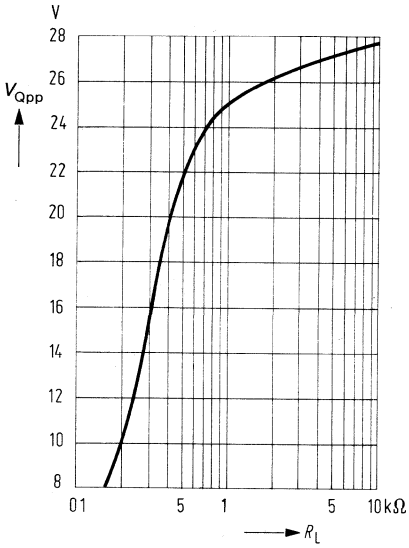
Input offset current versus supply voltage



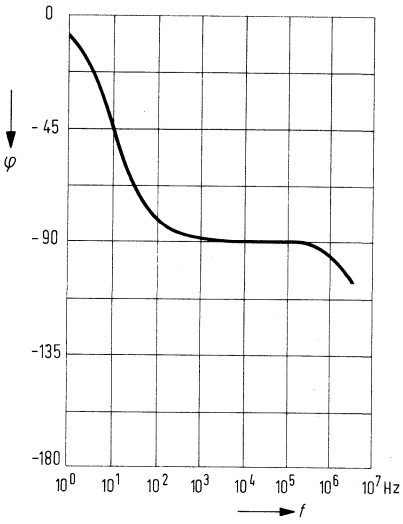
Input offset current versus ambient temperature
$V_S = \pm 15$ V



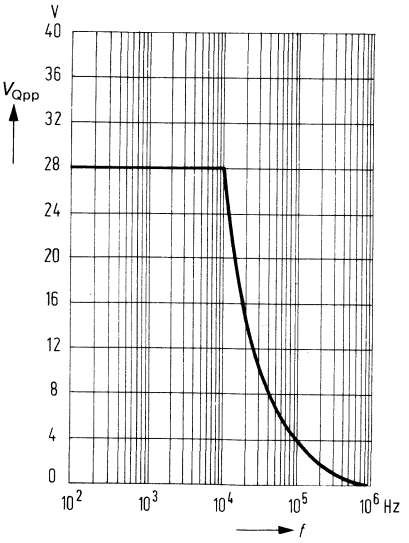
Output voltage versus load resistance
$V_S = \pm 15$ V



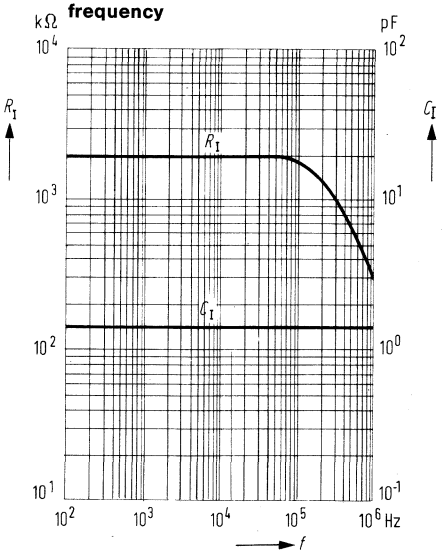
Phase response of open-loop voltage gain
Phase versus frequency
$V_S = \pm 15$ V



Output voltage versus frequency
$V_S = \pm 15$ V; $R_L = 10$ kΩ

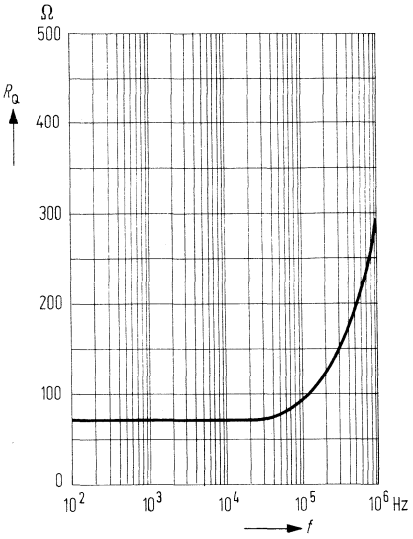


Input resistance and input capacitance versus frequency

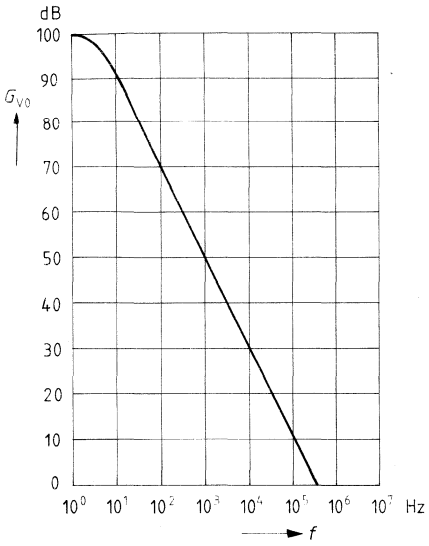


1

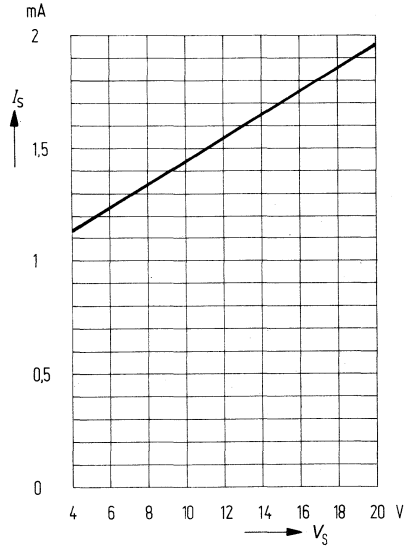
Output resistance versus frequency



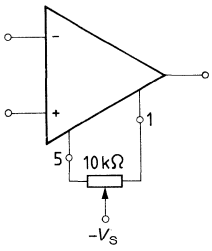
Open-loop voltage gain versus frequency



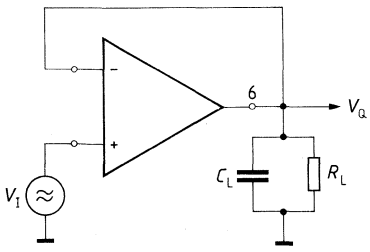
Supply current versus supply voltage



Offset voltage adjustment circuit



Transient response



SIEMENS

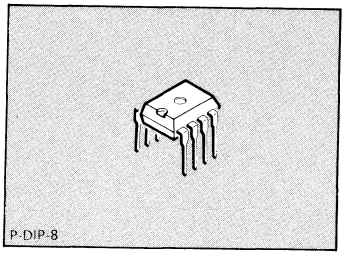
Dual Operational Amplifier

TAA 2762
TAA 2765

Bipolar IC

Features

- Wide common-mode range
- Large supply voltage range
- Wide temperature range (TAA 2762 A)
- High output current
- Large control range
- Internally frequency-compensated
- NPN input with protection diodes
- Open collector output

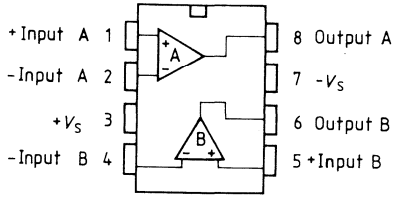


Applications

- Amplifier
- Comparator
- Level converter
- Driver

Pin Configuration

(top view)

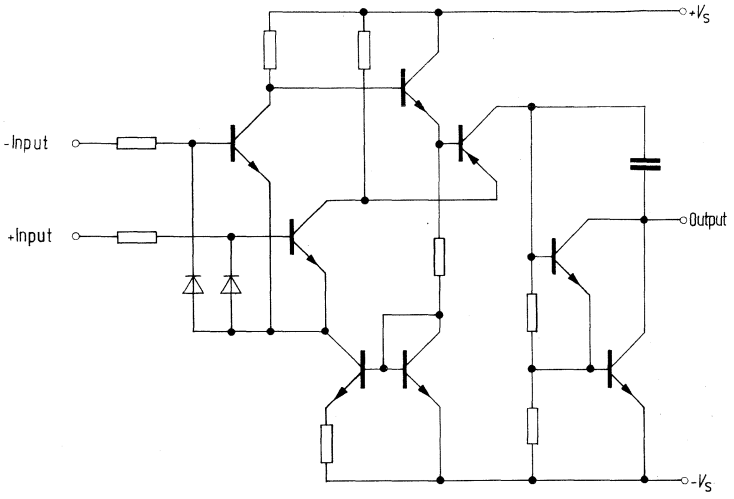


Type	Ordering Code	Package
S TAA 2762 A	Q67000-A2499	P-DIP-8
S TAA 2765 A	Q67000-A1031	P-DIP-8

These op amps are particularly economic and versatile. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

1

Circuit Diagram of one Op Amp



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	± V_S	
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TAA 2762 A/2765 A	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage		V_S	± 2 to ± 15	V
Ambient temperature	TAA 2762 A TAA 2765 A	T_A T_A	−55 to 125 −25 to 85	°C °C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−100	±50 0.3	100 0.7	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 100$ kHz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 85	 87 92		 80		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85			75	dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15 1.5		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	80			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Open-loop supply currrent consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	±80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 85 90		 80		 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45 405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1]) Slew-rate for inverting operation[1])	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

SIEMENS

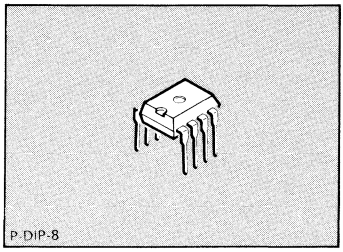
Dual Operational Amplifier with Darlington Input

TBC 2332
TBE 2335

Bipolar IC

Features

- High input impedance
- Wide common-mode range
- Large supply voltage range
- Large control range
- Wide temperature range (TBC 2332 B)
- Open collector output
- NPN Darlington input
- Low input current
- Internally frequency-compensated

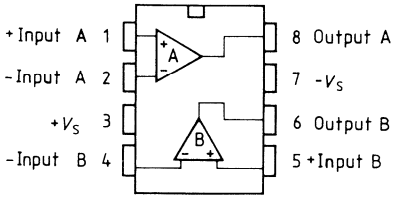


Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver

Pin Configuration

(top view)

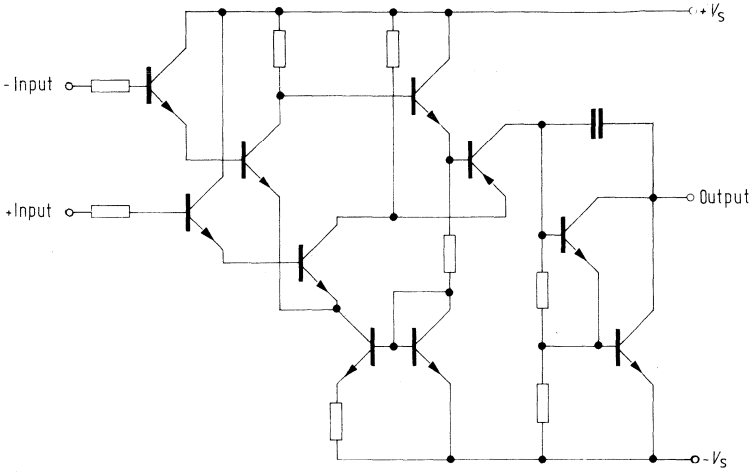


Type	Ordering Code	Package
S TBC 2332 B	Q67000-A2500	P-DIP-8
S TBE 2335 B	Q67000-A1165	P-DIP-8

These op amps are economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in measurement and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for measurement and control systems.

1

Circuit Diagram of one Op Amp



Absolute Maximum Ratings (TBC 2332)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage $V_S = \pm 13$ to ± 15 V $V_S = \pm 2$ to ± 13 V	 V_{ID} V_{ID}	 ±13 $\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range (TBC 2332)

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics (TBC 2332)

$V_S = \pm 5$ V to ± 15 V

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Control range							
$R_L = 2$ kΩ, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−14	14.8	−14	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−12.5	14.8	−12	V

Characteristics (TBC 2332)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain							
$f = 100$ Hz	G_{V0}	80	83		75		dB
$R_L = 10$ kΩ, $f = 100$ Hz	G_{V0}		88				dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	V_S		$-V_S+2.0$	V_S	$-V_S+3$	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		4	25		50	µV/K
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		50				pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1])	SR		0.5				V/µs
Slew rate for inverting operation[1])	SR		0.5				V/µs

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

1

Absolute Maximum Ratings (TBE 2335)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage $V_S = \pm 13$ to ± 15 V $V_S = \pm$ 2 to ± 13 V	 V_{ID} V_{ID}	 ±13 $\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range (TBE 2335)

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics (TBE 2335)

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			70		dB

Characteristics (TBE 2335)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−15		15	−18	18	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Control range $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V

Characteristics (TBE 2335)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_I		3				MΩ
Open-loop voltage gain							
$f = 100$ Hz	G_{V0}	75	80		75		dB
$R_L = 10$ kΩ, $f = 100$ Hz	G_{V0}		85				dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2.0$		$V_S-0.5$	$-V_S+3$	$-V_S-0.8$	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		4	25		50	µV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		50				pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1])	SR		0.5				V/µs
Slew rate for inverting operation[1])	SR		0.5				V/µs

Characteristics (TBE 2335)

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

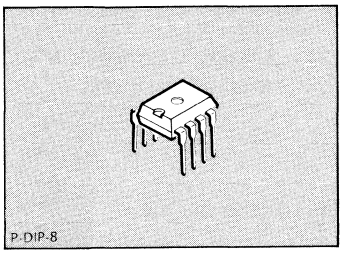
Dual PNP Operational Amplifiers

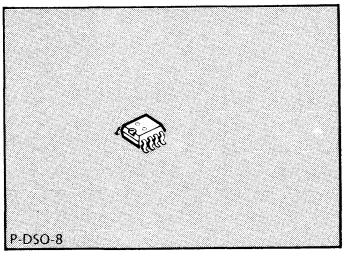
TAE 2453
TAF 2453

Bipolar IC

Features

- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.8 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (max. 100 mA)
- Output virtually short-circuit proof
- Wide common-mode voltage range
- Wide operating temperature range (TAF 2453 A; G)
- Pin-compatible to TBB 1458 B
- The characteristic curves of the electric parameters correspond to those of type TAE 1453 A; G





Applications

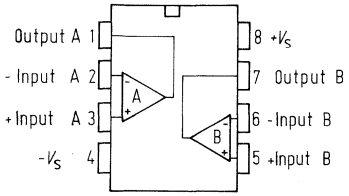
- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

Type	Ordering Code	Package	Color Code
S TAE 2453 A	Q67000-A2107	P-DIP-8	–
S TAE 2453 G	Q67000-A2108	P-DSO-8 (SMD)	white
S TAF 2453 A	Q67000-A2210	P-DIP-8	–
TAF 2453 G	Q67000-A2211	P-DSO-8 (SMD)	green

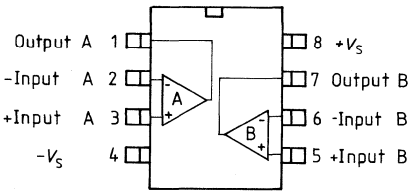
The TAF 2453/TAE 2453 consists of two independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence from the supply voltage.

Pin Configurations
(top view)

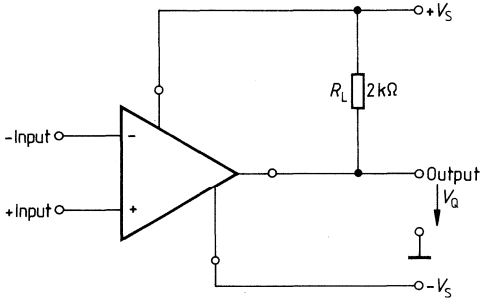
TAE 2453 A
TAF 2453 A



TAE 2453 G
TAF 2453 G

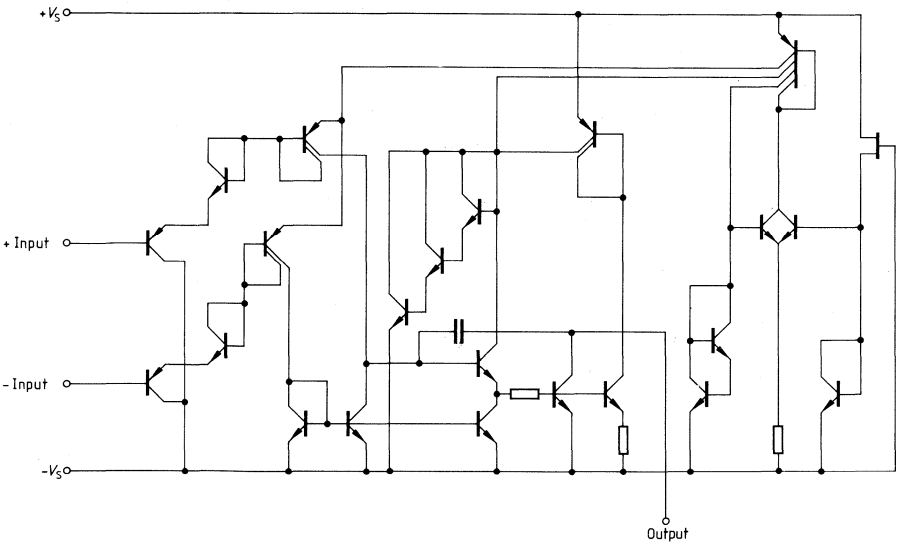


Connection Diagram



R_L = load resistance (collector resistance)

Circuit Diagram



1

Absolute Maximum Ratings (TAE 2453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	±18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAE 2453 A	$R_{th\ SA}$	100	K/W
TAE 2453 G	$R_{th\ SA}$	170	K/W

Operating Range (TAE 2453)

Supply voltage	V_S	±1.0 to ±18 (±0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics (TAE 2453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ, unless otherwise specified

		Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		
Parameter	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption, total	I_S		0.8	1.5		1.8	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−15		15	−100	100	nA
Input current	I_I		40	150		200	nA
Control range							
$R_L = 2$ kΩ, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.7	14.9	−14.7	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.5	14.9	−14.4	V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$-0.2		V_S-1.8	$-V_S$	V_S-2.0	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		75		dB

Characteristics (TAE 2453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6				µV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		1 1				V/µs V/µs

Characteristics $V_S = \pm 2$ V, $R_L = 10$ kΩ (TAE 2453)

Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−75	 40	75 150	−100	100 200	nA nA
Open-loop voltage gain	G_{V0}	70			70		dB

Absolute Maximum Ratings (TAF 2453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 150	°C °C
Thermal resistance system – air TAF 2453 A TAF 2453 G	 $R_{th\ SA}$ $R_{th\ SA}$	 100 170	 K/W K/W

Operating Range (TAF 2453)

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 with sligthly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

1

Characteristics (TAF 2453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption total	I_S		0.8	1.5		1.8	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−10	 40	10 100	−75	75 150	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14.7 −14.5	 14.8 14.8	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S$−0.3		V_S−1.5	$-V_S$	V_S−1.8	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.1	0.8		0.8	nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6	25		25	µV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		1 1				V/µs V/µs

Characteristics (TAF 2453)

$V_S = \pm 2$ V

Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−50	 40	50 100	−75	75 150	nA nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

SIEMENS

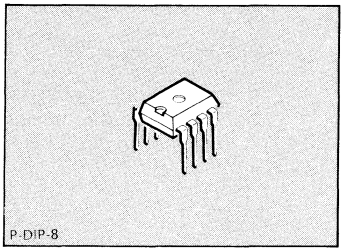
Dual Operational Amplifier

TBB 1458

Bipolar IC

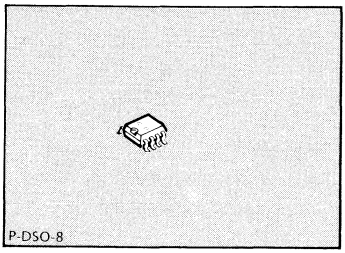
Features

- NPN input
- High differential input voltage
- Short-circuit proof
- Push-pull output
- Fully compatible with industrial standard type 1458



Applications

- Amplifier
- Comparator



The op amp TBB 1458 is outstanding for its large common-mode and differential input voltage range, as well as its short-circuit strength. No external components are required for frequency compensation.

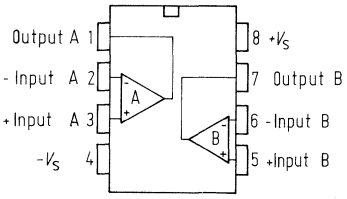
For single amplifier performance refer to the TBA 221 op amp.

Type	Ordering Code	Package	Color Code
■ S TBB 1458 B	Q67000-A1036	P-DIP-8	–
■ S TBB 1458 G	Q67000-A1458	P-DSO-8 (SMD)	orange/orange

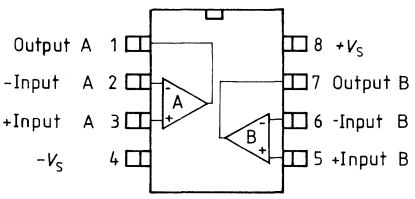
■ = Not for new Design

Pin Configurations (top view)

TBB 1458 B

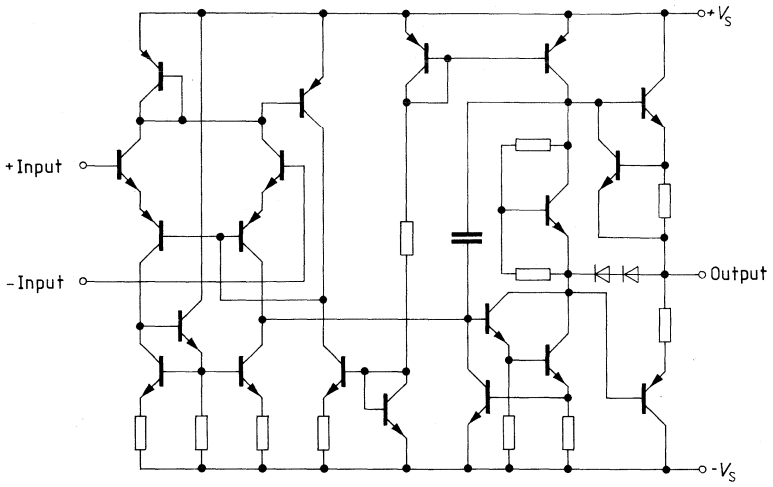


TBB 1458 G



1

Circuit Diagram of one Op Amp



Absolute Maximum Ratings

Parameter		Symbol	Limit Values	Unit
Supply voltage		V_S	±18	V
Input voltage[1] Differential input voltage[2]		V_I V_{ID}	±15 ±30	V V
Output short-circuit duration[3]		t_{QSC}	∞	
Junction temperature Storage temperature range		T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance	TBB 1458 B TBB 1458 G	$R_{th\ SA}$ $R_{th\ SA}$	100 170	K/W K/W
Operating Range				
Supply voltage		V_S	±4 to ±18	V
Ambient temperature		T_A	0 to 70	°C

1) For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
2) For supply voltages less than ±15 V, the maximum differential input voltage is equal to ± (V_S + I V_{S-} I).
3) Short circuit may be ground or to be supply voltage ± V_S, whereby the maximum ratings must not be exceeded.

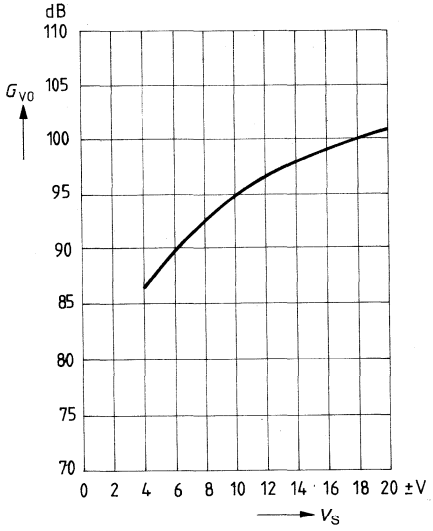
Characteristics

$V_S = \pm 15$ V

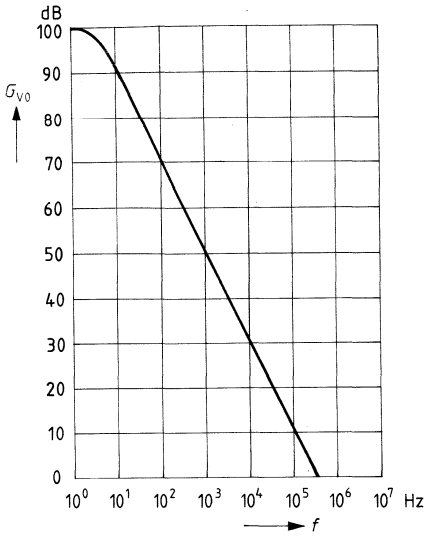
Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = 0$ °C to 70 °C min.	max.	Unit
Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current Open-loop supply current consumption, total Output short-circuit current	I_{IO} I_I I_S I_{QSC}	−200	±20 80 2 ±18	200 500 3	−300	300 800 3	nA nA mA mA
Input resistance	R_I	0.3	1				MΩ
Input capacitance	C_I		6				pF
Output resistance	R_Q		75				Ω
Control range $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	$V_{Q\,pp}$ $V_{Q\,pp}$	13 11	±14 ±13	−13 −11			V V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V
Voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L = 2$ kΩ	G_V	86	100		84		dB
Common-mode rejection $R_G \leq 10$ kΩ	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SCR}		30	150		150	µV/V
Temperature coefficient of V_{IO} Temperature coefficient of I_{IO}	α_{VIO} α_{IIO}		3 0.4				µV/K nA/K
Slew rate[1]) $G_V = 1$, $R_L \geq 2$ kΩ	SR		0.5				V/µs

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

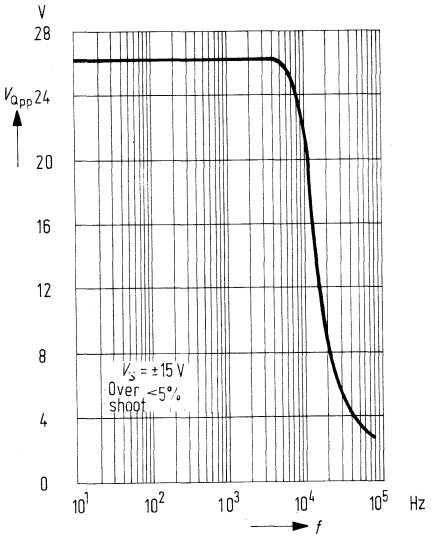
Open-loop voltage gain versus supply voltage



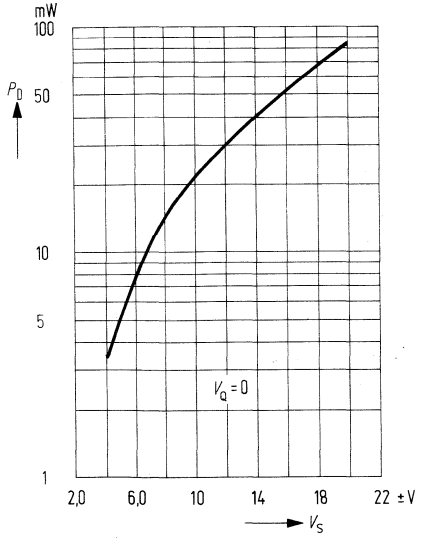
Open-loop voltage gain versus frequency



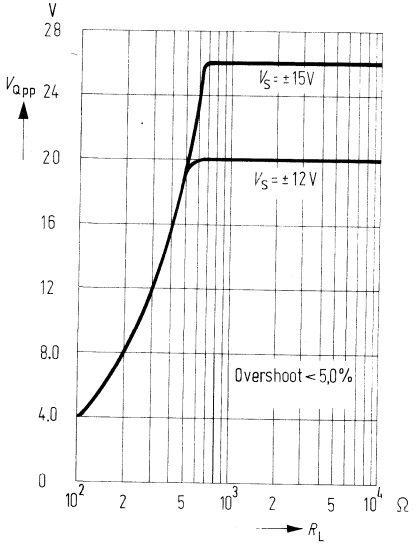
Power bandwidth
Output voltage versus frequency

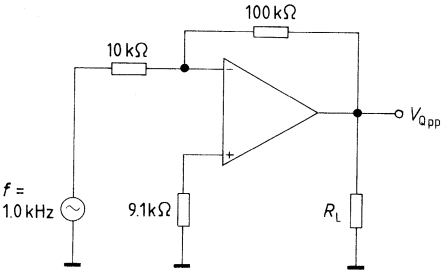


Power dissipation versus supply voltage

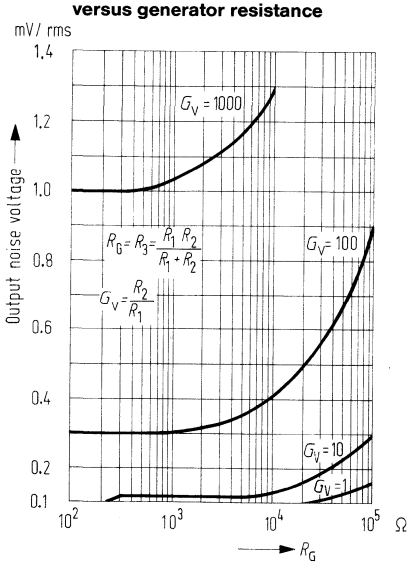


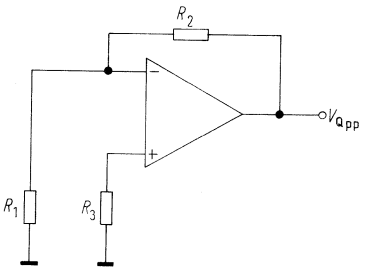
Output voltage versus load resistance





Output noise voltage versus generator resistance





For additional characteristic curves refer to TBA 221.

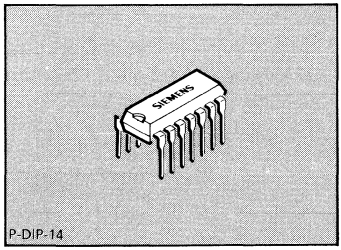
Quad Operational Amplifiers

TAA 4762
TAA 4765

Bipolar IC

Features

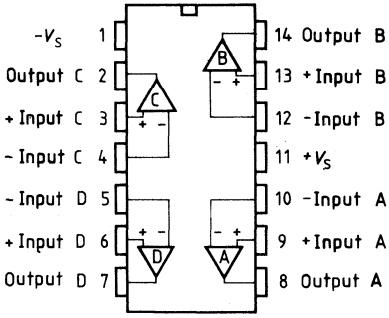
- Wide common-mode range
- Large supply voltage range
- Comprehensive protection against destruction
- High output current
- Large control range
- Internal frequency compensation
- Wide temperature range (TAA 4762 A)
- Open collector output



Applications

- Amplifier
- Comparator
- Level converter
- Driver

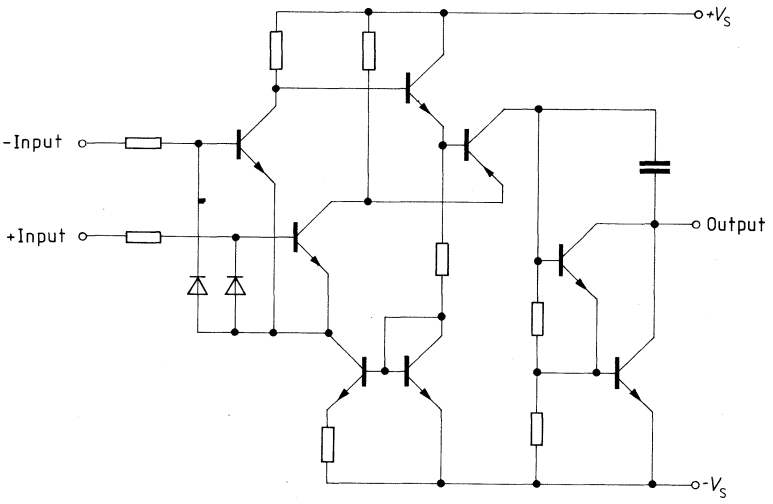
Pin Configuration (top view)



	Type	Ordering Code	Package
S	TAA 4762 A	Q67000-A2502	P-DIP-14
S	TAA 4765 A	Q67000-A1033	P-DIP-14

These op amps are particularly economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

Circuit Diagram of one Op Amp



Absolute Maximum Ratings (TAA 4762, TAA 4765)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

Operating Range (TAA 4762, TAA 4765)

Supply voltage		V_S	± 2 to ± 15	V
Ambient temperature	TAA 4762 A TAA 4765 A	T_A T_A	−55 to 125 −25 to 85	°C °C

1

Characteristics (TAA 4762)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4			−6	6	mV
Input offset current Input current	I_{IO} I_I	−100	±50 0.3	100 0.7	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ Ω, $f = 100$ Hz	 G_{V0} G_{V0}	 85	 87 92		 80		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_2+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15 1.5		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5$ Ω)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs

Characteristics (TAA 4762)

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain; $f = 100$ Hz	G_{V0}	80			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Characteristics (TAA 4765)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	±80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 85 90		 80		 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15		25	µV/K nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5$ Ω)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		0.5 0.5				V/µs V/µs

Characteristics (TAA 4765)

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain; $f = 100$ Hz	G_{V0}	75			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

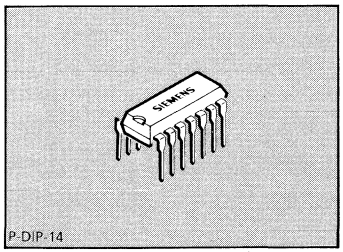
Quad Operational Amplifier with Darlington Input

TBC 4332 A
TBE 4335 A

Bipolar IC

Features

- High input impedance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Wide temperature range (TBC 4332 A)
- NPN Darlington input
- Open collector output
- Low input current
- Internal frequency compensation



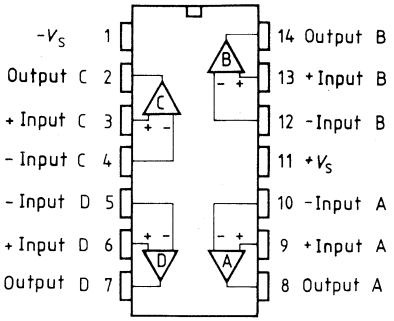
Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver

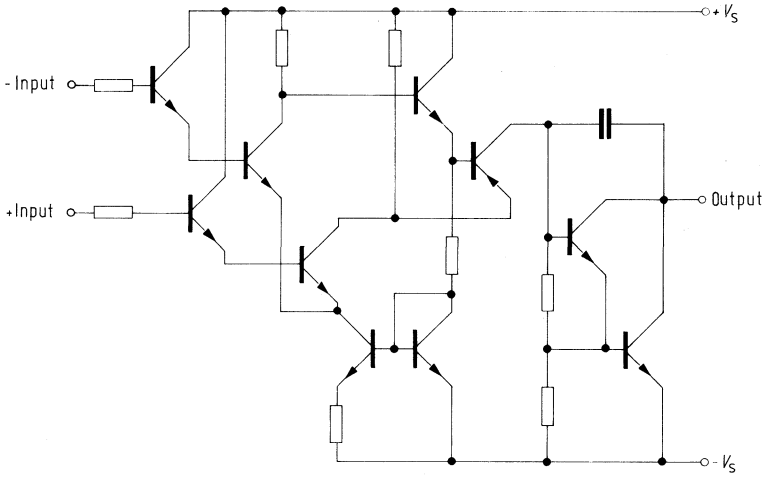
Type	Ordering Code	Package
S TBC 4332 A	Q67000-A2503	P-DIP-14
S TBE 4335 A	Q67000-A1167	P-DIP-14

These op amps are economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in control systems.

Pin Configuration
(top view)



Circuit Diagram of one Op Amp



Absolute Maximum Ratings (TBC 4332 A)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage, $V_S = \pm 13$ to ± 15 V Differential input voltage, $V_S = \pm$ 2 to ± 13 V	V_{ID} V_{ID}	±13 $\pm V_S$	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

Operating Range (TBC 4332 A)

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics (TBC 4332 A)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Control range $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$ $V_{Q\ pp}$	14.9 14.9		−14 −12.5	14.8 14.8	−14 −12	V V
Input impedance $f = 1$ kHz	Z_I		3				MΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	G_{V0} G_{V0}	80	83 88		75		dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range (comparator operation)	V_{IC}	V_S		$-V_S+2.0$	V_S	$-V_S+3$	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V

Characteristics (TBC 4332 A)

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		−4	25		50	μV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		50				pA/K
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1])	SR		0.5				V/μs
Slew rate for inverting operation[1])	SR		0.5				V/μs

Characteristics (TBC 4332 A)

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			70		dB

Absolute Maximum Ratings (TBE 4335 A)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage, $V_S = \pm 13$ to ± 15 V	V_{ID}	± 13	V
Differential input voltage, $V_S = \pm$ 2 to ± 13 V	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage tempture range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

Operating Range (TBE 4335 A)

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−25 to 85	°C

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−15		15	−18	18	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Control range $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance $f = 1$ kHz	Z_I		3				MΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 75	 80 85		 75		 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range (comparator operation)	V_{IC}	$+V_S$−0.5		$-V_S$+2.0	$+V_S$-0.8	$-V_S$+3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$ Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{VIO} α_{IIO}		4 50	25		50	µV/K pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

SIEMENS

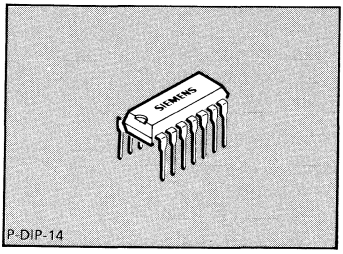
Quad PNP Operational Amplifier

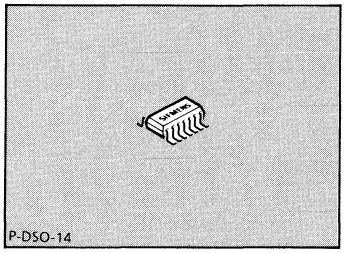
TAE 4453
TAF 4453

Bipolar IC

Features

- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 1.6 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Output virtually short-circuit proof
- Wide common-mode range
- Wide temperature range (TAF 4453 A; G)
- Pin-compatible to LM 324
- The typical characteristics of the electric parameters correspond to those of the TAE 1453 A; G





Applications

- Amplifier
- Level converter
- Driver
- Offset voltage switch
- Comparator

	Type	Ordering Code	Package
S	TAE 4453 A	Q67000-A2109	P-DIP-14
S	TAE 4453 G	Q67000-A2152	P-DSO-14 (SMD)
■ S	TAF 4453 A	Q67000-A2212	P-DIP-14
■	TAF 4453 G	Q67000-A2213	P-DSO-14 (SMD)

■ = Not for new design

The TAE 4453/TAF 4453 consists of four independent, frequency-compensated op amps, each having a PNP input, differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage.

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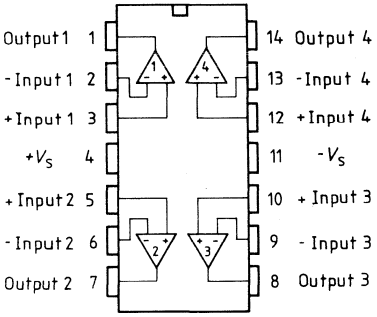
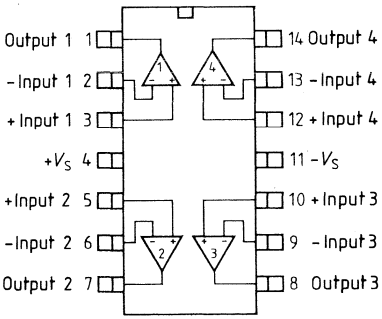
Pin Configurations (top view)

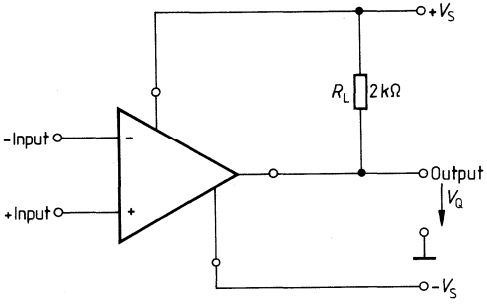
TAE 4453 A, TAF 4453 A



TAE 4453 G, TAF 4453 G

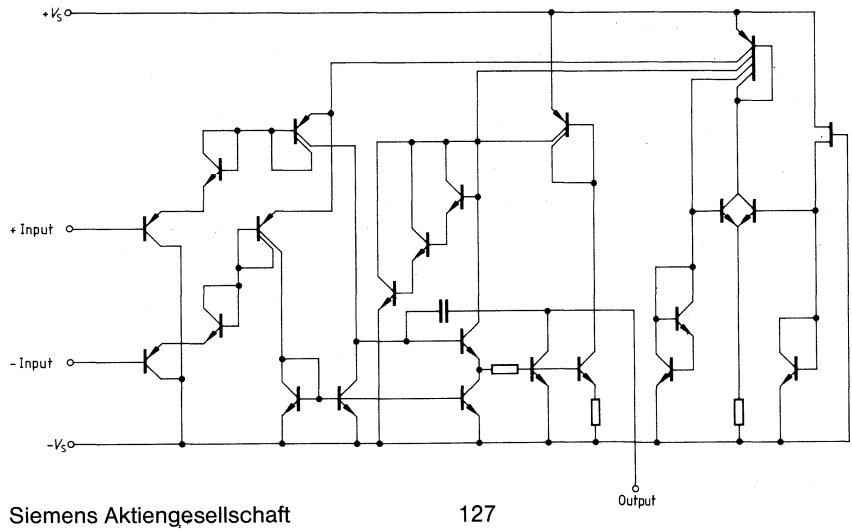


Connection Diagram



R_L = load resistance (collector resistance)

Circuit Diagram of one Op Amp



Absolute Maximum Ratings (TAE 4453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAE 4453 A	$R_{th\ SA}$	80	K/W
TAE 4453 G	$R_{th\ SA}$	120	K/W

Operating Range (TAE 4453)

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics (TAE 4453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	15		15	−25	25	nA
Input current	I_I		40	150		200	nA
Control range							
$R_L = 2$ kΩ, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.7	14.9	−14.7	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.5	14.9	−14.4	V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA

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Characteristics (TAF 4453)

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -25$ to 85 °C min.	max.	Unit
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S-0.2$		$+V_S-1.8$	$-V_S$	$+V_S-2.0$	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		6				µV/K
Slew rate for non-inverting operation[1])	SR		1				V/µs
Slew rate for inverting operation[1])	SR		1				V/µs

Characteristics (TAE 4453)

$V_S = \pm 2$ V

Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−75		75	−100	100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	70			70		dB

Absolute Maximum Ratings (TAF 4453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAF 4453 A	$R_{th\ SA}$	80	K/W
TAF 4453 G	$R_{th\ SA}$	120	K/W

Operating Range (TAF 4453)

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with sligthly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−10	 40	10 100	−15	15 150	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14.7 −14.5	 14.8 14.8	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$−0.3		$+V_S$−1.5	$-V_S$	$+V_S$−1.8	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6	0.8 25		0.8 25	nA/K µV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		1 1				V/µs V/µs

Characteristics

$V_S = \pm 2$ V

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−50	 40	50 100	−75	75 150	nA nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

SIEMENS

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Quad Low-Drift PNP Operational Amplifier

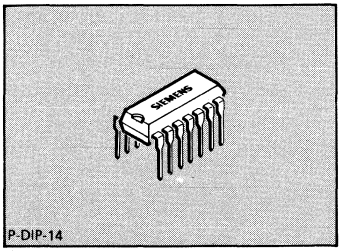
TAF 4463

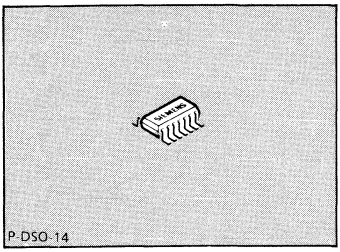
Advance Information

Bipolar IC

Features

- Low offset voltage drift
- High offset long-term stability
- Large common-mode range
- Supply voltage range: 2 V (1.8 V) to 36 V
- Low output saturation voltage, nearly independent of load current
- Output current up to 50 mA
- Output short-circuit proof (max. 10 h)
- Wide temperature range
- Pin-compatible to LM 324





Applications

- Low-drift sensor amplifier
- Level converter
- Driver
- Offset voltage switch
- Comparator

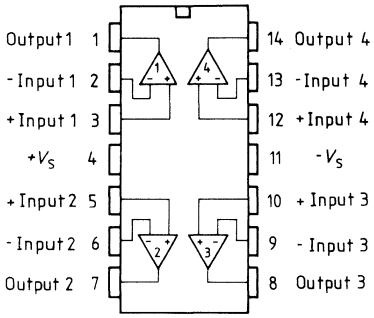
Type	Ordering code	Package
▼TAF 4463 A	Q67000-A8308	P-DIP-14
▼TAF 4463 G	Q67000-A8306	P-DSO-14 (SMD)

▼ = New type

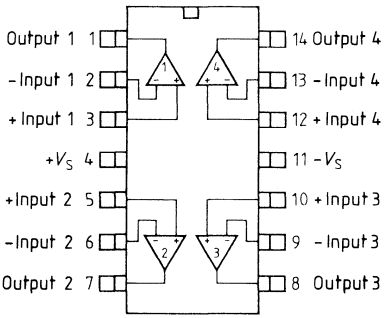
The TAF 4463 consists of four independent, frequency-compensated op amps, each having a PNP input, differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence from the supply voltage. The input offset voltage drift is lower than 200 µV after 100 thermal cycling operations.

Pin Configurations (top view)

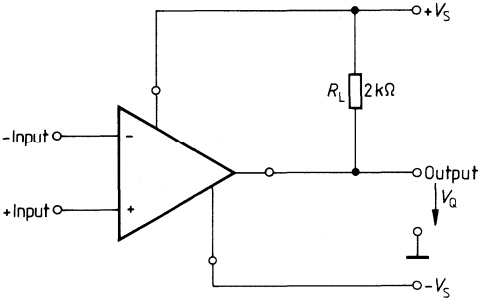
TAE 4463 A, TAF 4463 A



TAE 4463 G, TAF 4463 G

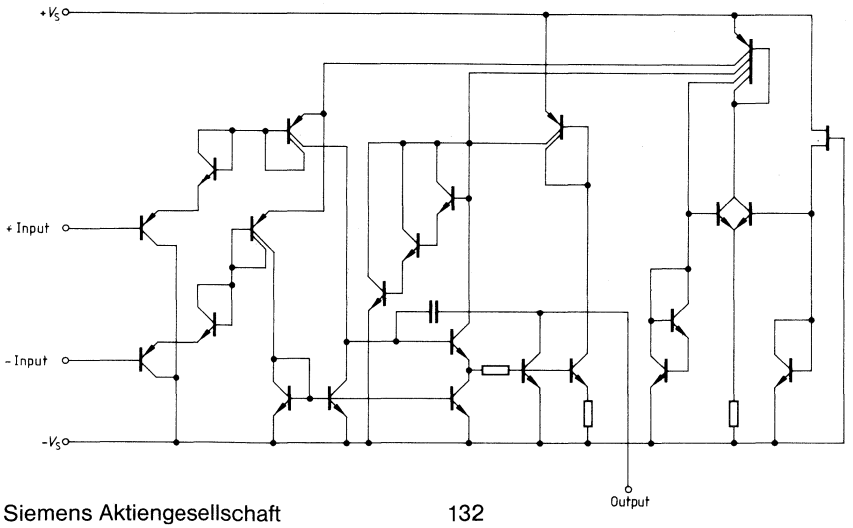


Connection Diagram



R_L = load resistance (collector resistance)

Circuit Diagram of one Op Amp



Absolute Maximum Ratings

Parameter		Symbol	Limit Values	Unit
Supply voltage		V_S	± 18	V
Output current		I_Q	50	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance system – air	TAF 4463 A	$R_{th\ SA}$	80	K/W
	TAF 4463 G	$R_{th\ SA}$	120	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18	V
Ambient temperature	T_A	−55 to 125	°C

[1]) at 0.1 W power dissipation

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−14		1	−2	2	mV
Input offset current Input current	I_{IO} I_I	−10		10 50	−15	15 100	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14.7 −14.5	 14.8 14.8	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$−0.3		$+V_S$−1.5	$-V_S$	$+V_S$−1.8	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}			0.1		0.1	nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}			5		5	µV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		1 1				V/µs V/µs
Input offset voltage drift[2]	ΔV_{IO}	−200		200	−200	200	µV
Input offset current drift[2]	ΔI_{IO}	−5		5	−5	5	nA

[1] For the relationship between power bandwidth and slew rate refer to **"Introduction to Operational Amplifiers"**

[2] after 100 thermal cycling operations (−55...150 °C)

Selector Guide

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C	Page
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA max	Input offset voltage ($R_G = 50\ \Omega$) V_{IO} mV min/max	
Threshold Switches						
TCA 105	P-DIP-6	30	−25 to 85	50		137
TCA 105 B	P-DIP-6	20	−25 to 85	50		137
TCA 105 G	P-DSO-6 (SMD)	30	−25 to 85	50		137
TCA 345 A	P-DIP-4	10	−25 to 85	70		143
TCA 965 A	P-DIP-14	4.75 to 27	−25 to 85	50		147
TCA 965 G	P-DSO-14 (SMD)	4.75 to 27	−25 to 85	50		147
Comparators with Darlington Input						
TCA 312 A	P-DIP-6	±2 to ±15	−55 to 125	70	±10	161
TCA 312 G	P-DSO-6 (SMD)	±2 to ±15	−55 to 125	70	±10	161
TCA 315 A	P-DIP-6	±2 to ±15	−25 to 85	70	±15	161
TCA 315 G	P-DSO-6 (SMD)	±2 to ±15	−25 to 85	70	±15	161
Comparators with TTL-compatible Output Voltage, High Output Current						
TCA 322 A	P-DIP-6	±2 to ±15	−55 to 125	70	±4	162
TCA 322 G	P-DSO-6 (SMD)	±2 to ±15	−55 to 125	70	±4	162
TCA 325 A	P-DIP-6	±2 to ±15	−25 to 85	70	±5.5	162
TCA 325 G	P-DSO-6 (SMD)	±2 to ±15	−25 to 85	70	±5.5	162
Current-Monitoring IC						
TLE 4951	P-DIP-14	4.5 to 32	−40 to 125	40		176
TLE 4951 G	P-DSO-14	4.5 to 32	−40 to 125	40		176

SIEMENS

Threshold Switch

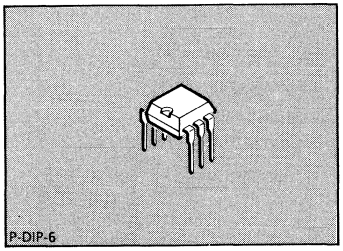
TCA 105

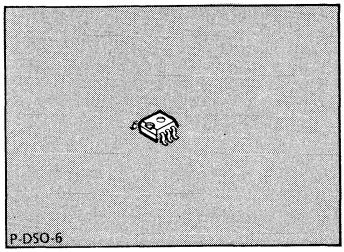
2

Bipolar IC

Features

- Wide range of supply voltage, 4.5 to 30 V
- High output current, 50 mA
- TTL-compatible
- Triggerable with dc signal





Type	Ordering Code	Package	Color Code
S TCA 105	Q67000-A527	P-DIP-6	–
S TCA 105 B	Q67000-A587	P-DIP-6	–
S TCA 105 G	Q67000-A988	P-DSO-6 (SMD)	orange/white

The TCA 105 contains an oscillator stage, a threshold switch, and two anti-valent output stages. The IC is especially suitable for application in proximity switches, light reflection switches, and other contactless switching applications.

Absolute Maximum Ratings

Parameters	Symbol	Limit Values		Unit
		TCA 105	TCA 105 B	
Supply voltage	V_S	30	20	V
Output voltage (pin 4, pin 5)	V_Q	30	20	V
Output current	I_Q	50	50	mA
Switching frequency	f_S	40	40	kHz
Input voltage	V_I	≥ 0[1])	≥ 0[1])	V
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−55 to 125	−55 to 125	°C
Thermal resistance (system – air)				
TCA 105, TCA 105 B	$R_{th\ SA}$	115	115	K/W
TCA 105 G	$R_{th\ SA}$	200		K/W

Operating Range

Supply voltage	V_S	4.75 to 30	4.75 to 20	V
Ambient temperature	T_A	−25 to 85	−25 to 85	°C
Oscillating frequency	f_{OSC}	1 to 4.5	1 to 4.5	MHz

Characteristics

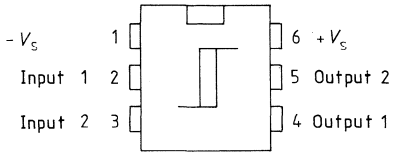
Static measurement, pins 3 and 1 interconnected
$V_S = 12$ V, $T_A = 25$ °C, $R_C = 5.6$ kΩ

Parameters	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current	I_S		3.4	5	mA
Input threshold voltage with compensation resistor R_C	V_I	300	400	480	mV
Input threshold current	I_I		−60		µA
Hysteresis	V_{hy}	20	35	50	mV
L output voltage $I_Q = 16$ mA	$V_{Q\,L}$		0.25	0.35	V
H output voltage	$V_{Q\,H}$		corresponds to V_S		
Reverse current, $V_S = 30$ V and/or 20 V	$I_{Q\,H}$			60	µA
L output voltage $I_Q = 50$ mA	$V_{Q\,L}$		0.7	1.15	V
Switching time in TTL operation $I_Q = 16$ mA	t		3		µs

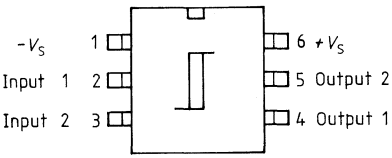
[1]) Negative input voltages are not permitted

Pin Configurations
(top view)

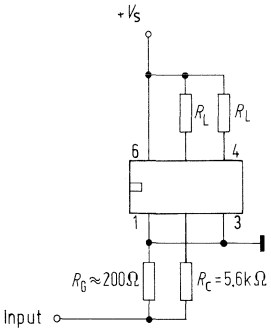
TCA 105,
TCA 105 B



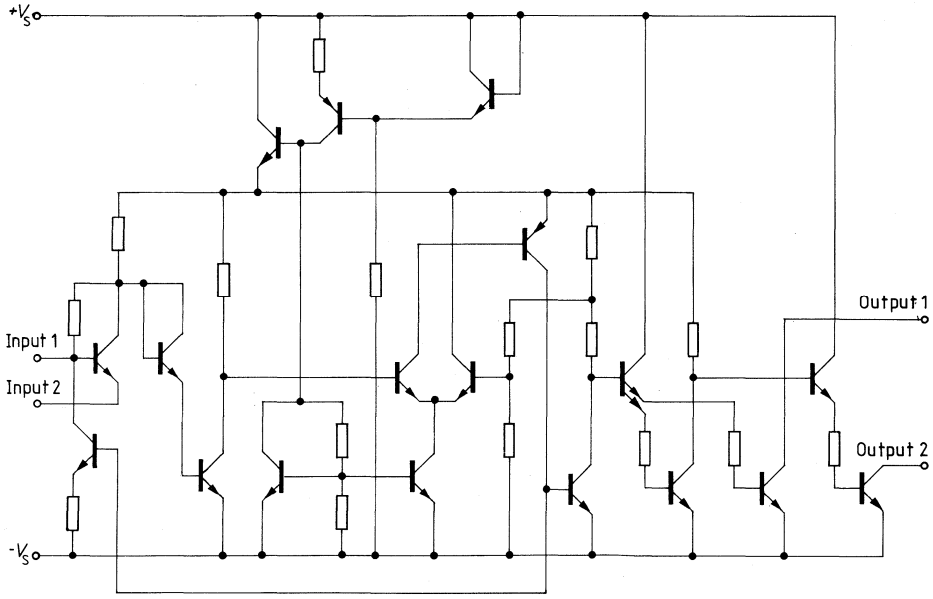
TCA 105 G



Test Circuit

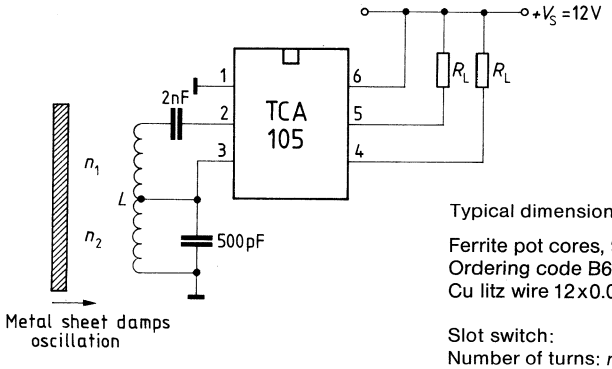


Circuit Diagram



Application Examples

Inductive Slot Switch or Proximity Switch



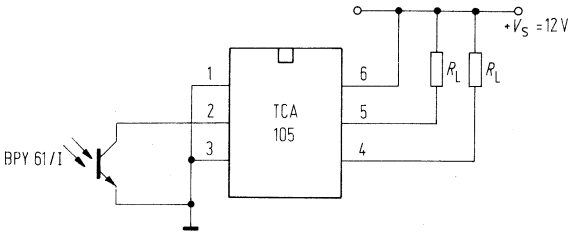
Typical dimensioning values:

Ferrite pot cores, 9 mm dia.
Ordering code B65935-A-X25
Cu litz wire 12x0.04 mm

Slot switch:
Number of turns: $n = 2 \times 25$
Distance between pot core halves:
2.5 to 3.5 mm

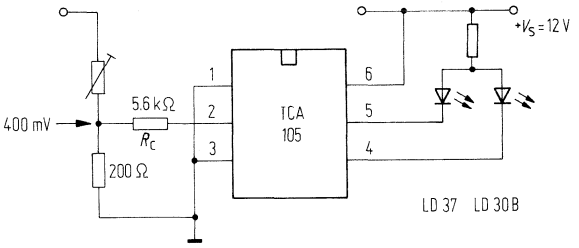
Proximity switch:
Number of turns: $n_1 = 8$, $n_2 = 40$
Distance: 2 to 3 mm

Light-Operated Switch (switching amplifier for phototransistor BPY 61)

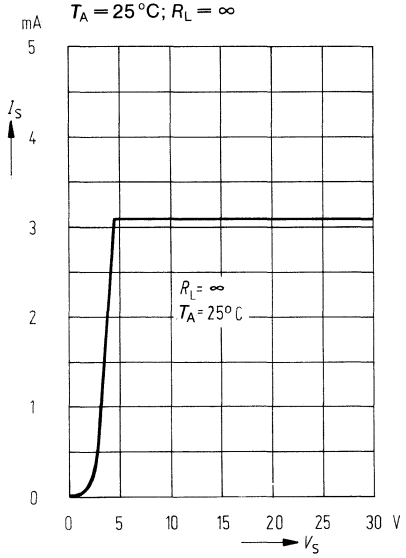


Application Example

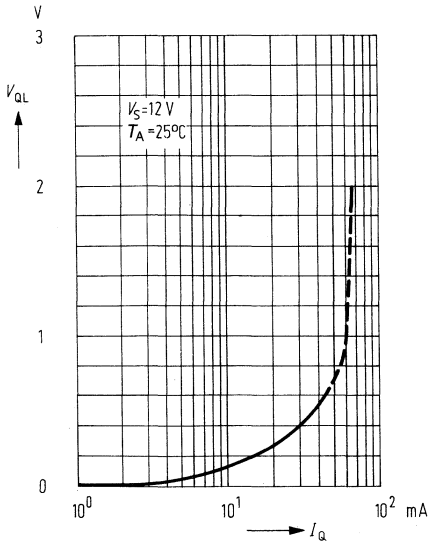
Voltage Monitor



Current consumption
Supply current versus supply voltage
$T_A = 25\,°C$; $R_L = \infty$

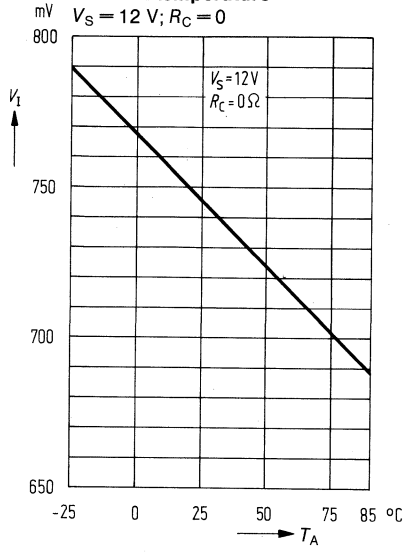


L output voltage versus output current
$T_A = 25\,°C$; $V_S = 12$ V



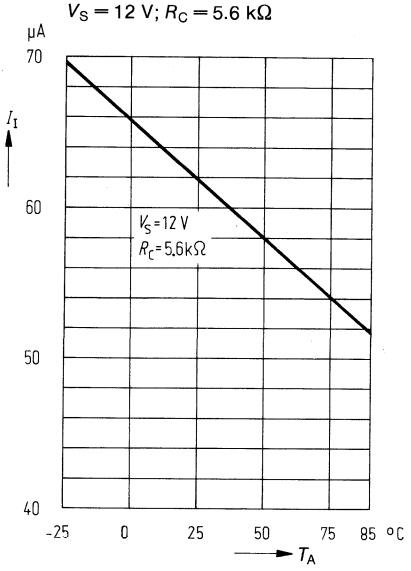
Switching threshold Input voltage versus ambient temperature

$V_S = 12$ V; $R_C = 0$

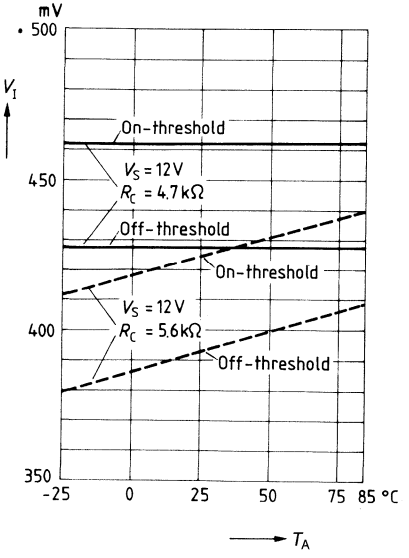


Input current versus ambient temperature

$V_S = 12$ V; $R_C = 5.6$ kΩ

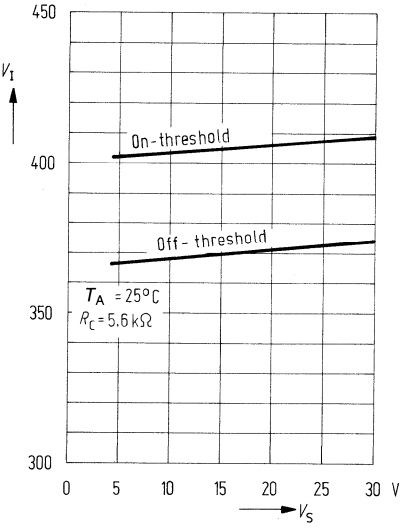


Switching threshold Input voltage versus ambient temperature



Switching threshold Input voltage versus supply voltage

$T_A = 25$ °C; $R_C = 5.6$ kΩ



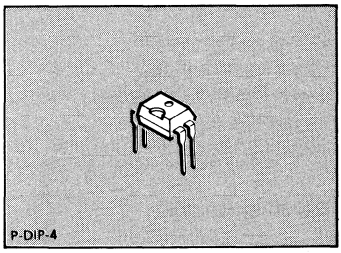
Threshold Switch

TCA 345 A

Bipolar IC

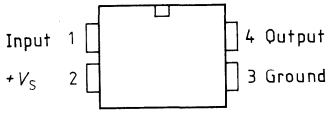
Features

- TTL-compatible
- High output current
- Very high input impedance
- Good stability due to hysteresis
- Few external components



Pin Configuration

(top view)



Type	Ordering Code	Package
■ S TCA 345 A	Q67000-A564	P-DIP-4

■ = Not for new design

Threshold switches featuring linear, supply voltage-dependent threshold value. Inductive loads may be switched at the output without protective diode.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	10	V
Output current	I_Q	70	mA
Input voltage	V_I	0 to V_S	V
Inductance at the output	L_Q	500	mH
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	140	K/W

Operating Range

Supply voltage	V_S	2 to 10	V
Ambient temperature	T_A	−25 to 85	°C

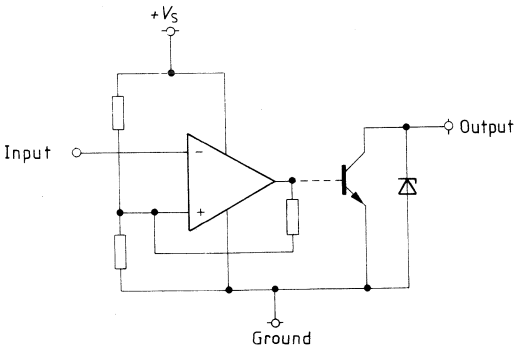
Characteristics

$T_A = 25\ °C$

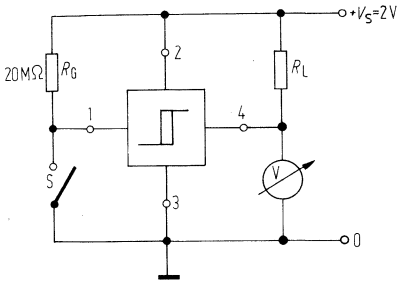
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption at output current					
I_Q = 0 mA; V_S = 2 V	$I_{S\,H}$		0.55	0.80	mA
= 5 V	$I_{S\,H}$		1.35	2.00	mA
I_Q = 40 mA; V_S = 2 V	$I_{S\,L}$		1.85	3.00	mA
= 5 V	$I_{S\,L}$		7.00	9.00	mA
L output voltage at I_Q = 40 mA V_S = 2 V	$V_{Q\,L}$		150	300	mV
Output reverse current V_Q = 10 V	$I_{Q\,H}$			30	µA
Switching threshold V_S = 2 to 10 V[1]	V_I	0.63 x V_S	0.66 x V_S	0.69 x V_S	V
Linearity error of the switching threshold (referred to V_S = 2 V)				3.0	%
Hysteresis (in % of V_S) V_S = 2 V	ΔV_I	6.0	10	15	%
Hysteresis (in % of V_S) V_S = 5 V	ΔV_I	6.0	20		%
Hysteresis (in % of V_S) V_S = 10 V	ΔV_I	6.0	20		%
Input current	I_I		10	30	nA
Z voltage via output	V	11.0	13.6	15.0	V
Temperature response of switching threshold			30		ppm/K

[1]) measured with increasing input voltage

Circuit Diagram

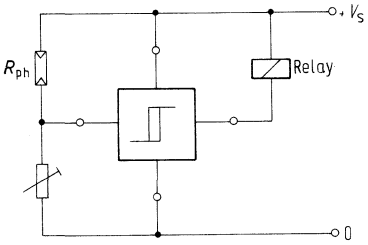


Test Circuit

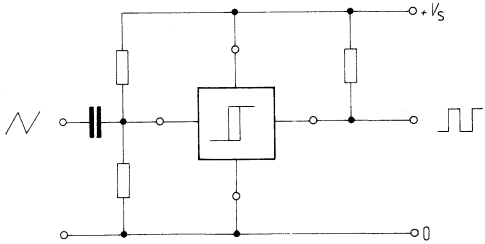


Application Circuits

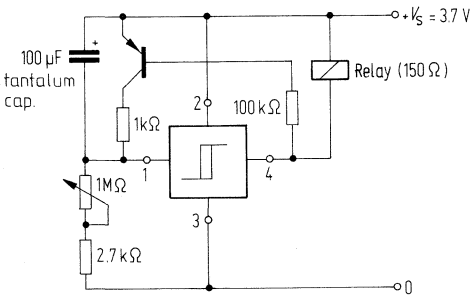
Twilight Switch
(switches on light at nightfall)



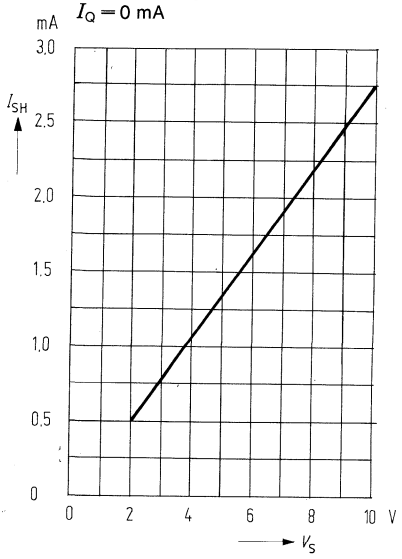
Triangle-square Converter



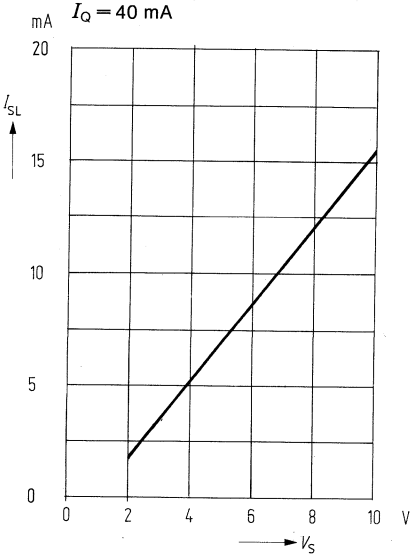
Clock Generator



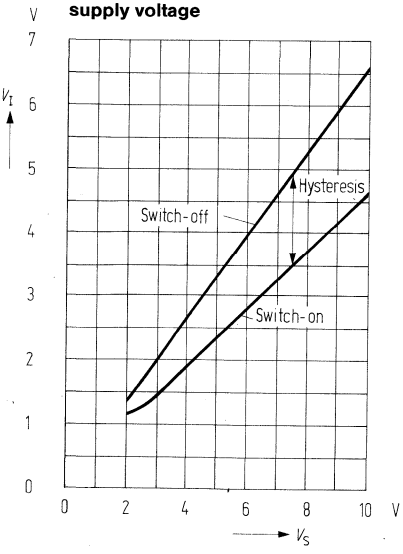
Current consumption I_{SH} versus supply voltage
$I_Q = 0$ mA



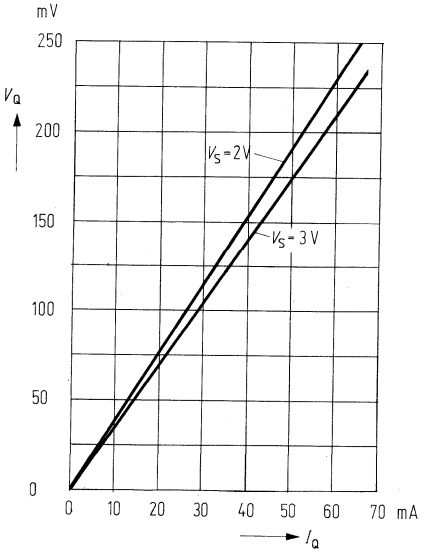
Current consumption I_{SL} versus supply voltage
$I_Q = 40$ mA



Switching threshold Input voltage versus supply voltage



Output voltage versus output current



SIEMENS

Window Discriminator

TCA 965 A

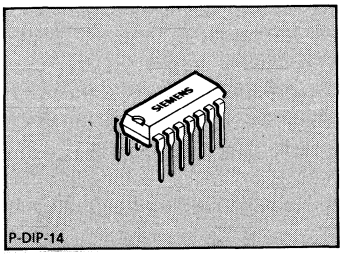
2

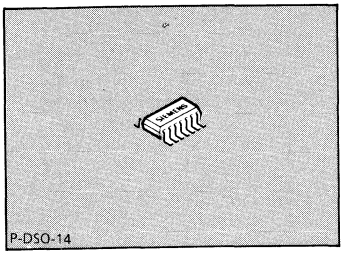
Preliminary Data

Bipolar IC

Features

- Two window settings
  - direct setting of lower and upper edge voltage (window edges)
  - indirect setting by window center voltage and half window width
- Adjustable hysteresis
- Digital outputs with open collectors for currents up to 50 mA
- Adjustable reference voltage V_{Stab}





	Type	Ordering Code	Package
▼ S	TCA 965 A	Q67000-A8227	P-DIP-14
▼ S	TCA 965 G	Q67000-A2368	P-DSO-14 (SMD)

▼ New type

The window discriminator compares an input voltage to a defined voltage window. The digital outputs show whether the input voltage is below, within or above this window.

The TCA 965 A window discriminator is especially suitable as a tracking or compensating controller with a dead band in control engineering and for the selection of DC voltages within a certain tolerance of the required setpoint value in measurement engineering. When it is used as a Schmitt trigger, switching frequencies up to a typical value of 200 kHz are possible.

Functional Description

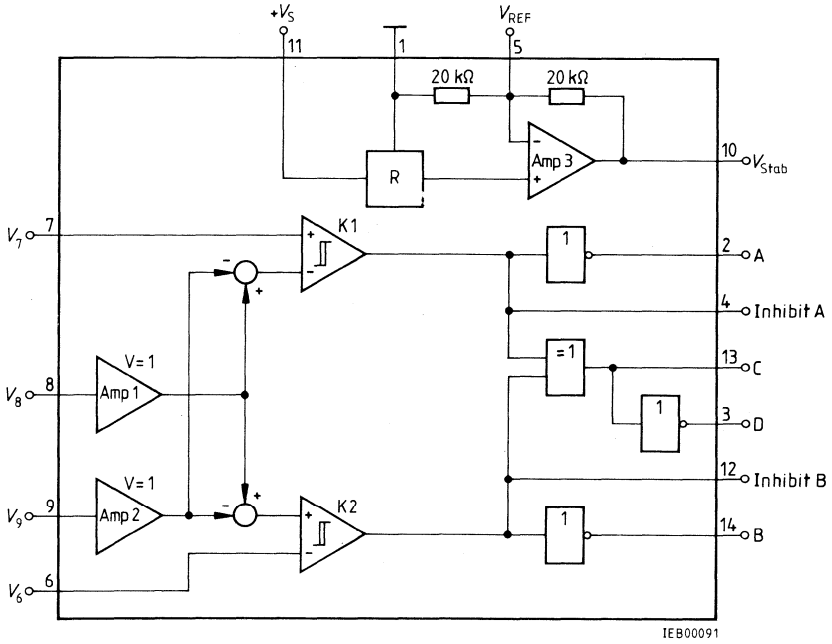
Amplifier Amp 3 increases the voltage of the reference source R to $V_{Stab} = 2 \times V_{REF}$. The amplification factor can be altered by external wiring. With direct setting of the window, the input voltage appears on amplifier Amp 1 (V_8), the upper edge voltage on comparator K2 (V_6) and the lower edge voltage on comparator K1 (V_7).

With indirect setting of the window, the input voltage appears on inputs V_6 and V_7, while the center voltage is connected to amplifier A1 (V_8).

The voltage applied to the input (V_9) of amplifier Amp 2 is subtracted symmetrically from the output voltage of amplifier Amp 1 and added. The comparators switch with hysteresis. The logic gates have open collectors.

If the inhibit input A or B is connected to ground, output A or B will always be high. If output A or B is not to be inhibited, the inhibit inputs can be connected to V_8 or left open-circuit. It is advisable to connect the inhibit inputs to V_8 for an improved signal-to-noise ratio.

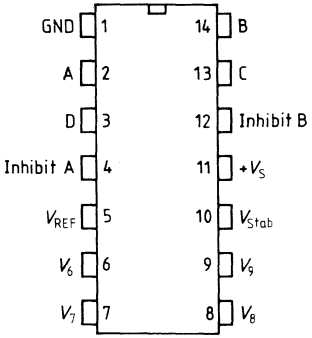
Block Diagram



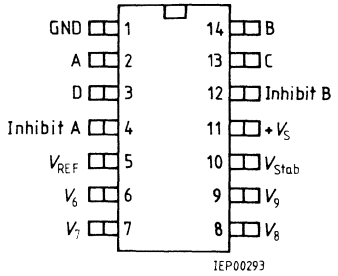
Outputs A, B, C, D are open-collector

Pin Configuration
(top view)

P-DIP-14



P-DSO-14



Pin Definitions and Functions

Pin	Symbol	Pin Function in direct setting | of window	indirect setting
1	GND	GND	
2	A	Logic output A	
3	D	Logic output D = A ⊕ B EXNOR	
4	Inhibit A	Connected to GND: logic output A = HIGH	
5	V_{REF}	Internal V_{REF} = 3 V	
6	V_6	Upper edge voltage	Input voltage $V_{6/7}$
7	V_7	Lower edge voltage	Input voltage $V_{6/7}$
8	V_8	Input voltage	Center voltage
9	V_9	GND	Half window width
10	V_{Stab}	Internal V_{Stab} = 6 V	
11	$+V_S$	Supply voltage	
12	Inhibit B	Connected to GND: logic output B = HIGH	
13	C	Logic output C = A ⊕ B EXOR	
14	B	Logic output B	

Absolute Maximum Ratings

Maximum ratings for ambient temperature T_A −25 to 85 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage (pin 11)	V_S		30	V
Difference in input voltage between pins 6, 7, 8	V_I		15	V
Input voltage (pins 6, 7, 8, 9)	V_I		30	V
Output current (pins 2, 3, 13, 14)	I_Q		50	mA
Output voltage (pins 2, 3, 13, 14) independent of V_S	V_Q		30	V
Voltage on V_{REF} (pin 5)	V_R		8	V
Output current of stabilized voltage (pin 10)	I_{10}		10	mA
Inhibit input voltage (pins 4, 12)	V_{IH}		30	V
Junction temperature	T_J		150	°C
Storage temperature	T_{Stg}	−55	125	°C
Thermal resistance system-air P-DIP-14	$R_{th\ SA}$		80	K/W
P-DSO-14	$R_{th\ SA}$		125	K/W

Operating Range

Supply voltage	V_S	4.5	30	V
Ambient temperature	T_A	−25	85	°C

Electrical Characteristics

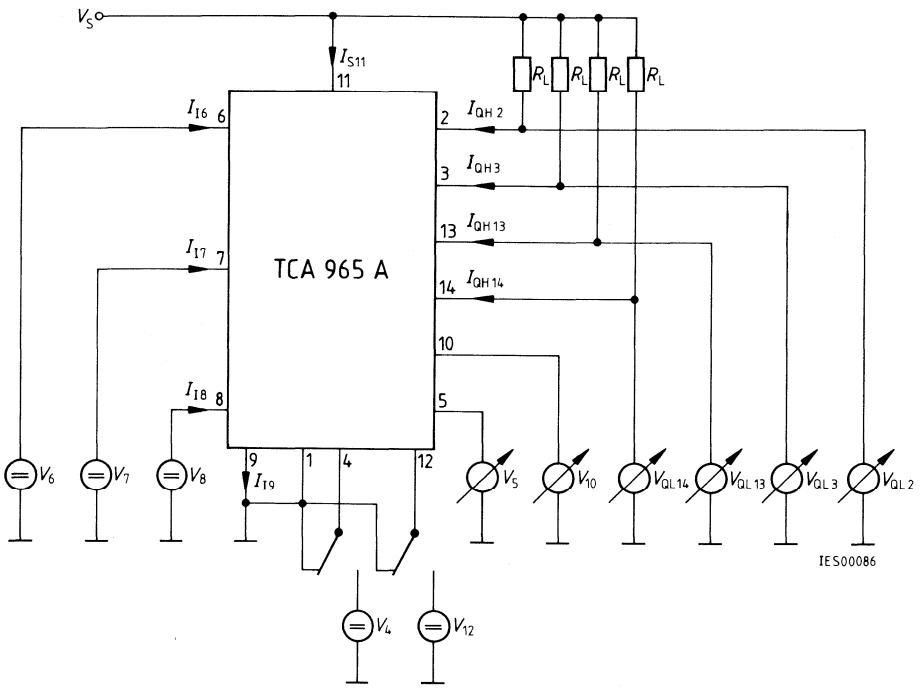
$V_S = 10$ V; $T_A = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
Current consumption	I_S		5	7	mA	V_2, $V_{13} = V_{QH}$	1
Input current (pins 6, 7, 8)	I_I		20	50	nA		1
Input current, pin 9	$-I_I$		400	3000	nA		1
Input offset voltage in direct setting of window	V_{IO}	−20		20	mV		1
Input offset voltage in indirect setting of window	V_{IO}	−50		50	mV		2
Input-voltage range on pins 6, 7, 8	V_I	1.5		V_S-1	V	$\Delta V_I < 13$ V	1
Input-voltage range on pin 9	V_I	50		$V_S/2$	mV		2
Differential input voltage	$V_6-(V_8-V_9)$			13	V		
	$(V_8+V_9)-V_7$			13	V		
Reference voltage[1])	V_5	2.8	3	3.2	V	$I_{ref} = 0$	
Stabilized voltage on pin 10[2])	V_{10}	5.5	6	6.5	V	$V_s > 7.9$ V	
TC of reference voltage	αV_5		0.3		mV/K		
Sensitivity of reference voltage to supply-voltage variation	$\Delta V_5/\Delta V_S$		2		mV/V		
Output reverse current	I_{QH}			10	µA		
Output saturation voltage	V_{QL}		100	200	mV	$I_Q = 10$ mA	1
			500	800	mV	$I_Q = 50$ mA	
Hysteresis of window edges	V_U-V_L	18	22	35	mV		
Inhibit threshold	$V_{4,12}$	1		1.8	V		
Inhibit current	$I_{4,12}$		−100		µA		
Switching frequency	f_{dir}	50	80		kHz		1
	f_{ind}	150	200		kHz		2

[1]) Range aimed at is 2.85 to 3.15 V
[2]) Range aimed at is 5.6 to 6.4 V

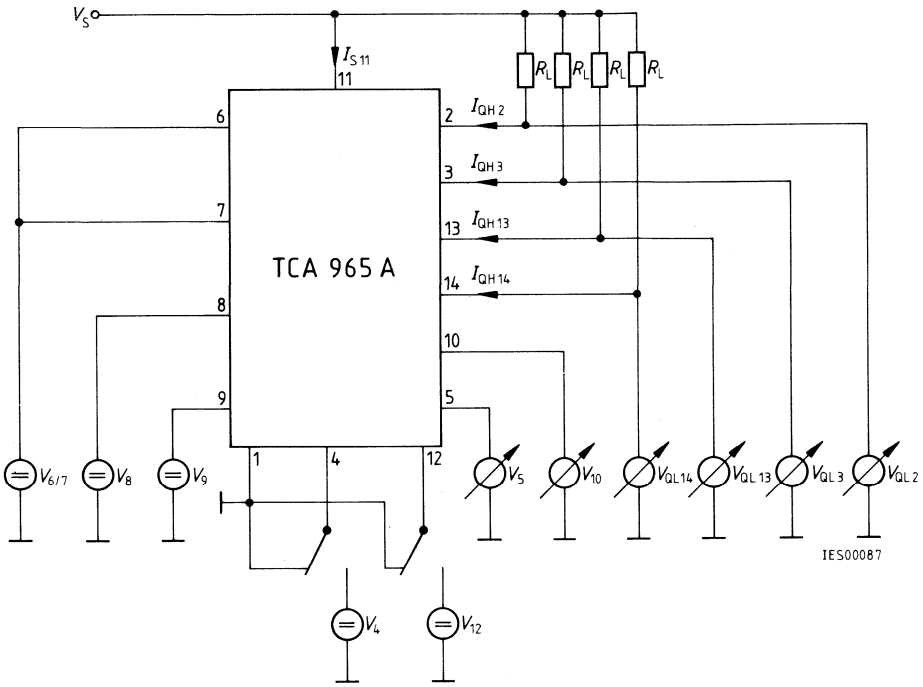
Test Circuit 1

Direct Setting of Window

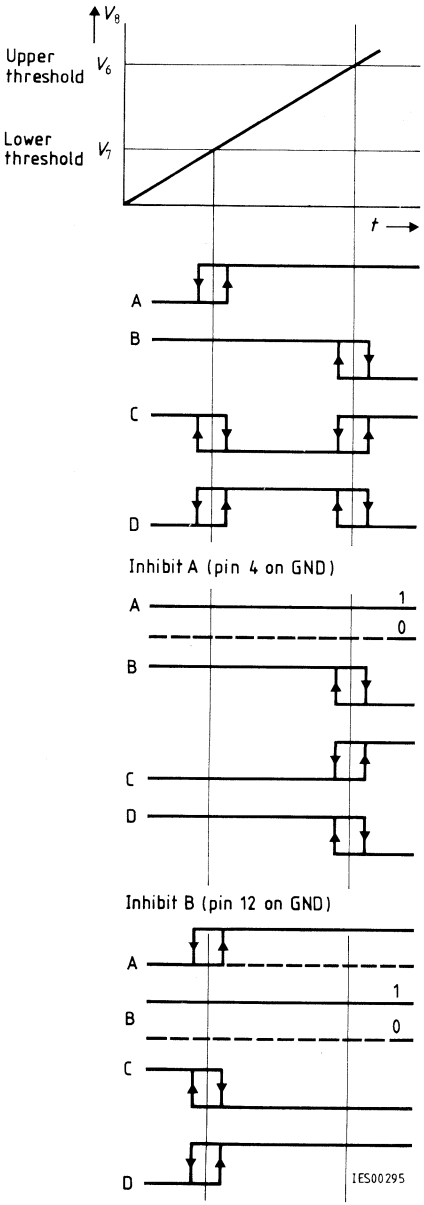


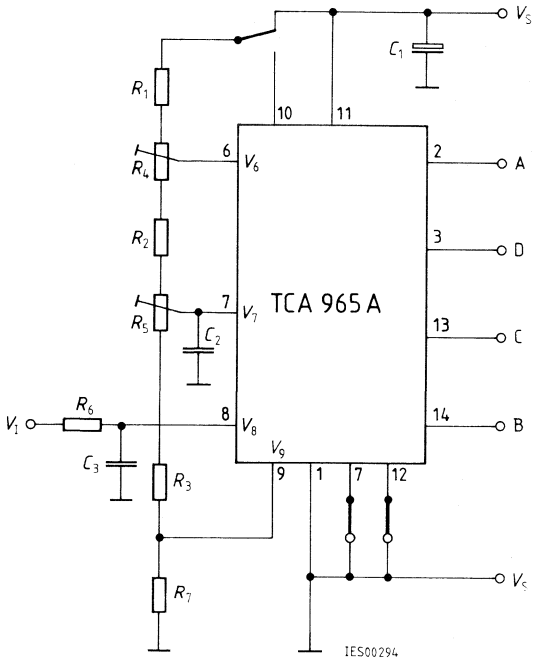
Test Circuit 2

Indirect Setting of Window by Center Voltage and Half Window Width



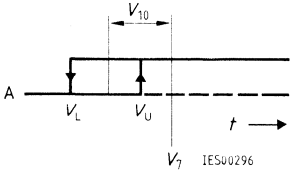
Application Circuit 1: Direct Setting of Window Assignment of Logic Outputs A, B, C, D





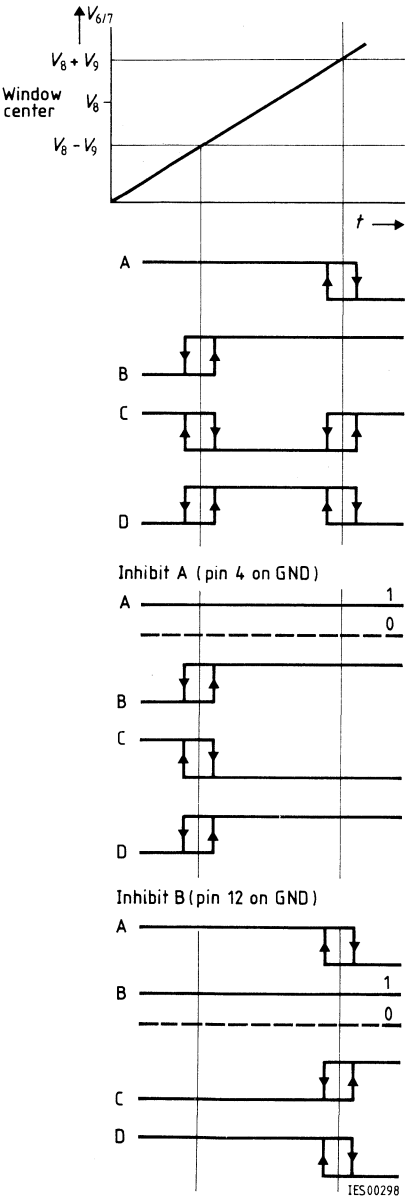
To increase switching frequency, pin 9 is grounded via R_7 (V_S approx. 10 mV) and not directly

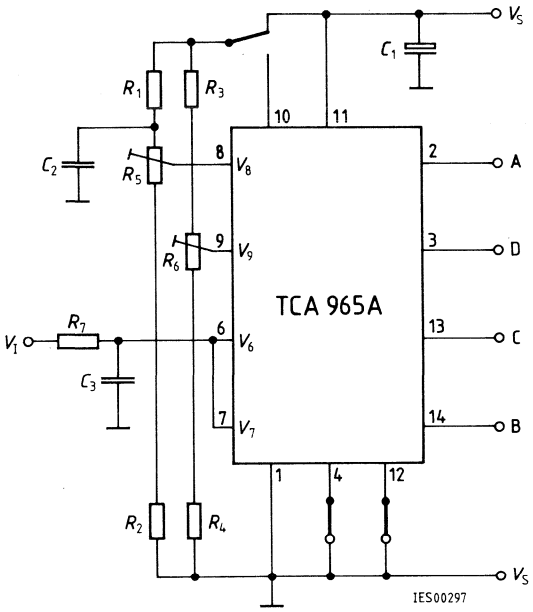
$V_6 - V_9$ = Upper edge voltage
$V_7 + V_9$ = Lower edge voltage
V_8 = Input voltage



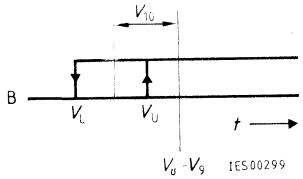
$$V_{10} = \frac{V_L + V_U}{2} - V_7$$

Application Circuit 2: Indirect Setting of Window by Center Voltage and Half-Window Width V
Assignment of Logic Outputs A, B, C, D



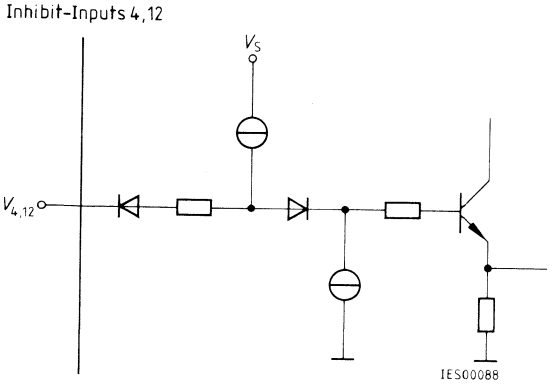


V_6 = V_7 = Input voltage
V_8 = Center voltage
V_9 = Half window width



$$V_{10} = \frac{V_L + V_U}{2} - (V_8 - V_9)$$

Schematic Circuit Diagram



TCA 965 A

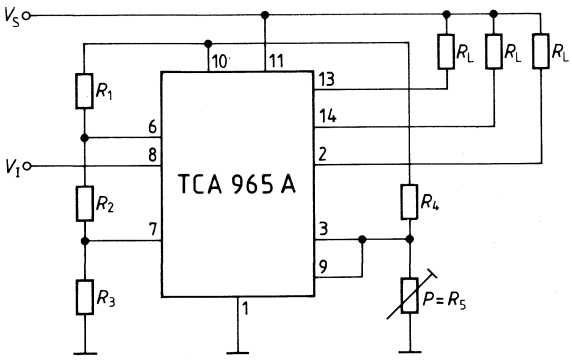
$V_{4,12}$	Output A, B
GND	HIGH
V_S	Normal funct.
Open	Normal funct.

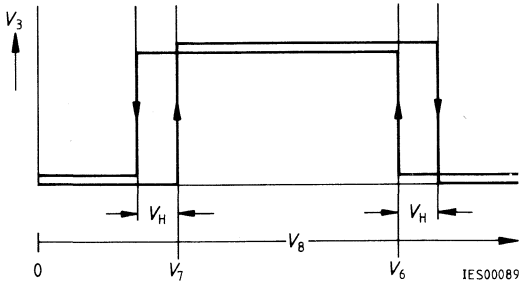
TCA 965 for comparison

$V_{4,12}$	Output A, B
GND	HIGH
V_S	Impermissible
Open	Normal funct.
< 6 V	Low

Application Circuit 3

Symmetrically enlarged edge hysteresis in direct setting of window





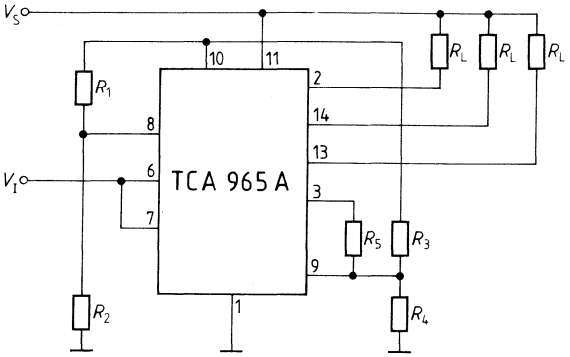
Calculation of hysteresis V_H

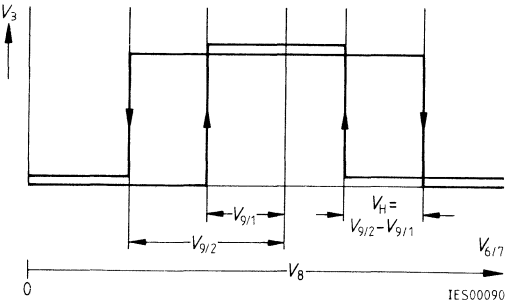
$$V_H = V_{10} \frac{R_5}{R_4 + R_5}$$

$$\frac{V_{10}}{R_4 + R_5} + \frac{V_{10}}{R_1 + R_2 + R_3} \leq 10 \text{ mA}$$

Application Circuit 4

Symmetrically enlarged edge hysteresis in indirect setting of window





Calculation of hysteresis V_H

$$V_H = V_{9/2} - V_{9/1}$$

$$V_{9/1} = V_{10} \frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5}$$

$$V_{9/2} = V_{10} \frac{R_4}{R_3 + R_4}$$

SIEMENS

Comparators with Darlington Input TTL-Compatible

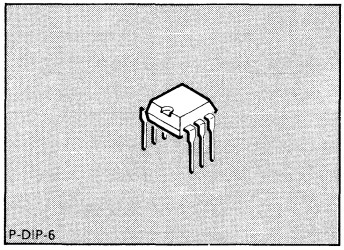
TCA 312
TCA 315

2

Bipolar IC

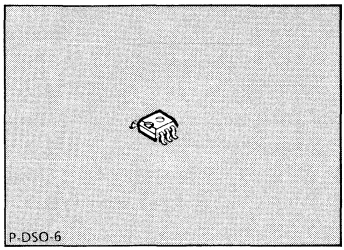
Features

- Very high input resistance
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 312 A; G)
- NPN input
- Open collector output
- High slew rate



Applications

- Comparator
- Level converter
- Driver



Type	Ordering Code	Package	Color Code
S TCA 312 A	Q67000-A2048	P-DIP-6	–
TCA 312 G	Q67000-A2509	P-DSO-6 (SMD)	red
S TCA 315 A	Q67000-A561	P-DIP-6	–
S TCA 315 G	Q67000-A1005	P-DSO-6 (SMD)	red/yellow

TCA 312 abd TCA 315 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly.

SIEMENS

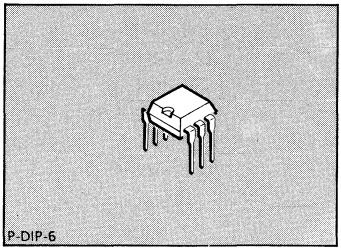
Comparators, TTL-Compatible

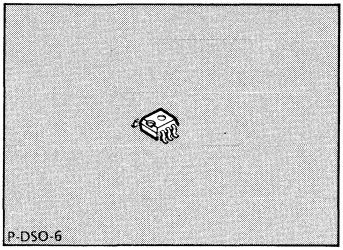
TCA 322
TCA 325

Bipolar IC

Features

- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 322)
- NPN input
- Open collector output
- High slew rate





Applications

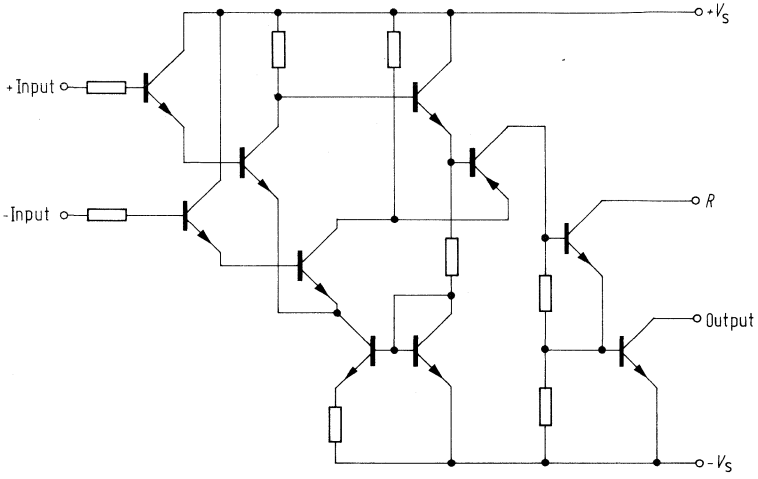
- Comparator
- Level converter
- Impedance converter
- Driver

	Type	Ordering Code	Package	Color Code
■ S	TCA 322 A	Q67000-A2501	P-DIP-6	–
■	TCA 322 G	Q67000-A2508	P-DSO-6 (SMD)	brown
■ S	TCA 325 A	Q67000-A562	P-DIP-6	–
■ S	TCA 325 G	Q67000-A1012	P-DSO-6 (SMD)	green/yellow

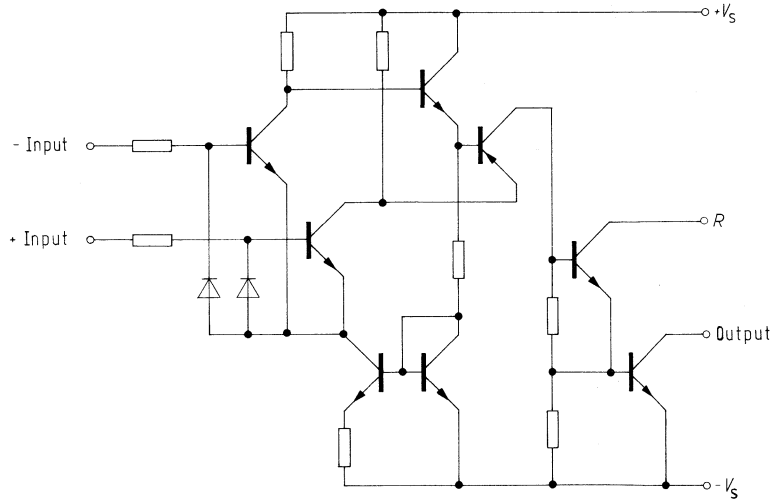
■ = Not for new design

TCA 322 and TCA 325 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly.

Circuit Diagram TCA 312/315



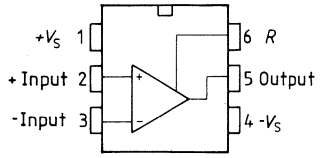
Circuit Diagram TCA 322/325



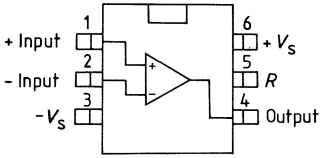
Pin Configurations

(top view)

TCA 312 A; TCA 322 A
TCA 315 A; TCA 325 A

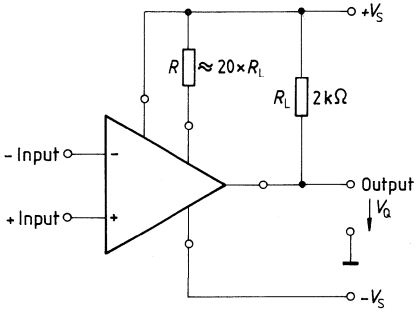


TCA 312 G; TCA 322 G
TCA 315 G; TCA 325 G



Connection Diagram

R_L = load resistance (collector resistance)



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current Driver current	I_Q I_{dr}	70 10	mA mA
Differential input voltage V_S = 13 to 15 V Differential input voltage V_S = 2 to 13 V	V_{ID} V_{ID}	± 13 ± V_S	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 312 A system – air TCA 312 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V; R = 6.8 kΩ
R_L = 2 kΩ
unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = −55 to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current Input current V_{ID} = ± 13 V	I_{IO} I_I I_I	−5	 5 	5 15 200	−10	10 25 	nA nA nA
Control range V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V V_S = ± 15 V, f = 100 kHz	$V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	14.9 14.9	 ± 10	−14.8 −14.0	14.8 14.8	−14.6 −13.5	V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ,
$R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 83 88 60	 	 75	 	 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50			µV/K pA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		30				V/µs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			1		5	µA

Characteristics

$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General Technical Information"**

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	±15	V
Output current Driver current	I_Q I_{dr}	70 10	mA mA
Differential input voltage V_S = 13 to 15 V Differential input voltage V_S = 2 to 13 V	V_{ID} V_{ID}	±13 $\pm V_S$	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 315 A system – air TCA 315 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

V_S = ±5 V to ±15 V
R = 6.8 kΩ, R_L = 2 kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = −25 to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−15		15	−18	18	mV
Input offset current Input current Input current V_{ID} = ±13 V	I_{IO} I_I I_I	−10	 5 	10 25 200	−20	20 35 	nA nA nA
Control range V_S = ±15 V R_L = 620 Ω; V_S = ±15 V V_S = ±15 V, f = 100 kHz	$V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	14.9 14.9	 ±10	−14.8 −14.0	14.8 14.8	−14.6 −13.5	V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ,
$R_L = 2$ kΩ,
unless otherwise specified

		Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		
Parameter	**Symbol**	**min.**	**typ.**	**max.**	**min.**	**max.**	**Unit**
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 75	 80 85 60	 	 75	 	 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50			µV/K pA/K
Slew rate of V_q for non-inverting operation[1] (see TAA 765, test circuit 1)	SR		30				V/µs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			10		20	µA

Characteristics

$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General Technical Information"**

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current Driver current at R	I_Q I_{dr}	70 10	mA mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 322 A system – air TCA 322 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−100	± 50 0.3	100 0.7	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V $V_S = \pm 15$ V, $f = 100$ kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9	 ± 10	 −14.8 −14.0	 14.8 14.8	 −14.6 −13.5	 V V V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values $T_A = -55$ to 125 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 85	 87 92 60	 	 80	 	 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		6 0.3	25 1.5			µV/K nA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		50				V/µs
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			1		5	µA

Characteristics
$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	80			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General Technical Information"**

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 15	V
Output current Driver current at R	I_Q I_{dr}	70 10	mA mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 325 A system – air TCA 325 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	± 80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V $V_S = \pm 15$ V, $f = 100$ kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9	 ± 10	 −14.8 −14.0	 14.8 14.8	 −14.6 −13.5	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C min.	typ.	max.	Limit Values T_A −25 to 85 °C min.	max.	Unit
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 85 90 60		 80		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		6 0.3				µV/K nA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		50				V/µs
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			10		20	µA

Characteristics

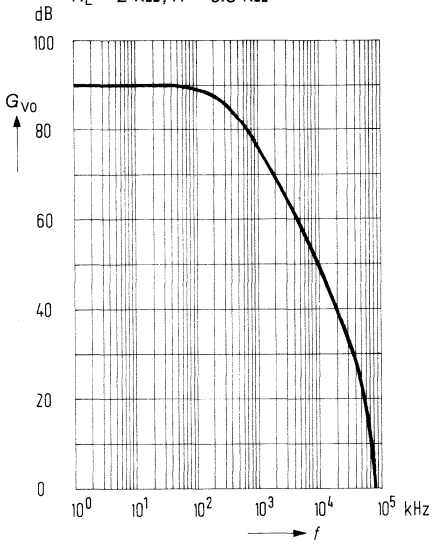
$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			75		dB

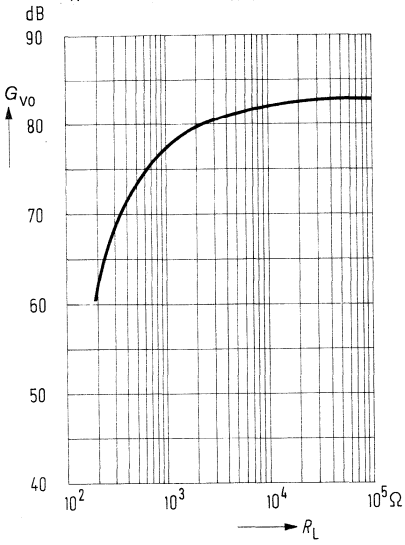
1) For the relationship between power bandwidth and slew rate refer to **"General Technical Information"**

2

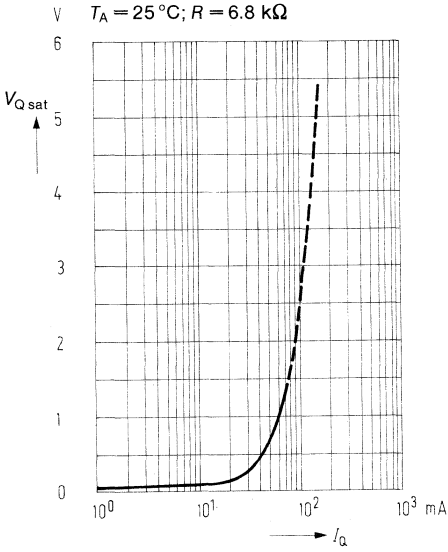
Open-loop voltage gain versus frequency
$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



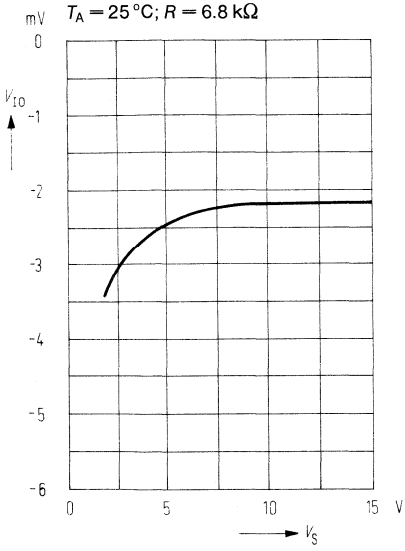
Open-loop voltage gain versus load resistance
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



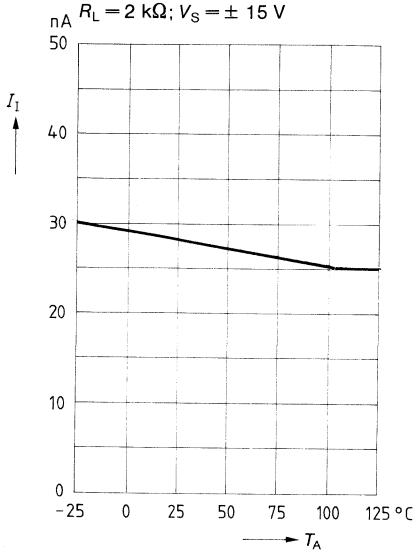
Output saturation voltage versus output current
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



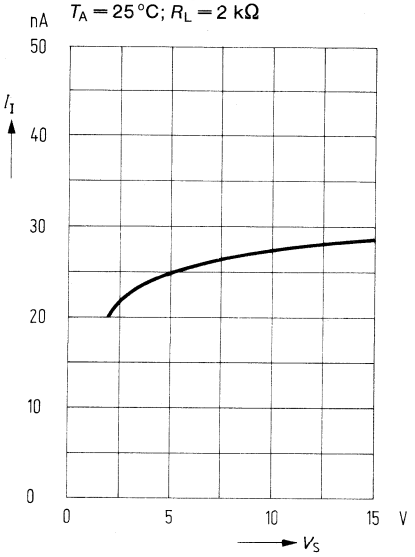
Input offset voltage versus supply voltage
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



Input current versus ambient temperature
$R_L = 2\ k\Omega$; $V_S = \pm 15\ V$

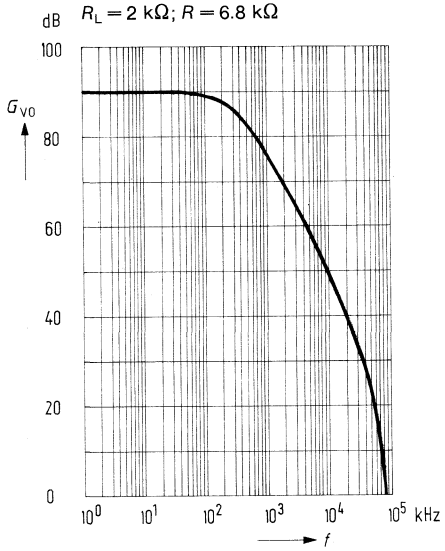


Input current versus supply voltage
$T_A = 25\,°C$; $R_L = 2\ k\Omega$

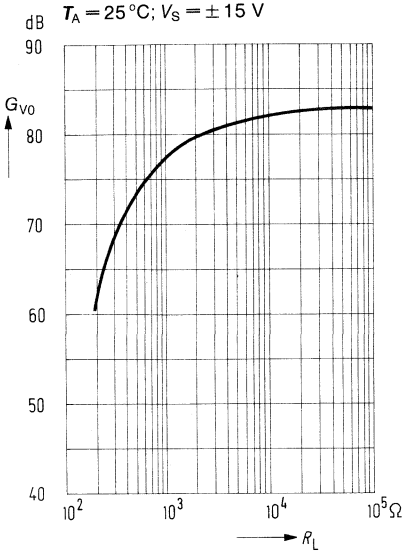


2

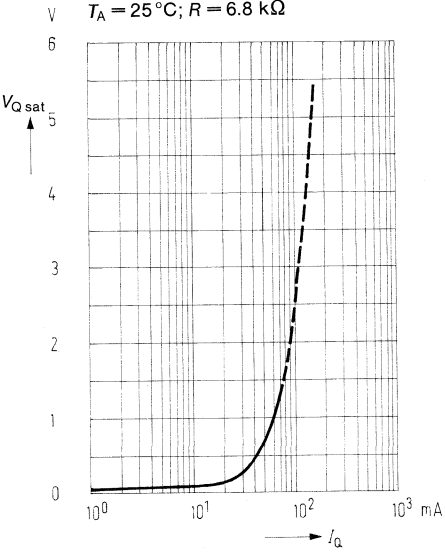
Open-loop voltage gain versus frequency
$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



Open-loop voltage gain versus load resistance
$T_A = 25\,°C$; $V_S = \pm 15\ V$



Output saturation voltage versus output current
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



SIEMENS

Current-Monitoring IC

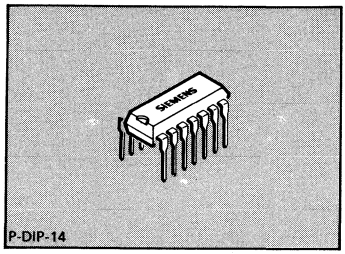
TLE 4951

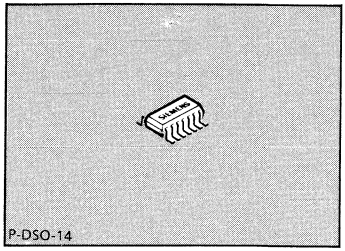
Preliminary Data

Bipolar IC

Features

- Input currents max 25 µA, protective resistors can be connected in series
- Effective protection against destruction by excessive voltages such as load dump pulses occuring in cars
- Supply voltage range from 4.5 to 32 V
- Input voltage range up to 32 V, independent of supply voltage
- Switching threshold of comparators dependent on supply voltage, corresponding to the characteristic of light bulbs
- Temperature range: −40 °C to 125 °C





Applications

Current monitoring of

- light bulbs
- electric motors
- relays
- glow plugs
- circuits

especially suitable for:

- automotive electronics
- industrial plants

	Type	Ordering Code	Package
S ■	TLE 4951	Q67000-A8266	P-DIP-14
S ■	TLE 4951 G	Q67000-A8267	P-DSO-14 (SMD)

■ Not for new design

The TLE 4951 is designed to monitor the correct function of circuits, in particular those of light bulbs in cars. The IC comprises four identical comparator stages, the logic function of which corresponds to an exclusive-OR gate. With each comparator, pairs of lamps or single lamps can be monitored by means of the voltage drops across shunt resistors (R_{sh}) in the positive supply line (see **application circuits 1 and 2**).

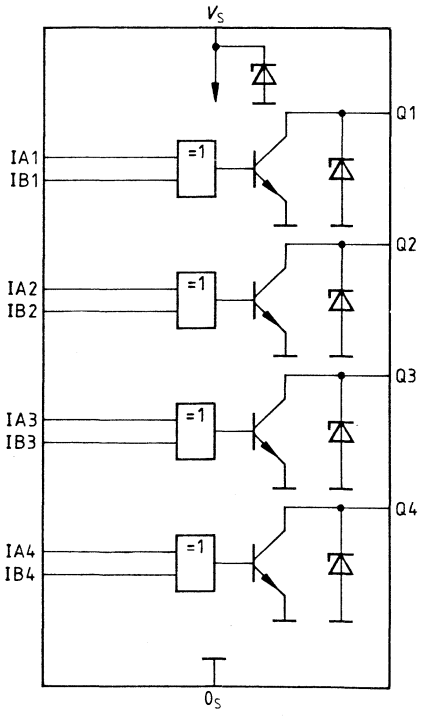
Due to small differential input currents it is possible to connect protective resistors (R_s) in series. This provides a high degree of **protection against destruction** by interfering voltages occuring in automobiles.

Functional Description

The component incorporates four identical comparator circuits. Each of these functional units has two equivalent inputs and one open-collector output Q. If the voltages differ by more than approx. 15 mV, the switching state changes from H (off-state) to L (on-state).

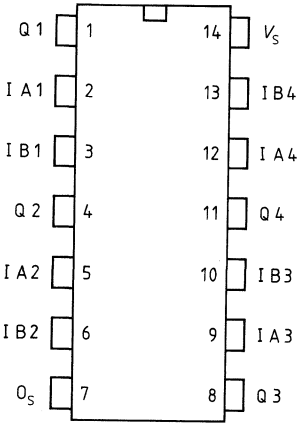
For an input voltage < 4.5 V at both the inputs, the output can switch to H independently of the differential input voltage. For an input voltage < 2.0 V the output is reliably off-state.

Block Diagram

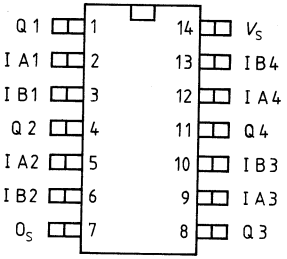


Pin Configurations
(top view)

TLE 4951



TLE 4951 G



Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	Output 1
2 3	IA1 IB1	Input A1 Input B1
4	Q2	Output 2
5 6	IA2 IB2	Input A2 Input B2
7 8	0_S Q3	GND Output 3
9 10	IA3 IB3	Input A3 Input B3
11	Q4	Output 4
12 13	IA4 IB4	Input A4 Input B4
14	V_S	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage	V_S	−0.5	32	V	
Input voltages	$V_{A,B}$	−45	45	V	
Output voltage	V_Q	−0.5	32	V	
Output current	I_Q		40	mA	
Current through protecting structures					
at the supply terminal	I_S	−600	600	mA	$t_d < 2$ ms
at the outputs Q	I_{SQ}	−400	400	mA	$t_d < 2$ ms
Thermal resistance					
system – air TLE 4951	$R_{th\ SA}$		75	K/W	
system – air TLE 4951 G	$R_{th\ SA}$		125	K/W[1])	

[1]) 75 K/W ceramic substrate

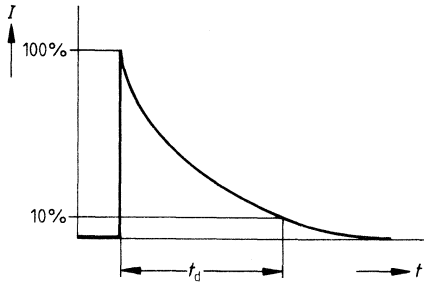
Operating Range

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S	4.5	32	V
Ambient temperature	T_A	−40	125	°C
Common-mode input voltage range independent of V_S	V_{IC}	4.5	32	V
Differential input voltage	V_{ID}		100	mV

Permissible short-term overvoltages with series resistors R_S:

$$+V\,(V_{S;\,Q}) = I_{S;\,Q} \times R_V\,(V_{S;\,Q}) + 32\ \text{V}$$

$$-V\,(V_{S;\,Q}) = -I_{S;\,Q} \times R_V\,(V_{S;\,Q})$$



Characteristics

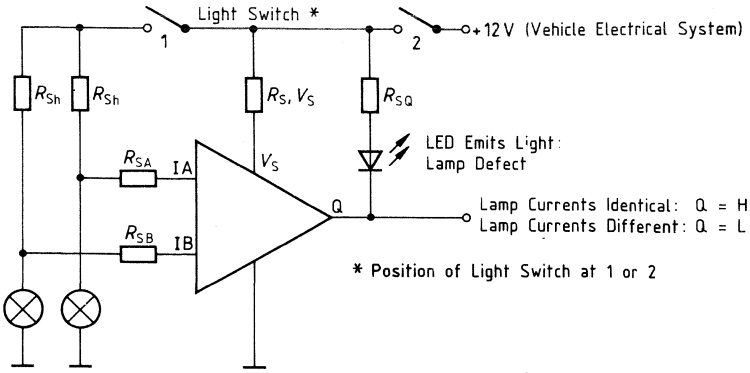
$T_A = -30\,°C$ to $110\,°C$; $V_S = 10$ to $16\,V$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
Current consumption	I_S			3 8	mA mA	Q1=Q2=Q3=Q4=H Q1=Q2=Q3=Q4=L	1
Switching threshold							
with $R_{SA,B}$	V_{Diff}[1]	7	14	20	mV	$V_S = 13.5\,V$, $R_S = 1\,k\Omega$	2
without $R_{SA,B}$	V_{Diff}[1]	4	8	12	mV	$V_S = 13.5\,V$	1
with $R_{SA,B}$	V_{Diff}	2		14	mA	$4.5\,V < V_S < 5.5\,V$, $R_S = 1\,k\Omega$	2
without $R_{SA,B}$	V_{Diff}	1.5		8	mV	$4.5\,V < V_S < 5.5\,V$	1
Input current	$I_{A,B}$			25	µA	$V_A = V_B$	1
Output saturation voltage	V_{QL}			0.4	V	$I_Q = 30\,mA$	1
Output reverse current	I_{QH}			10	µA	$V_{QH} = 32\,V$	1

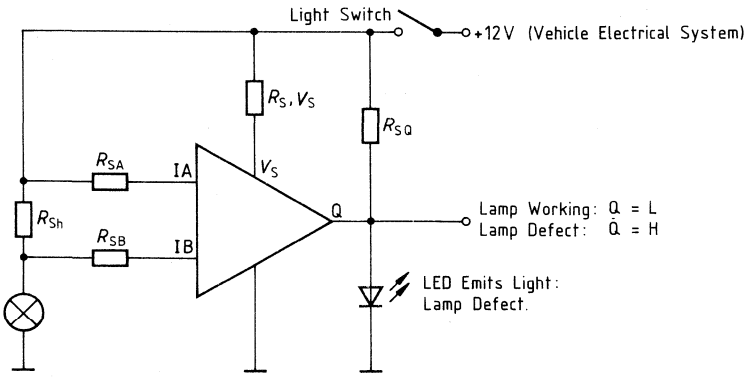
[1] $V_{Diff} = |V_A - V_B|$

Application Circuits

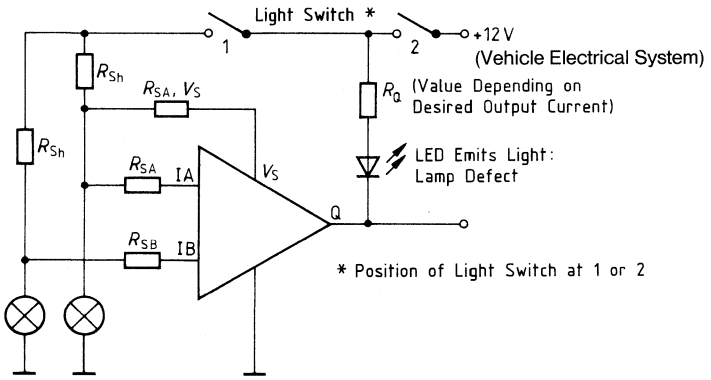
1. Differential measurement



2. Absolute-value measurement

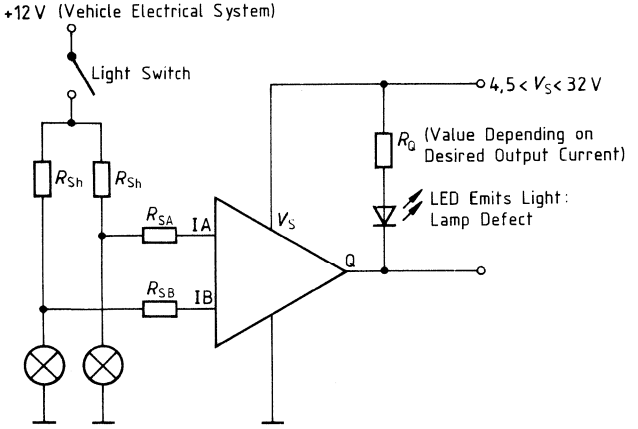


3. Supply from shunt resistor (function as "1": Differential measurement)



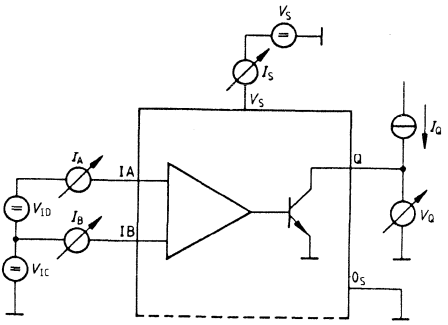
Recommended Protective Resistors: $R_{SA,B} = 1\,k\Omega$
$R_{SA}, V_S = 100\,\Omega$

4. Voltage supply separated from vehicle electrical system
(function as "1": Differential measurement)

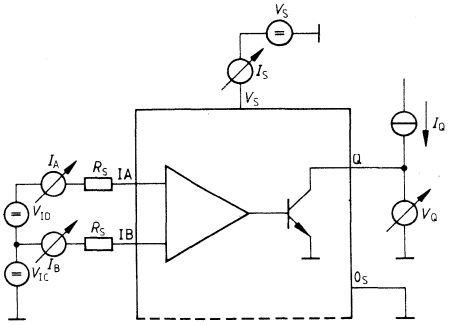


Recommended Protective Resistors : $R_{SA,B} = 1\,k\Omega$

Test Circuit 1

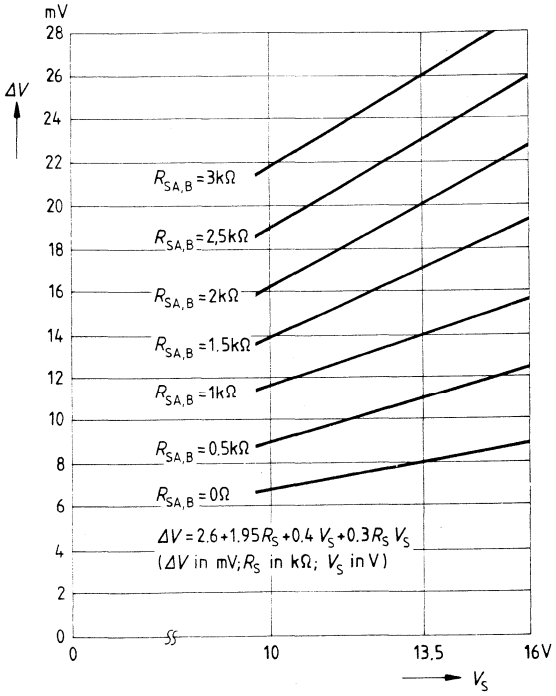


Test Circuit 2



Differential switching voltage versus supply voltage

Parameters: protective resistors at the inputs $R_{SA,B}$



Selector Guide

Type	Package	Operating range (V)	Temperature range (°C)	Max. frequency (kHz)	Undervoltage shut-down	Reset signal	Supply current (mA) typ.	Driver outputs	Max. output current (mA)	Standby	Current limitation	Page
PWM Control												
TDA 4700	C-DIP-24	11 to 30	–25 to 85	100	●		12	2	70		●	188
TDA 4700 A	P-DIP-24	10.5 to 30	0 to 70	100	●		12	2	70		●	188
TDA 4718	C-DIP-18	11 to 30	–25 to 85	100	●		12	2	70		●	188
TDA 4718 A	P-DIP-18	10.5 to 30	0 to 70	100	●		12	2	70		●	188
TDA 4716 C	P-DIP-16	10.5 to 30	–25 to 85	100	●		12	2	70		●	203
TDA 4714 C	P-DIP-14	10.5 to 30	–25 to 85	100	●		12	2	70		●	203
TDA 4918 A	P-DIP-20	10 to 30	–40 to 85	300	●		12	2	+700 −500	●	●	236
TDA 4918 G	P-DSO-20	10 to 30	–40 to 85	300	●		12	2	+700 −500	●	●	236
TDA 4919 A	P-DIP-20	10 to 30	–40 to 85	300	●		12	1	+700 −500	●	●	236
TDA 4919 G	P-DSO-20	10 to 30	–40 to 85	300	●		12	1	+700 −500	●	●	236
Sinusoidal Line-Current Control												
TDA 4814 A	P-DIP-14	11.2 to 17	–25 to 85		●		5	1	400	●	●	216
TDA 4816 G	P-DSO-16	11.2 to 17	–25 to 85		●		5	1	400	●	●	216
TDA 4817	P-DIP-8	11.2 to 17	–25 to 85		●		5	1	400	●	●	229
TDA 4817 G	P-DSO-8	11.2 to 17	–25 to 85		●		5	1	400	●	●	229
5 V Low-Drop Voltage Regulators												
TLE 4258	P-T66-7-H	6 to 24	–40 to 150[1]			●	2[2]	2	750	●	●	255
TLE 4260	P-T66-5-H	6 to 32	–40 to 150[1]			●	500 µA[2]	1	500	●	●	265
TLE 4261	P-T66-7-H	6 to 32	–40 to 150[1]			●	50 µA[2]	1	500	●	●	275

= SMD

[1] T_j = Junction temperature
[2] Standby current

Control ICs for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

The TDA 47xx family of control ICs for SMPS consists of four basic types that, in line with the particular application, will enable optimal adaptation to the SMPS concept that is called for. These devices include all the important basic functions that are expected of a modern SMPS, such as feed-forward control, soft start, dynamic current limitation, error comparators, reference-voltage source, undervoltage shut-down and push-pull open-collector outputs.

The 4714 C is the most economic version. TDA 4700 A is the version with the widest range of functions.

The following table gives an overview over the four basic types.

Features \ Type	TDA 4700	TDA 4718	TDA 4716	TDA 4714
Undervoltage Protection	●	●		
External Synchronization	●	●		
On Chip General Purpose OP AMP	●		●	
Overvoltage Protection with Lock-up Option	●	●	●	●
Symmetric Inputs	●			
Dynamic Current Limiting	●	●	●	●
Feed-Forward Control	●	●	●	●
Double Pulse Suppression	●	●	●	●
Soft Start	●	●	●	●
V_S Undervoltage Protection	●	●	●	●

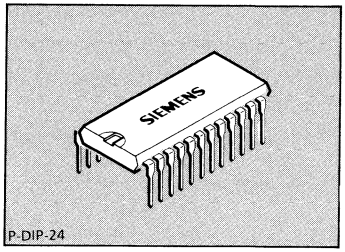
SIEMENS

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

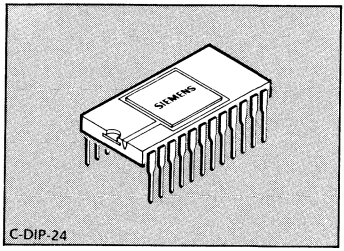
TDA 4700
TDA 4718

Features

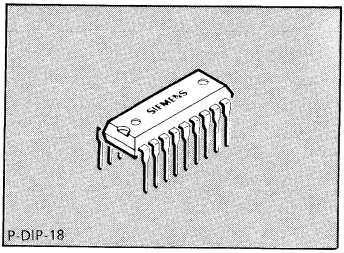
- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter (TDA 4700)
- Push-pull outputs
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression



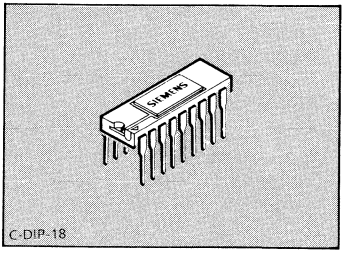
P-DIP-24



C-DIP-24



P-DIP-18

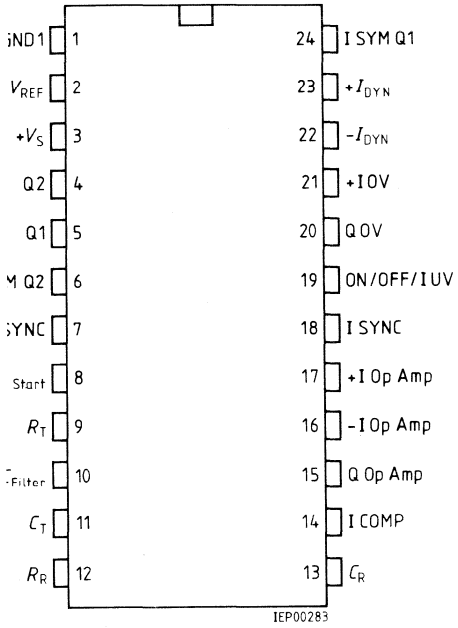


C-DIP-18

	Type	Ordering Code	Package	Temp.-Range
	TDA 4700	Q67000-Y595	C-DIP-24	−25 to 85 °C
S	TDA 4700 A	Q67000-Y594	P-DIP-24	− 0 to 70 °C
S	TDA 4718	Q67000-Y638	C-DIP-18	−25 to 85 °C
S	TDA 4718 A	Q67000-Y639	P-DIP-18	− 0 to 70 °C

These versatile SMPS control ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

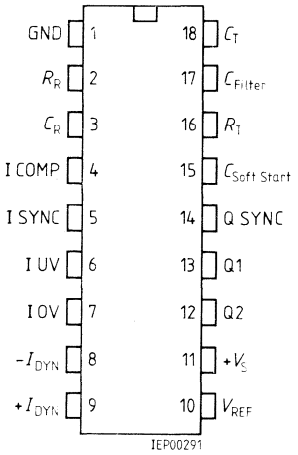
Pin Configuration (TDA 4700)
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2	$+V_{REF}$	Reference voltage
3	$+V_S$	Supply voltage
4	Q2	Output Q2
5	Q1	Output Q1
6	I SYM Q2	Symmetry Q2
7	Q SYNC	Sync. output
8	$C_{soft\ start}$	Soft start
9	R_T	VCO R_T
10	C_{filter}	Capacitance
11	C_T	VCO C_T
12	R_R	Ramp generator R_R
13	C_R	Ramp generator C_R
14	I COMP	Comparator input
15	Q Op Amp	Operational amplifier output
16	−I Op Amp	Operational amplifier input (−)
17	+I Op Amp	Operational amplifier input (+)
18	I SYNC	Sync. input
19	ON/OFF/IUV	ON/OFF, undervoltage
20	QOV	Overvoltage output
21	IOV	Overvoltage input
22	$-I_{DYN}$	Dynamic current limitation (−)
23	$+I_{DYN}$	Dynamic current limitation (+)
24	I SYM Q1	Symmetry

Pin Configuration (TDA 4718)
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2	R_R	Ramp generator R_R
3	C_R	Ramp generator C_R
4	I COMP	+ input comparator K2
5	I SYNC	Sync. input
6	I UV	Input undervoltage, ON/OFF
7	I OV	Input overvoltage
8	$-I_{DYN}$	Input dynamic current limitation (–)
9	$+I_{DYN}$	Input dynamic current limitation (+)
10	V_{REF}	Reference voltage
11	$+V_S$	Supply voltage
12	Q2	Output Q2
13	Q1	Output Q1
14	Q SYNC	Sync. output
15	$C_{soft\ start}$	Soft start
16	R_T	VCO R_T
17	C_{filter}	Capacitance
18	C_T	VCO C_T

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K 2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1 (TDA 4700; A)

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse-Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K 3

Comparator K3 limits the voltage at capacitance $C_{soft\ start}$ (and also at K2) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K 4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error Flipflop

Error signals which are routed to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

The K7 common-mode range covers 0 V to +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry (TDA 4700; A)

In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

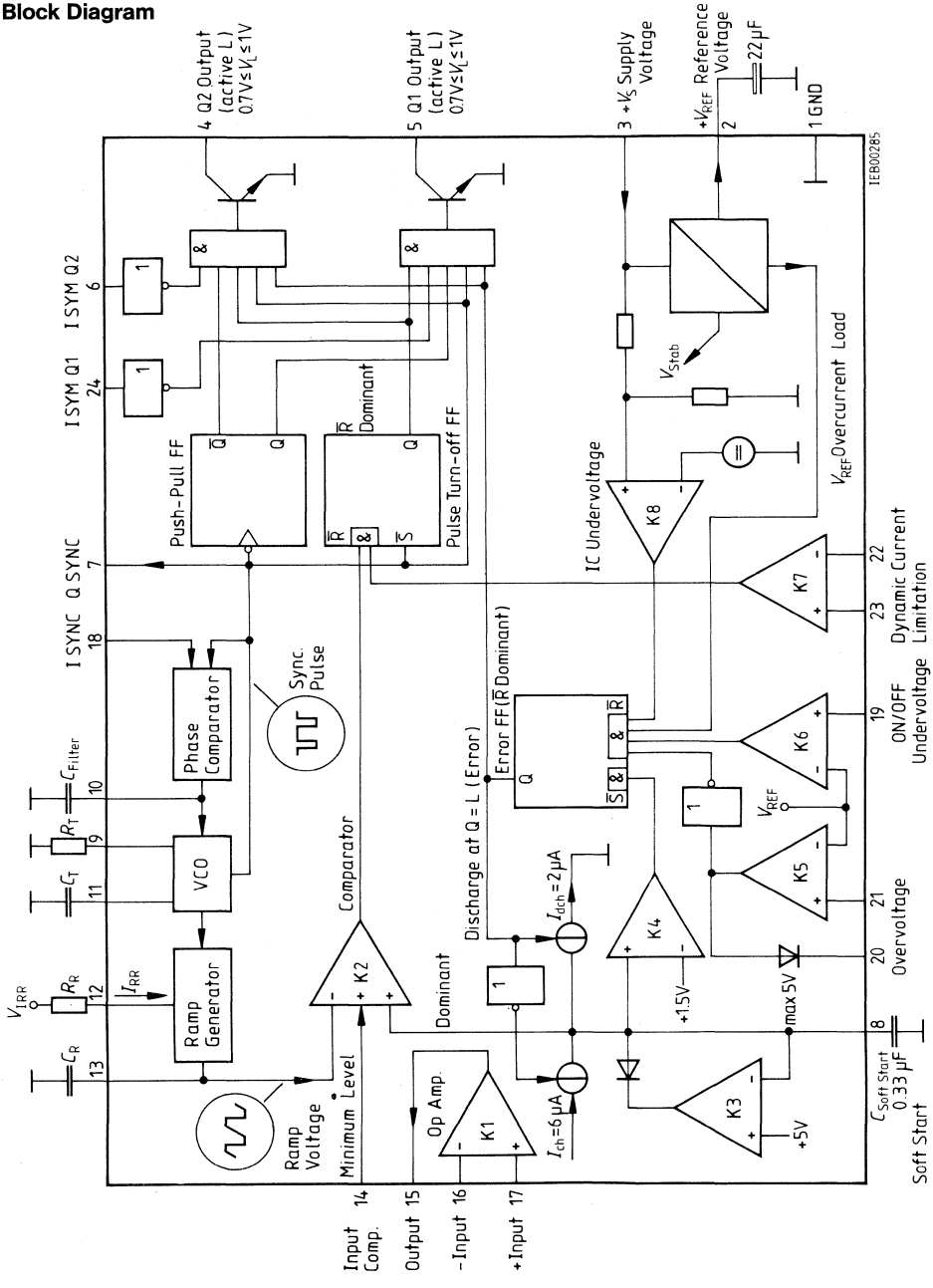
Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

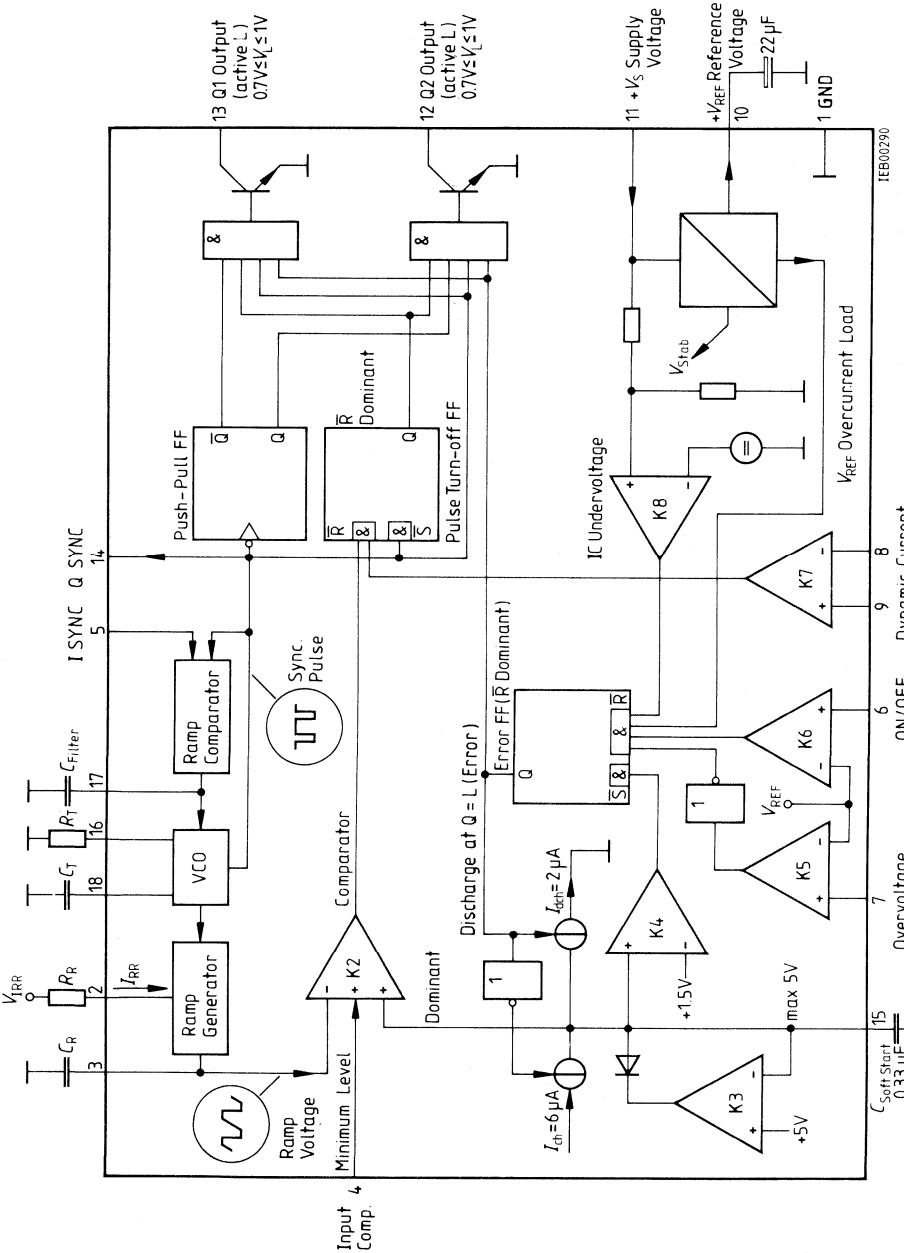
Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Block Diagram



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Supply voltage	V_S	−0.3	33	V	
Voltage at Q1, Q2	V_Q	−0.3	33	V	Q1, Q2 HIGH
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 LOW
Symmetry 1, 2 TDA 4700; A	V_{SYM}	−0.3	33	V	
Sync output	$V_{SYNC\ Q}$	−0.3	7	V	SYNC Q HIGH
	$I_{SYNC\ Q}$	0	10	mA	SYNC Q LOW
Sync input	$V_{SYNC\ I}$	−0.3	33	V	
Input C_{filter}	$V_{I\ Cf}$	−0.3	7	V	
Input R_T	$V_{I\ RT}$	−0.3	7	V	
Input C_T	$V_{I\ CT}$	−0.3	7	V	
Input R_R	$V_{I\ RR}$	−0.3	7	V	
Input C_R	$I_{I\ CR}$	−10	10	mA	
Input comparator K2, K5, K6, K7	$V_{I\ K}$	−0.3	33	V	
Output K5	$V_{Q\ K5}$	−0.3	33	V	
Input op amp TDA 4700; A	$V_{I\ Op\ Amp}$	−0.3	33	V	
Output op amp TDA 4700; A	$V_{Q\ Op\ Amp}$	−0.3	V_S-1	V	
			max. 7	V	
Reference voltage	V_{REF}	−0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\ soft\ start}$	−0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance system – air TDA 4700; A	$R_{th\ SA}$		65	K/W	
TDA 4718	$R_{th\ SA}$		70	K/W	
TDA 4718 A	$R_{th\ SA}$		60	K/W	

Operating Range

Supply voltage	V_S	10.5	30	V	
Ambient temperature TDA 4700; TDA 4718	T_A	−25	85	°C	
TDA 4700A; TDA 4718A	T_A	0	70	°C	
VCO frequency	f	40	250000	Hz	
Ramp generator frequency	f_{RG}	40	250000	Hz	

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply current	I_S	8		20	mA	$C_T = 1$ nF, $f_{VCO} = 100$ kHz
Reference						
Reference voltage	V_{REF}	2.35	2.5	2.65	V	0 mA < I_{REF} < 5 mA
Reference voltage change	ΔV_{REF}		8		mV	14 V ± 20%
Referenve voltage change	ΔV_{REF}		15		mV	25 V ± 20%
Reference voltage change	ΔV_{REF}			15[1]	mV	0 mA < I_{REF} < 5 mA
Temperature coefficient	TC		0.25	0.4	mV/K	
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA	
Oscillator (VCO)						
Frequency range	f_{VCO}	40		100 000	Hz	
Frequency change	$\Delta f/f_{VCO}$		0.5		%	14 V ± 20%
Frequency change	$\Delta f/f_{VCO}$	−1		1	%	25 V ± 20%
Tolerance	$\Delta f/f_{VCO}$	−7		7	%	$\Delta R_T = 0$, $\Delta C_T = 0$
Fall time sawtooth	t		1		µs	$C_T = 1$ nF
	t		10		µs	$C_T = 10$ nF
RC combination	C_T	0.82		47	nF	
VCO	R_T	5		700	kΩ	
Ramp Generator						
Frequency range	f	40		100 000	Hz	
Maximum voltage at C_R	V_H		5.5		V	
Minimum voltage at C_R	V_L		1.8		V	
Input current through R_R	I_{RR}	0		400	µA	
Current transformation ratio	I_{RR}/I_{CR}		1/4			
Synchronization						
Sync output	$V_{Q\,H}$	4			V	$I_{Q\,H} = -200$ µA
	$V_{Q\,L}$			0.4	V	$I_{Q\,L} = 1.6$ mA
Sync input	$V_{I\,H}$	2			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			5	µA	
Comparator K2						
Input current	$-I_{I\,K2}$			2	µA	
Turn-off delay[2]	$t_{D\,OFF}$			500	ns	
Input voltage	$V_{I\,K2}$					for duty cycle
			1.8		V	$D = 0$
			5		V	D = max.
Common-mode input voltage range	$V_{I\,C}$	0		5.5	V	

[1] At $T_A = 0\,°C$ to $70\,°C$, this value falls to max. 5 mV.
[2] At the input: step function $\Delta V = -100$ mV ⇌ $\Delta V = +100$ mV

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}		6		µA	
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA	
Upper limiting voltage	V_{lim}		5		V	
Switching voltage K4	V_{K4}		1.5		V	
Operational Amplifier K1 (TDA 4700; TDA 4700 A)						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	−10		10	mV	
Temperature coefficient of V_{IO}	TC	−30		30	µV/K	
Input current	$-I_I$			2	µA	
Common-mode input voltage range	V_{IC}	0		5	V	
Output current	I_Q	−3		1.5	mA	
Rise time of output voltage	$\Delta V/\Delta t$		1		V/µs	
Transition frequency	f_T		3		MHz	
Phase at f_T	φ_T		120		deg.	
Output voltage	$V_{Q\,H/L}$	1.5		5.5	V	$-3\ mA < I < 1.5\ mA$
Symmetry (TDA 4700; TDA 4700 A)						
Input voltage	$V_{I\,H}$	2.0			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			2	µA	
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$			30	V	
	$V_{Q\,L}$			1.1	V	$I_Q = 20$ mA
Output leakage current	I_Q			2	µA	$V_{Q\,H} = 30$ V
ON, OFF, Undervoltage K6						
Switching voltage	V	V_{REF}-0.03mV		V_{REF}+0.03mV	V	
Input current	$-I_I$			2	µA	
Turn-off delay time[1])	$t_{D\,OFF}$		250		ns	
Error detection time[1])	t		50		ns	

[1]) At the input: step function $V_{REF} = -100$ mV ⇀↽ $V_{REF} = +100$ mV

Characteristics

V_S = 11 to 30 V; T_A = −25 °C to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}	0		4	V	
Input offset voltage	V_{IO}	−10		10	mV	
Input current	$-I_I$			2	µA	
Turn-off delay time[2])	$t_{D\ OFF}$		250		ns	
Error detection time)	t		50		ns	
Overvoltage K5						
Switching voltage	V	V_{REF}-0.03mV		V_{REF}+0.03mV	V	
Input current	$-I_I$			2	µA	
Output current	$-I_Q$	0		200	µA	V_{QHmin} = 5 V
Turn-off delay time[1])	$t_{D\ OFF}$		250		ns	
Error detection time[1])	t		50		ns	
Supply Undervoltage						
Turn-on threshold for V_S rising	V_S	8.8		11 10.5	V V	0 °C < T_A < 70 °C
Turn-off threshold for V_S falling	V_S	8.5		10.5 10	V V	0 °C < T_A < 70 °C
Input C_{filter}						
Rated voltage for rated frequency	V_R		4		V	
Frequency approx. proportional to voltage within the range	V_R	3		5	V	
Voltage at open sync input	$V_{c\ filter}$		1.6		V	

[1]) At the input: step function V_{REF} = −100 mV ⌟→ V_{REF} = +100 mV
[2]) At the input: step function ΔV = −100 mV ⌟→ ΔV = +100 mV

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

5. In the case of a free-running VCO: connect sync output with sync input.

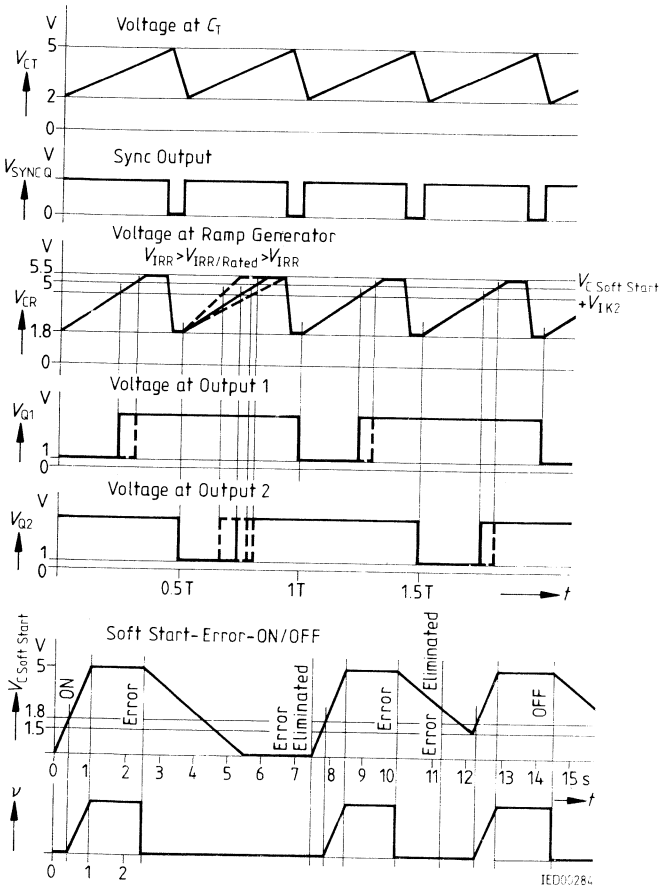
6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2. (TDA 4700; TDA 4700A)

7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

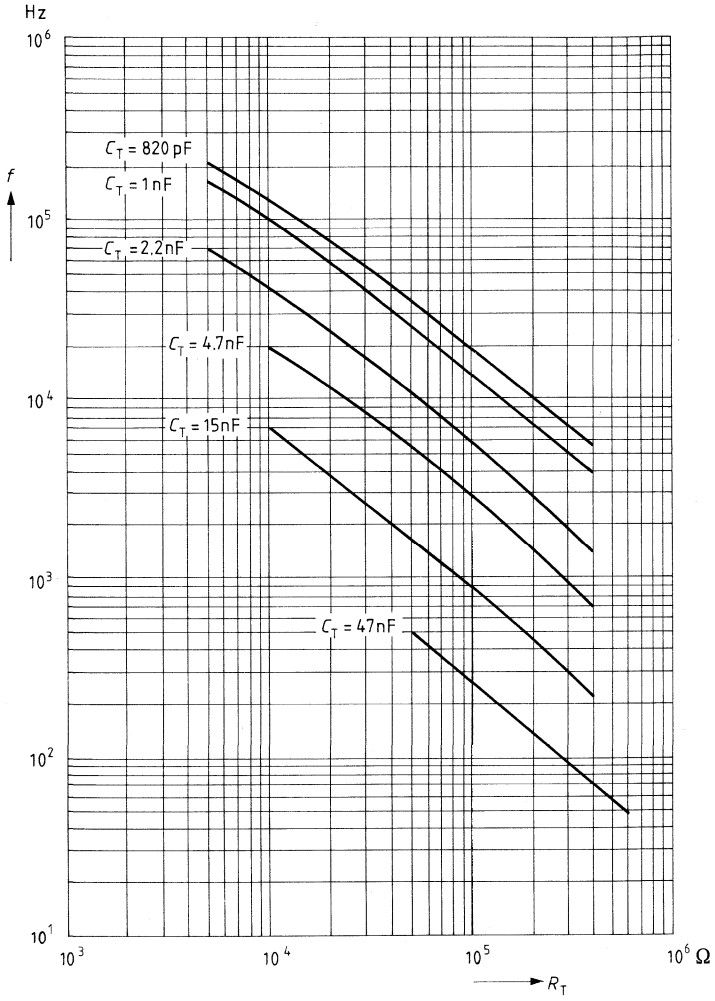
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

Pulse Diagram



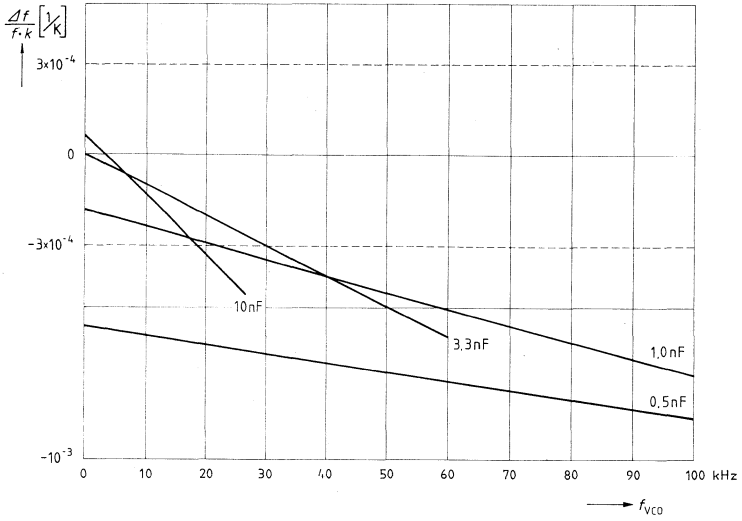
VCO frequency versus R_T and C_T.



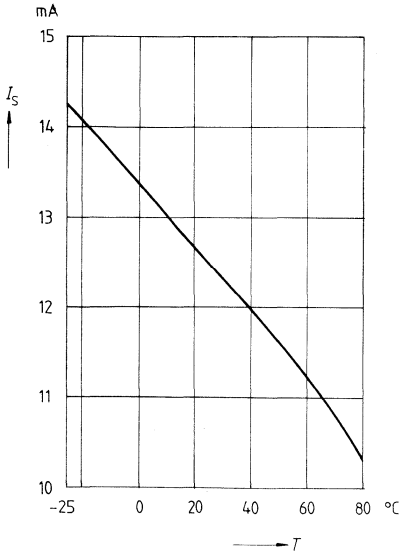
VCO temperature response

$V_S = 12$ V; D = max.

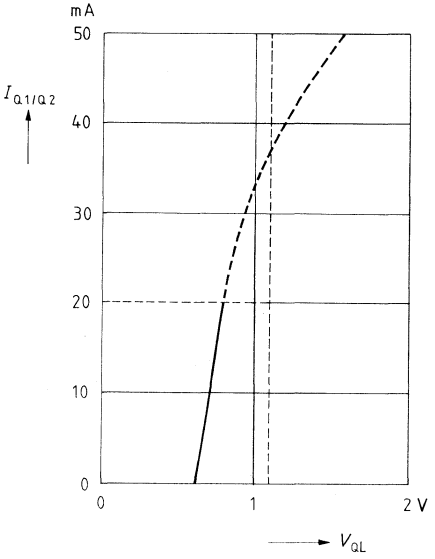
$\frac{\Delta f_{VCO}}{f_K \times K}$ $\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



SIEMENS

IC for Switched-Mode Power Supplies (SMPS)

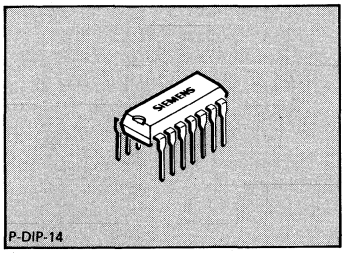
TDA 4714 C
TDA 4716 C

Bipolar IC

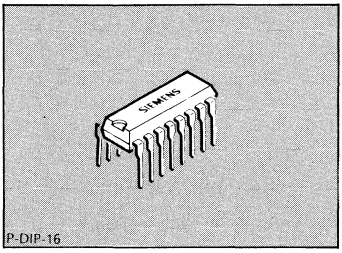
3

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source
- Reference overload protection
- Soft start
- Feed-forward control
- Operational amplifier (TDA 4716 C)



P-DIP-14



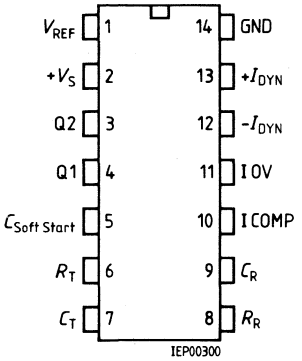
P-DIP-16

Type	Ordering Code	Package	Temp.-Range
TDA 4714 C	Q67000-A8312	P-DIP-14	−25 to 85 °C
TDA 4716 C	Q67000-A8313	P-DIP-16	−25 to 85 °C

These versatile SMPS ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The components can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps which activate protective functions.

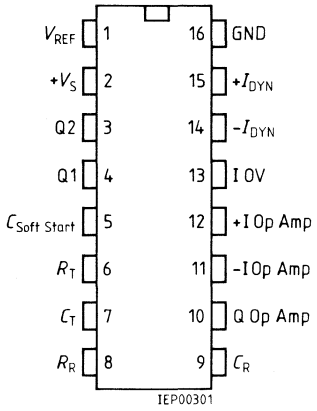
Pin Configuration
top view

TDA 4714 C



Pin Configuration
top view

TDA 4716 C



Pin Definitions and Functions (TDA 4714 C)

Pin	Symbol	Function
1	V_{REF}	Reference voltage
2	$+V_S$	Supply voltage
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	I COMP	Input comparator
11	I OV	Inpot overvoltage
12	$-I_{DYN}$	Dynamic current limitation (–)
13	$+I_{DYN}$	Dynamic current limitation (+)
14	GND	Ground

Pin Definitions and Functions (TDA 4716 C)

Pin	Symbol	Function
1	V_{REF}	Reference voltage V_{REF}
2	V_S	Supply voltage V_S
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	Q op amp	Operational amplifier output
11	–I op amp	Operational amplifier input (–)
12	+I op amp	Operational amplifier Input (+)
13	I OV	Input overvoltage
14	$-I_{DYN}$	Dynamic current limitation (–)
15	$+I_{DYN}$	Dynamic current limitation (+)
16	GND	Ground

Circuit Description

The following is a description of the individual functional units and their interaction.

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a DC voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1 (TDA 4716C)

The op amp K1 is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage of capacitance $C_{soft\ start}$ (and also at K2!) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA at the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again by the soft start.

Comparator K5, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again by the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the operational amplifier have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

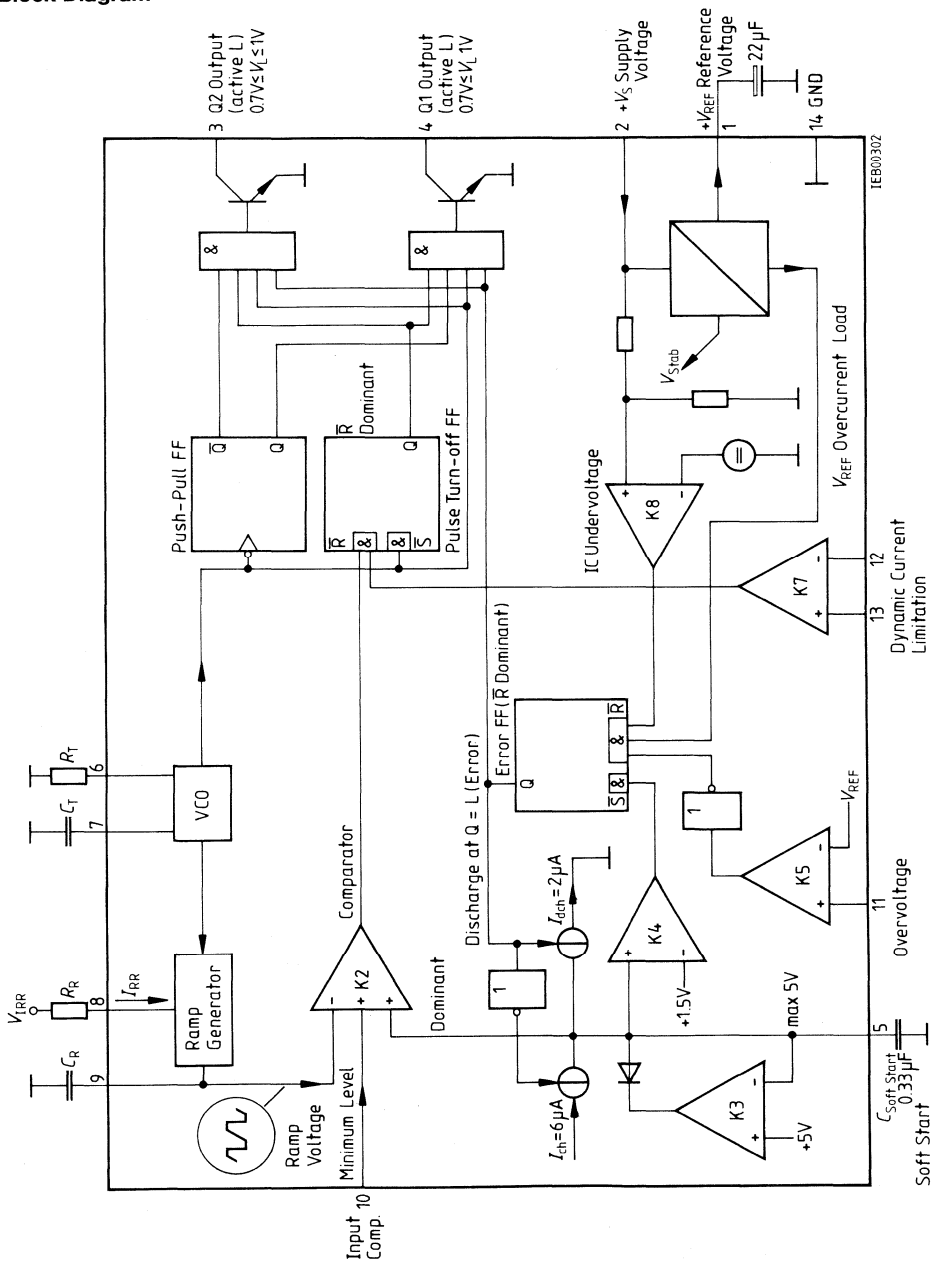
Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

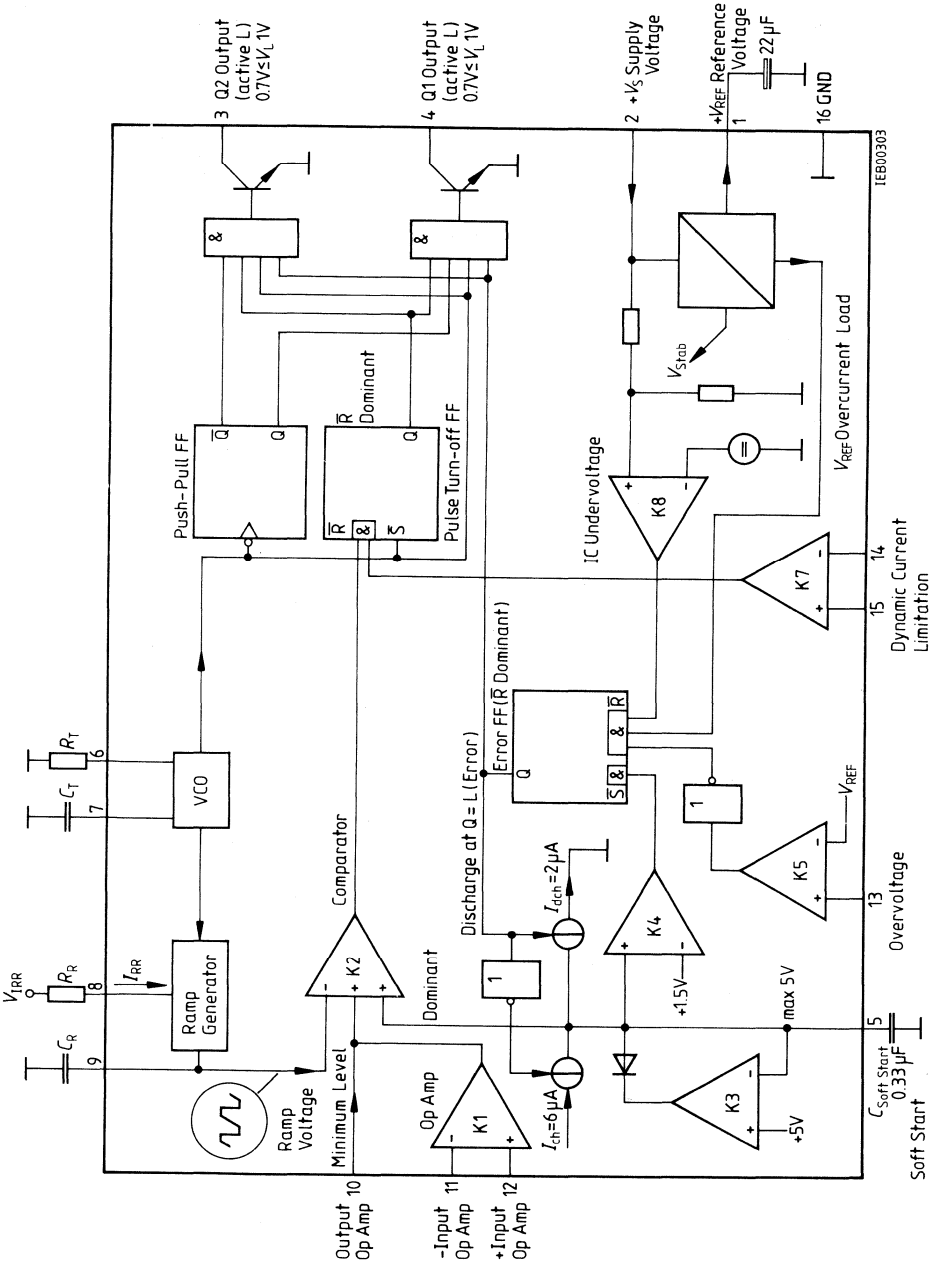
Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Block Diagram



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Supply voltage	V_S	−0.3	33	V	
Voltage at Q1, Q2	V_Q	−0.3	33	V	Q1, Q2 HIGH
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 LOW
Input R_T	$V_{I\,RT}$	−0.3	7	V	
Input C_T	$V_{I\,CT}$	−0.3	7	V	
Input R_R	$V_{I\,RR}$	−0.3	7	V	
Input C_R	$I_{I\,CR}$	−10	10	mA	
Input comparator K2, K5, K7	$V_{I\,K2,5,7}$	−0.3	33	V	
Output K5	$V_{Q\,K5}$	−0.3	33	V	
Input op amp TDA 4716 C	$V_{I\,Op\,Amp}$	−0.3	33	V	
Output op amp TDA 4716 C	$V_{Q\,Op\,Amp}$	−0.3	V_S−1 max. 7 V	V	
Reference voltage	$V_{Q\,REF}$	−0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\,soft\ start}$	−0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance system – air	$R_{th\,SA}$		70	K/W	

Operating Range

Supply voltage	V_S	10.5	30	V	
Ambient temperature	T_A	−25	85	°C	
Frequency	f	40	100	kHz	
VCO frequency	f_{VCO}	40	250	kHz	
Ramp generator frequency	f_{RG}	40	250	kHz	

Characteristics

11 V < V_S < 30 V; −25 °C < T_A < 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Supply current C_T = 1 nF f_{VCO} = 100 kHz	I_S	8		20	mA
Reference					
Reference voltage, T_A = 25 °C I_{REF} = 1 mA, V_S = 12 V	V_{REF}	2.475	2.500	2.525	V
Voltage change V_S = 14 V ± 20%	ΔV_{REF}		8		mV
Voltage change V_S = 25 V ± 20%	ΔV_{REF}		15		mV
Voltage change[1] 0 mA < I_{REF} < 5 mA	ΔV_{REF}			15	mV
Temperature coefficient	TC		0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA
Oscillator (VCO)					
Frequency range	f	40		100	kHz
Frequency change V_S = 14 V ± 20%	$\Delta f/f$		0.5		%
Frequency change V_S = 25 V ± 20%	$\Delta f/f$	−1		1	%
Tolerance ΔR_T = 0; ΔC_T = 0	$\Delta f/f$	−7		7	%
Fall time sawtooth					
C_T = 1 nF			1		µs
C_T = 10 nF			10		µs
RC combination	C_T	0.82		47	nF
VCO	R_T	5		700	kΩ
Ramp Generator					
Frequency range	f_{RG}	40		100	kHz
Maximum voltage at C_R	V_H		5.5		V
Minimum voltage at C_R	V_L		1.8		V
Input current through R_R	I_{RR}	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4		

[1]) Between 0 °C and 70 °C ambient temp. ΔV_{REF} is reduced to max. 5 mV.

Characteristics

11 V < V_S < 30 V; −25 °C < T_A < 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Comparator K2					
Input current	$-I_{K2}$			2	µA
Turn-off delay time[1])	$t_{D\ OFF}$			500	ns
Input voltage	$V_{I\ K2}$				
Duty cycle $D = 0$			1.8		V
D = max			5		V
Common-mode input voltage range	V_{IC}	0		5.5	V
Soft Start K3, K4					
Charge current for $C_{soft\ start}$	I_{ch}		6		µA
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA
Upper limiting voltage	V_{lim}		5		V
Switching voltage K4	V_{K4}		1.5		V
Operational Amplifier (TDA 4716 C)					
Open-loop voltage gain	G_{V0}	60	80		dB
Input offset voltage	V_{IO}	−10		10	mV
Temperature coefficient of V_{IO}	TC	−30		30	µV/K
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		5	V
Output current	I_Q	−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$		1		V/µs
Transition frequency	f_T		3		MHz
Phase at f_T	φ_T		120		degr.
Output voltage −3 mA < I < 1.5 mA	$V_{Q\ H/L}$	1.5		5.5	V
Output Stages Q1, Q2					
Output voltage I_Q = 20 mA	V_{QH}			30	V
	V_{QL}			1.1	V
Output leakage current V_{QH} = 30 V	I_Q			2	µA

[1]) At the input: step function $\Delta V = -100$ mV → $\Delta V = +100$ mV

Characteristics

11 V < V_S < 30 V; −25 °C < T_A < 85 °C

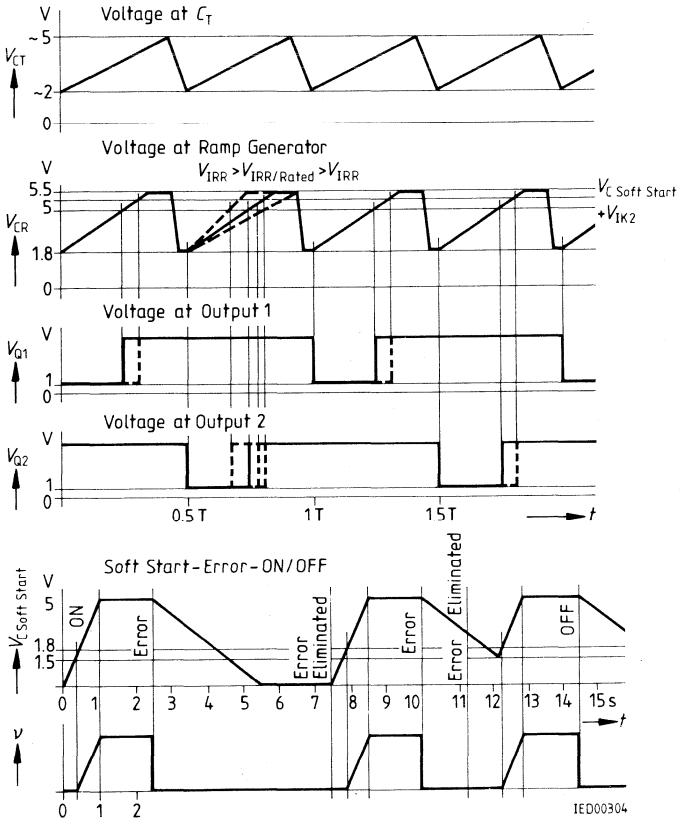
Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Dynamic Current Limitation K7					
Common-mode input voltage range	V_{IC}	0		4	V
Input offset voltage	V_{IO}	−10		10	mV
Input current	$-I_I$			2	µA
Turn-off delay time[2]	$t_{D\ OFF}$		250		ns
Error detection time[2]	t		50		ns
Overvoltage K5					
Switching voltage	V	V_{REF}−0.03		V_{REF}+0.03	V
Input current	$-I_I$			2	µA
Turn-off delay time[1]	$t_{D\ OFF}$		250		ns
Error detection time[1]	t		50		ns
Supply Undervoltage					
Turn-on threshold for V_S, rising	V_S	8.8		11	V
Turn-on threshold for V_S, rising (0 °C < T_A < 70 °C)	V_S			10.5	V
Turn-off threshold for V_S, falling	V_S	8.5		10.5	V
Turn-on threshold for V_S, falling (0 °C < T_A < 70 °C)	V_S			10	V

[1]) At the input: step function $V_{REF} = -100$ mV ⌐→ $V_{REF} = +100$ mV
[2]) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

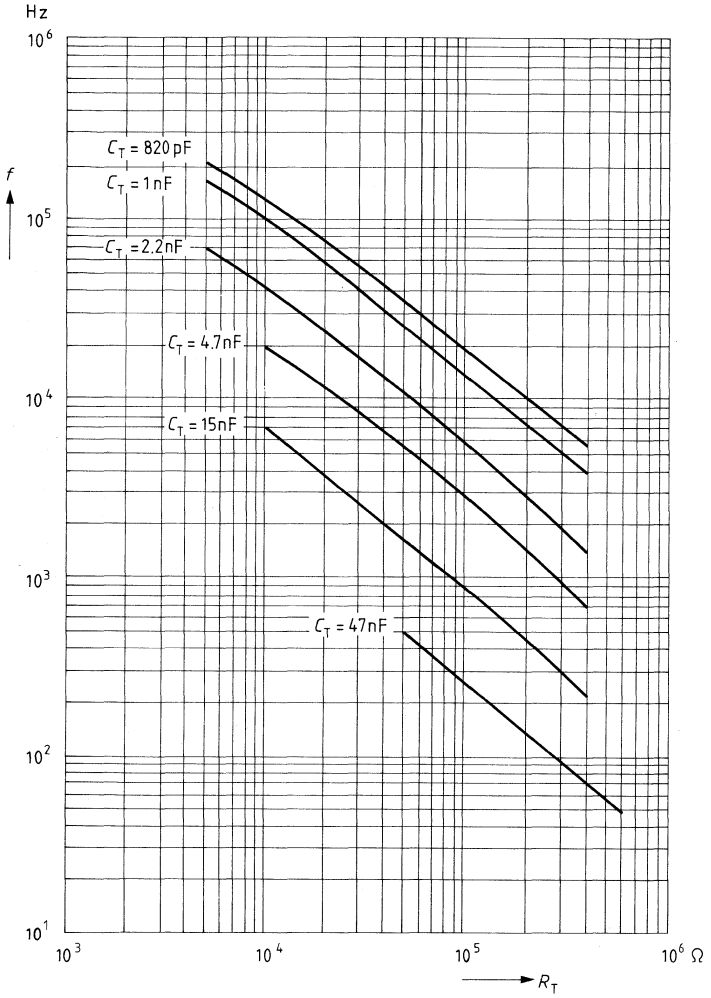
Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$
5. Wiring of the operational amplifier according to the dynamic requirements (TDA 4716 C).

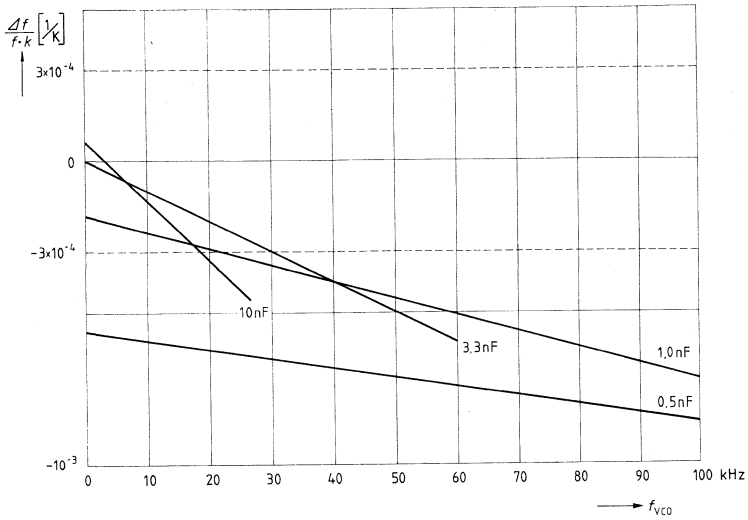
Pulse Diagram



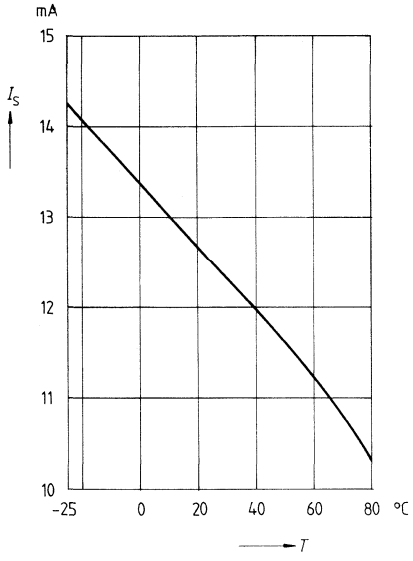
VCO frequency versus R_T and C_T



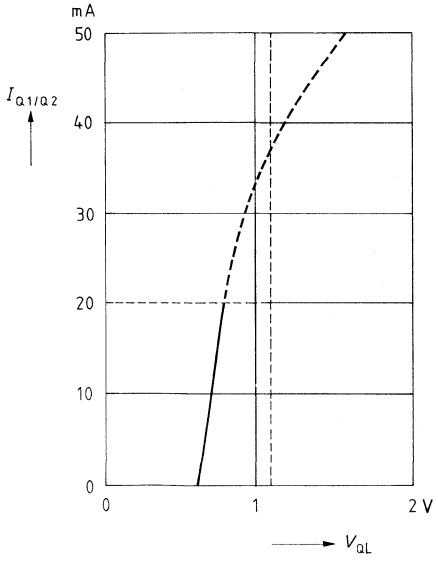
VCO temperature response
$V_S = 12$ V; D = max.
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



SIEMENS

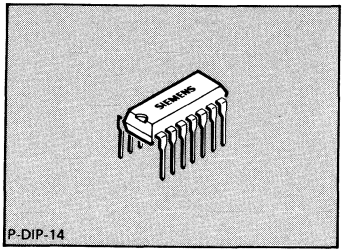
IC for Sinusoidal Line-Current Consumption

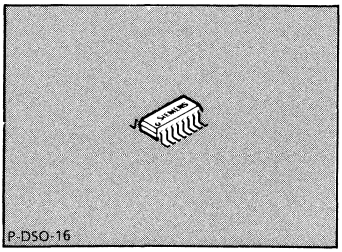
TDA 4814 A
TDA 4816 G

Bipolar IC

Features

- Excellent sinewave current simulation
- Power factor approaching 1
- Direct drive of SIPMOS transistors
- Zero crossing detector
- 110/220 V AC operation without switchover
- Standby current consumption of 0.5 mA
- Start/stop monitoring circuit for lamp generators





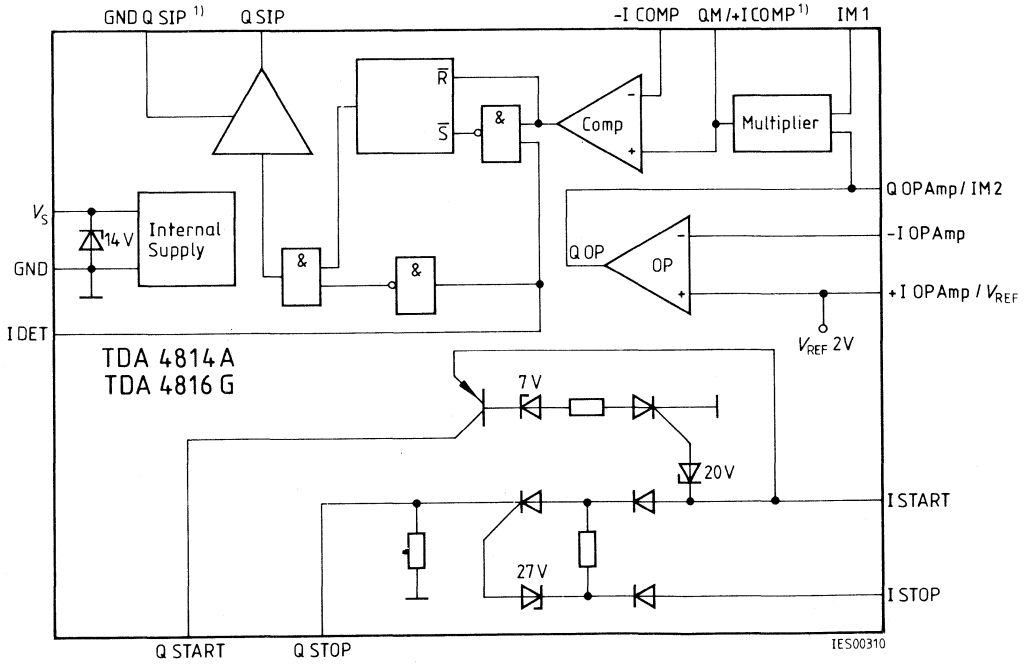
Type	Ordering Code	Package	Temp.-Range
S TDA 4814 A	Q67000-A8163	P-DIP-14	−25 to 85 °C
TDA 4816 G	Q67000-A8290	P-DSO-16 (SMD)	−25 to 85 °C

These devices contain components for designing a switch-mode power supply with sinusoidal line-current consumption. Sinusoidal line current is drawn from the supply network in particular when there is high power consumption. One possible application is in electronic ballasts for fluorescent lamps, especially when a large number of these lamps are concentrated on one supply point. These ICs are additionally suitable for general driving of switch-mode power supplies. The possibility of regulating the output voltage will enable operation on different line voltages (110 V AC/220 V AC) without any switchover.

A monitoring circuit makes it possible to control various turn-on and turn-off functions of different units of equipment.

With the TDA 4816 G, the features of the TDA 4814 A have been extended. Compared to the TDA 4814 A, the TDA 4816 G comes in a P-DSO-16 package, and its multiplier output QM is led through, which is an additional advantage in fixed-frequency applications. The PCB layout has been made less complicated by implementing a separate driver grounding (GND QSIP).

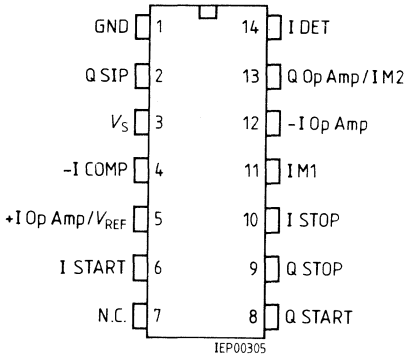
Block Diagram



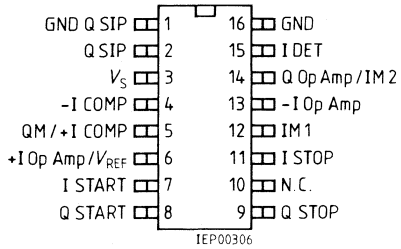
1) TDA 4816 G only

Pin Configuration
(top view)

P-DIP-14



P-DSO-16



Pin Definitions and Functions

Pin No.			
P-DIP-14	**P-DSO-16**	**Symbol**	**Function**
–	1	GND QSIP	Driver Ground
1		GND	Ground
2	2	QSIP	Driver output
3	3	V_S	Supply voltage
4	4	–ICOMP	Negative comparator input
–	5	QM/+ICOMP	Multiplier output/positive comparator input
5	6	+I OP Amp/V_{REF}	Positive input/reference voltage
6	7	I START	Start input
7	10	N.C.	Not connected
8	8	Q START	Start output
9	9	Q STOP	Stop output
10	11	I STOP	Stop input
11	12	I M1	Multiplier input M1
12	13	–I OP Amp	Negative input OP amplifier
13	14	QOP Amp/I M2	Op amplifier output and multiplier input M2
14	15	I DET	Detector input
–	16	GND	Ground 0 V

Circuit Description

The IC switches from standby to full current consumption when the turn-on threshold on V_S is exceeded. Turn-off is controlled by hysteresis. The integrated Z-diode limits the voltage on V_S when impressed current is fed.

The operational amplifier can be wired as a control amplifier. It will then compare the divided output voltage V_Q to a reference voltage V_{REF} that is stable with temperature. The output voltage of the op amp that is produced in this way is multiplied by a sine-magnitude voltage in the multiplier (M). At the output of the latter a sine-magnitude voltage then appears that is variable in amplitude. This nominal voltage is applied to the plus input of the comparator. The nominal voltage at the multiplier output can then be compared via the comparator to a voltage derived from the actual line current. The output of the comparator feeds the reference signal via a logic circuit to the driver that switches the SIPMOS transistor. No current gaps must appear in the choke, otherwise the line current would no longer be sinusoidal. To achieve that, the detector input I DET senses when the choke current has fallen to zero after turn-off of the SIPMOS transistor. This ensures that the SIPMOS transistor does not turn on too early and that no current gaps occur.

When the detector input I DET is on high potential, the SIPMOS driver output QD is blocked. At the same time the flipflop can be set by the comparator.

When I DET is low, the Q output is enabled and can be disabled again by the comparator by resetting the flipflop.

Consequently the choke is always currentless when the SIPMOS transistor turns on and no current gaps appear in the choke.

Circuit Description for the TDA 4816G

Operation with a constant frequency and trapezoidal shaped current:

This mode of operation turns on the SIPMOS transistor again, before the free-wheel diode forces the current to become zero. Resulting diode reverse currents cause turn-on losses in the transistor. Therefore, the free-wheel diode should feature the lowest possible reverse recovery time.

In the application circuit only the control amplifier and the multiplier are used. All other necessary functions pertain to the TDA 4919A.

Ground Pins

Between the ground pins GND and GND QSIP, a very close and low-impedance connection is to be established.

Driver Output QSIP for SIPMOS Transistors

The output driver is designed as a push-pull stage. There is a resistor of 10 Ω in series with the output for the purpose of current limiting. Between QSIP and ground there is a resistor of 10 kΩ. This keeps the SIPMOS transistor reliably turned off during standby.

The QSIP output is additionally connected to the supply voltage V_S and to ground by way of diodes.

When the supply voltage to the switch-mode power supply is turned on, the diode towards V_S conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smooting capacitor on V_S. The voltage V_S must not exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode towards ground clamps negative voltages on QSIP to −0.7 V. Capacitive currents produced by voltage incursion on the drain of the SIPMOS transistor are thus able to flow away unhindered.

Reference Voltage (V_{REF})

The reference-voltage source is higly stable with temperature. It can be used if additional, external components are wired.

Monitoring Circuit (I START, I STOP, Q START, Q STOP)

The monitoring circuit guarantees the secure operation of a unit of equipment. Any circuitry that is shut down because of a fault, for instance, cannot be started up again until the monitoring start (I START/Q START) has turned on and a positive voltage pulse has been impressed on Q START.

If there is a defect present, the monitoring stop (I STOP/Q STOP) will turn on and shut down either the entire unit or simply the circuitry that has to be protected. No restart is then possible until the hold current impressed on I START or I STOP has been interrupted (e.g. by a power-down).

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_S	−0.3	V_Z	V	V_Z = Z Voltage
Inputs					
Comparator	$V_{I\ COMP}$	−0.3	33	V	
	$V_{-I\ COMP}$	−0.3	33	V	
Op Amp	$V_{I\ Op\ Amp}$	−0.3	6	V	
	$V_{-I\ Op\ Amp}$	−0.3	6	V	
Multiplier	V_{M1}	−0.3	33	V	
Outputs					
Multiplier	V_{QM}	−0.3	3	V	$V_S > 3$ V
Op Amp	$V_{Q\ Op\ Amp}/I_{M2}$	−0.3	6	V	
Z current V_S GND	I_Z	0	300	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	−0.3	V_S	V	Observe P_{max}
QSIP clamping diodes	$I_{QSIP\ D}$	−10	10	mA	$V_Q > V_S$ or $V_Q < -0.3$ V

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Iput START	$V_{I\ START}$	−0.3	25	V	see characteristics
STOP	$V_{I\ STOP}$	−0.3	33	V	see characteristics
Output START	$V_{Q\ START}$	−10	3	V	
STOP	$V_{Q\ STOP}$	−0.3	6	V	
Detector input	$V_{I\ DET}$	0.9	6	V	
Detector clamping diodes	$I_{I\ DET}$	−10	10	mA	$V_{I\ DET} > 6$ V or $V_{I\ DET} < 0.9$ V
Capacitance at I START to ground	$C_{I\ START}$		150	nF	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance system – air P-DIP-14	$R_{th\ SA}$		65	K/W	
P-DSO-16	$R_{th\ SA}$		100	K/W	

Operating Range

Supply voltage	V_S	$V_{S\ ON}$	V_Z	V	Values for $V_{S\ ON}$, V_Z: see characteristics
Z current	I_Z	0	200	mA	Observe P_{max}
Driver current	$I_{Q\ QSIP}$	−500	500	mA	
Operating temperature	T_A	−25	85	°C	

Characteristics ($V_{S\ ON}$[1]) < V_S < V_Z; T_A = −25 °C to 85 °C)

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Current Consumption					
Without load on driver QSIP and V_{REF}; QSIP LOW					
0 V < V_S < $V_{S\ ON}$	I_S			0.5	mA
$V_{S\ ON}$ < V_S < V_Z	I_S	2.5	5	6.5	mA
Load on QD with SIPMOS gate; dynamic operation 50 kHz V_S = 12 V load on Q = 10 nF	I_S			15	mA
Hysteresis on V_S					
Turn-on threshold for V_S rising	V_{SH}	9.6	10.4	11.2	V
Switching hysteresis	$V_{S\ hy}$	1.0		1.7	V

Characteristics $V_{S\,ON}$[1] $< V_S < V_Z$; $T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Comparator (COMP)					
Input offset voltage	V_{IO}	−10		10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		3.5	V
Operational Amplifier (Op Amp)					
Open-loop voltage gain	G_{V0}	60	80		dB
Input offset voltage	V_{IO}	−30		−10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		3.5	V
Output current	$I_{Q\ Op\ Amp}$	−3		1.5	mA
Output voltage	$V_{Q\ Op\ Amp}$	1.2		4	V
Transition frequency	f_T		2		MHz
Transition phase	φ_T		120		deg.
Output driver (QSIP)					
Output voltage high $I_Q = -10$ mA	V_{QH}	5			V
Output voltage low $I_Q = +10$ mA	V_{QL}			1	V
Output current					
rising edge $C_L = 10$ nF	$-I_Q$	200	300	400	mA
falling edge $C_L = 10$ nF	I_Q	250	350	450	mA
Reference-Voltage Source					
Voltage $0 < I_{REF} < 3$ mA	V_{REF}	1.8	2	2.2	V
Load current	$-I_L$	0		3	mA
Voltage change $10\ V < V_S < V_Z$	ΔV_{REF}			5	mV
Voltage change $0\ mA < I_{REF} < 3$ mA	ΔV_{REF}			20	mV
Temperature response	$\Delta V_{REF}/\Delta T$	−0.5		+0.5	mV/K
Z Diode (V_S − GND)					
Z voltage $I_Z = 200$ mA Observe P_{max}	V_Z	13	15.5	17	V

Characteristics $V_{S\,ON}$[1] $< V_S < V_Z$; $T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Multiplier (M1)					
Quadrant for input voltages			1		qu.
Input voltage M1	V_{M1}	0		1	V
Reference level for M1	$V_{REF\,M1}$		0		V
Input voltage M2	V_{M2}	V_{REF}		$V_{REF}+1$	V
Reference level for M2	$V_{REF\,M2}$		V_{REF}		V
Input current M1, M2	$-I_I$	0		2	µA
Coefficient for output-voltage source	C_Q	0.4	0.6	0.8	I/V
Max. output voltage	$V_{QM\,max}$		1.6		V
Output resistance	R_Q		5		kΩ
Temperature response of output-voltage coefficient	$\Delta TC/C_Q$	−0.3	−0.1	0.1	%/K
Monitoring Circuit					
Input I START					
Turn-on voltage	$V_{I\,ON\,START}$	17	22	26	V
Turn-on current	$I_{I\,ON\,START}$	50	90	130	µA
Turn-off voltage	$V_{I\,OFF\,START}$	2	3.5	5	V
Turn-off current	$I_{I\,OFF\,START}$	70	110	150	µA
Input I STOP*)					
Turn-on voltage	$V_{I\,ON\,STOP}$	27	30	33	V
Turn-on current	$I_{I\,ON\,STOP}$	100	150	200	µA
Turn-off voltage	$V_{I\,OFF\,STOP}$	4.5	6.5	8.5	V
Turn-off current	$I_{I\,OFF\,STOP}$	175	250	320	µA
Transfer I START – Q START					
Output current on Q START					
$V_{START} = 15$ V; $V_{Q\,START} = 2$ V	$-I_{Q\,START}$	400	600	800	mA
Transfer I STOP – Q STOP					
Output current on Q STOP					
$I_{STOP} = 1.5$ mA; $V_{STOP} = 18$ V; $V_{Q\,STOP} = 1.2$ V	$-I_{Q\,STOP}$	0.9	1.2		mA
$I_{STOP} = 0.4$ mA; $V_{STOP} \approx 7$ V; $V_{Q\,STOP} = 1.2$ V	$-I_{Q\,STOP}$	60	150		µA

*) The turn-on voltage of I_{STOP} exceeds the turn-on voltage of I_{START} by at least 3 V.

Characteristics $V_{S\,ON}$[1] $< V_S < V_Z$; $T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Detector (I DET)					
Upper switching voltage for voltage rising (H)	$V_{DET\,H}$	1	1.3	1.6	V
Lower switching voltage for voltage falling (L)	$V_{DET\,L}$	0.95			V
Switching hysteresis	$V_{S\,hy}$	50		300	mV
Input current $0.9\,V < V_{DET} < 6\,V$	$-I_{DET}$		5	10	µA
Clamping-diode current $V_{DET} > 6\,V$ or $V_{DET} < 0.9\,V$	I_{DET}	−3		3	mA
Delay Times					
Input comparator QSIP[3])	t	–	200	500	ns

Explanations

[1]) $V_{S\,ON}$ means that V_{SH} has been exceeded but that the voltage is still greater than $(V_{SH} - V_{S\,hy})$.

[2]) Calculation of the output voltage V_{QM}: $V_{QM} = C \cdot V_{M1}{}^* \cdot V_{M2}{}^*$ in V.
The voltages $V_{M1}{}^*$ and $V_{M2}{}^*$ are referred to the particular reference level.

[3]) Step functions at comparator input $\Delta V_{COMP} = -100\,mV \rightarrow \Delta V_{COMP} = +100\,mV$.

Use and Advantages of TDA 4814 A and TDA 4816 G in SMPS and Electronic Ballasts

1 Switch-Mode Power Supplies

The "active harmonics filter" consists of a rectifier arrangement in a bridge circuit followed by an up-converter. Through a controller action it is possible to draw a virtually sinusoidal current from the single-phase line and produce a regulated dc voltage at the output.

In the case of an SMPS with conventional line rectification it is possible to achieve a power factor (ratio of active power to apparent power) of 0.5 to 0.7. The active harmonics filter serves for improving the power factor, which reaches a value of almost 1, and for reducing the load on the line produced by harmonics. The losses caused by the active harmonics filter are more than compensated by the fact that a subsequent converter can constantly be operated at an optimal operating point because of the input control of the operating voltage.

The extra effort that is necessary, compared to an SMPS without an active harmonics filter, is compensated from about 500 W upwards by savings elsewhere (e.g. smaller smoothing capacitance and transistors of a higher resistance in the SMPS). With the wide-ranging power supplies that are in increasing demand, i.e. power supplies that can work on a line of 90 through 240 Vac without any switching changes, the power pay-off limit decreases considerably.

2 Electronic Ballasts for Fluorescent Lamps

The VDE and the EVUs require of **industrial** consumers that they take "sinusoidal current from the line, i.e. exhibit a purely ohmic response. This is the case with incandescent lamps, cooker rings and heating fixtures.

In all electronic devices with rectification and a CR load the current drain is pulsed, i.e. afflicted by a large harmonic content and impermissible according to VDE. The reflected current ripple can interfere with installations for AF power-line carrier control for instance, i.e. lead to faulty switching. Consequently the harmonic content of the current may not exceed certain values.

The line current for a ballast operating with a stable fluorescent lamp must be such that the share of harmonics in relation to the fundamental does not exceed the values given in table 1.

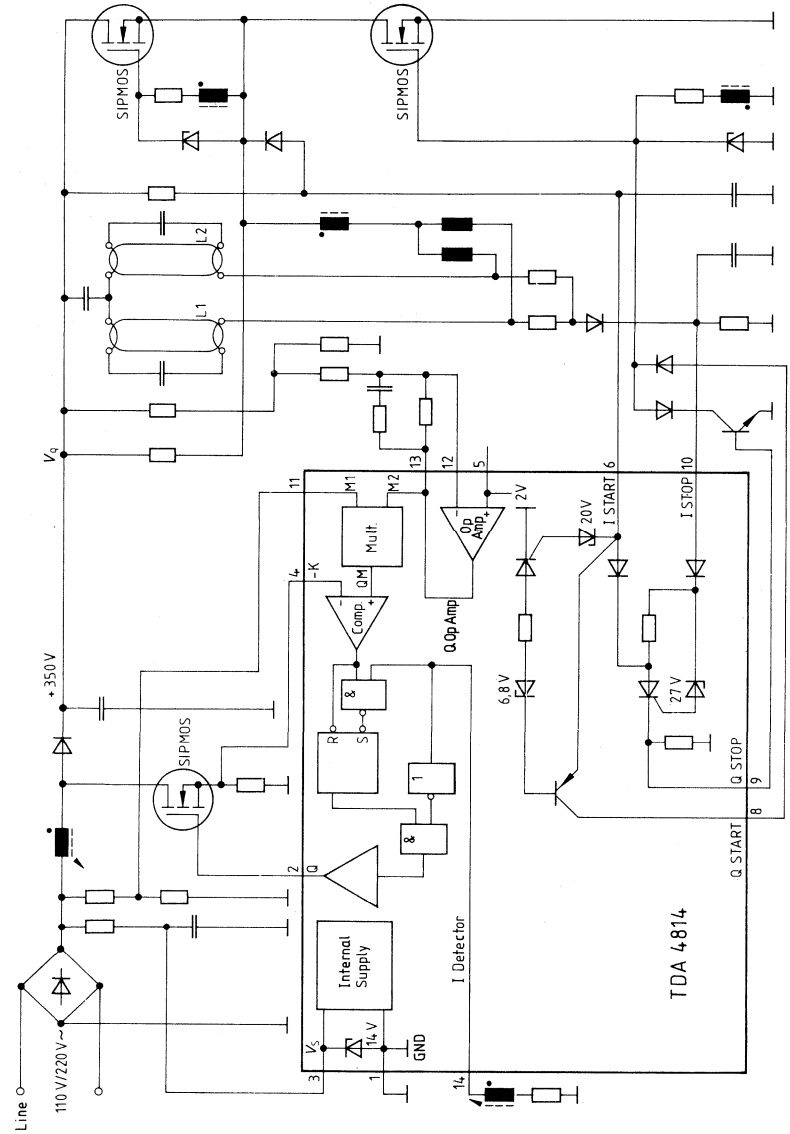
Table 1 Line-Current Harmonic Content in acc. with VDE 0712, Part 2

Harmonics	Permissible harmonic content[1] in %
3rd harmonic	$25 \times \frac{\lambda}{0.9}$
5th harmonic	7
7th harmonic	4
9th harmonic	3
11th harmonic	2
13th harmonic and higher	1

1) λ is the power factor

The values given here are achieved using the TDA 4814 A/TDA 4816 G to drive a SIPMOS in an upconverter regulating circuit.

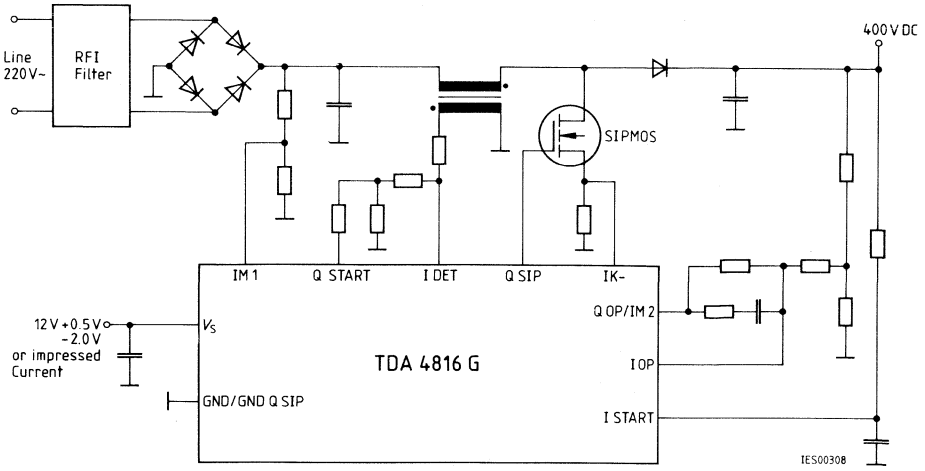
Application Example
Electronic ballast



Remark
Kindly note that the Siemens AG holds patents on electronic ballasts for fluorescent lamps, published in "Siemens Energy and Automation", Vol. II, No. 2, March/April 1985

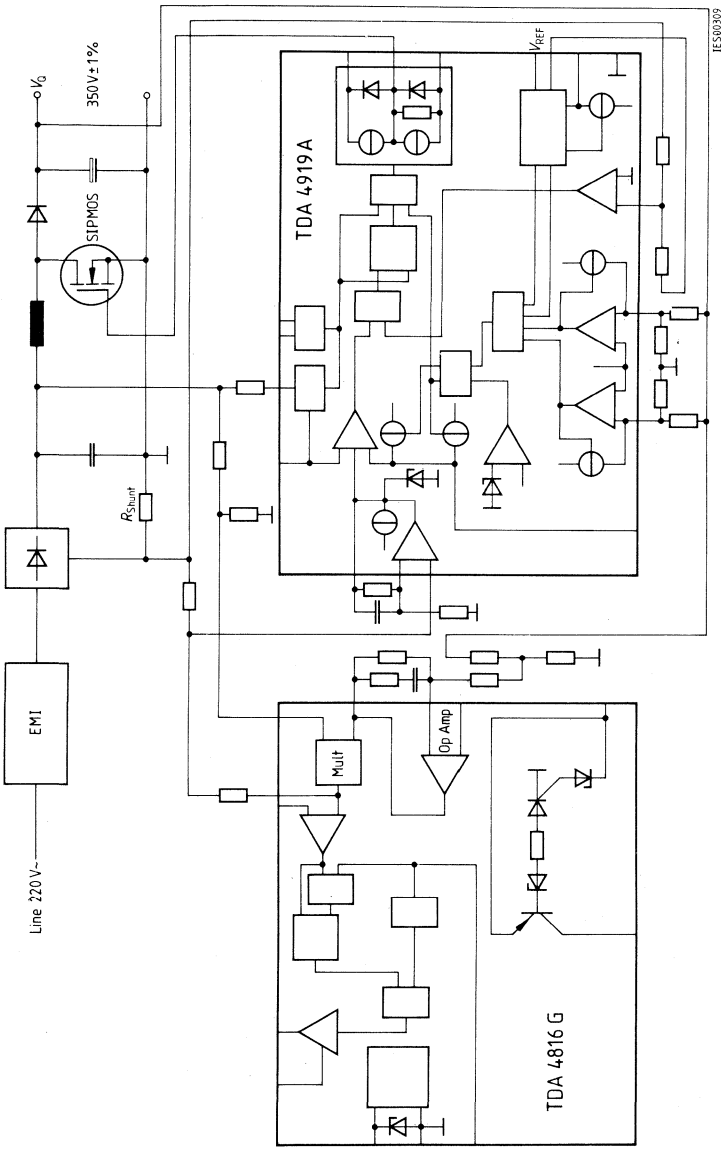
Application Circuit 1

(Circuit principle with detector, free-running frequency and triangular-shaped choke current)



Application Circuit 2

Circuit principle with fixed frequency, trapezoidal-shaped choke current



IC for Sinusoidal Line Current Consumption

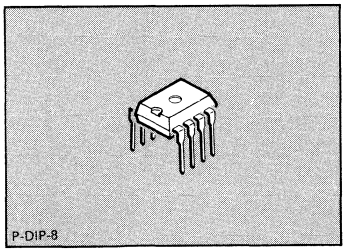
TDA 4817

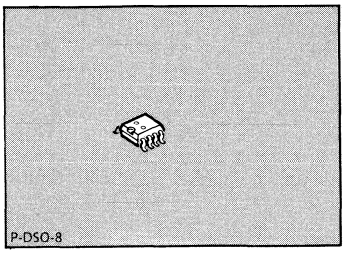
Advance Information

Bipolar IC

Features

- Excellent sinewave current simulation
- Power factor approaching 1
- Direct drive of SIPMOS transistor
- Zero crossing detector
- 110/220 V AC operation without switchover
- Standby current consumption of 0.5 mA





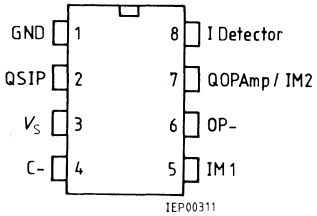
Type	Ordering Code	Package
▼ TDA 4817	Q67000-A8298	P-DIP-8
▼ TDA 4817 G	Q67000-A8299	P-DSO-8 (SMD)

▼ New type

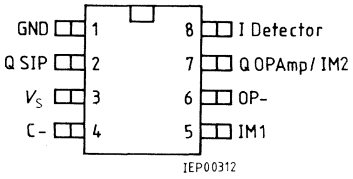
The device contains the components for designing a switch-mode power supply (SMPS) with sinusoidal line current consumption. A sinusoidal line current is required in particular when there is high power consumption. A typical application is in electronic ballasts for fluorescent lamps, especially when a large number of such lamps are concentrated on one line supply point. But this IC may also be used in general SMPS driving applications. The possibility of regulating the output voltage means that a device can be operated on different line voltages (110/220 V AC) without any switchover.

Pin Configurations
(top view)

P-DIP-8



P-DSO-8



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	QSIP	Driver output
3	V_S	Supply voltage
4	C–	Comparator input
5	M1	Multiplier input
6	OP–	Input
7	Q_{op}/M2	Operational-amplifier output Q_{OP} and multiplier input M2
8	I Detector	Detector input

The TDA 4817 is the 8-pin economy version of the TDA 4814 A without reference voltage and start/stop circuit.

Furthermore, the following main characteristics have been changed:

Type	Z current V_S – GND max. mA	Z current max. mA	Current consumption I_S $V_{Son} < V_S < V_Z$ max. mA
TDA 4814 A	300	200	6.5
TDA 4817	100	100	10

Circuit Description

The IC does not switch from standby to full current drain until the turn-on threshold on V_S is exceeded. Turn-off is governed by hysteresis. The integrated Z-diode limits the voltage on V_S when impressed current is fed.

The operational amplifier can be configured as a control amplifier. It then compares the divided output voltage V_Q with a reference voltage V_{REF} (2 V) that is stable with temperature. The output voltage of the op-amp that is produced in this way is multiplied by a sine-magnitude voltage in the multiplier (M1). At the output of the multiplier a sine-magnitude voltage then appears that is variable in amplitude. This nominal voltage is subsequently applied to the positive input of the comparator. The nominal voltage from the multiplier output can then be compared by the comparator with a voltage derived from the actual line current. The comparator output applies the reference signal via a logic circuit to the driver that controls the SIPMOS transistor.

General Notes on Possible Operating Modes

Defined operation with an inexpensive (slow) rectifier diode will only be possible if the SIPMOS transistor is unable to turn on until the current in the choke has become zero. No current gaps must occur in the choke because then the line current would no longer be sinusoidal. For this reason the input I Detector senses when the choke current has decreased to zero after turn-off of the SIPMOS transistor, thus ensuring that the SIPMOS transistor does not turn on too early and no current gaps appear. If a fast rectifier diode is used, the choke current doesn't need to fall to zero before turn-on. Here the total current is sensed and the SIPMOS transistor is switched so that this total current precisely follows up the sinusoidal definition. The advantages of this mode are thus substantially smaller current amplitudes in the choke, in the SIPMOS transistor and in the rectifier diode.

Free-running Operation with Detector (I Detector)

When input I Detector is high, the SIPMOS driver QSIP is turned off. At the same time the flipflop can be set by the comparator. When input I Detector is low, output QSIP is enabled and can be turned off again by the comparator by resetting the flipflop. Thus the choke is always currentless when the SIPMOS transistor turns on and no current gaps appear in the choke.

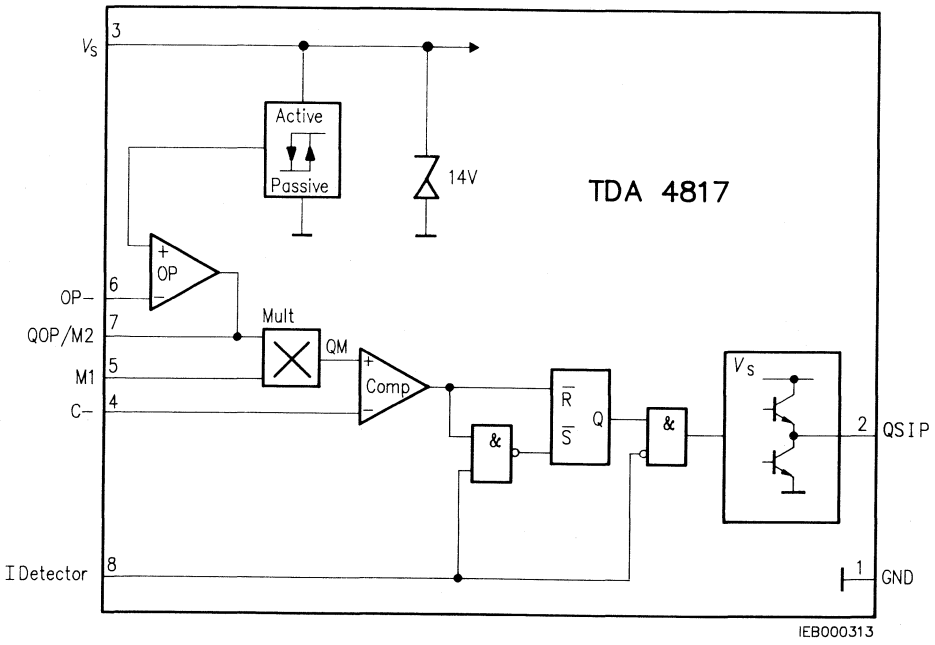
Driver Output (QSIP) for SIPMOS Transistors

The output driver is designed as a push-pull stage. There is a resistor of 10 Ω connected in series with the output for the purpose of current limiting. Across QSIP and ground there is a resistor of 10 KΩ to ensure that the SIPMOS transistor remains turned off during standby.

Output QSIP is additionally connected by diodes to the supply V_S and to ground. When the supply voltage to the switch-mode power supply is turned on, the diode to V_S conducts capacitive displacement currents from the gate of the SIPMOS transistor into the smoothing capacitor on V_S. The voltage on V_S must not exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode to ground clamps negative voltages on QSIP to −0.7 V. Capacitive currents produced by voltage dips on the drain of the SIPMOS transistor can thus be conducted away unhindered.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	typ.	max.	Units	Notes
Supply voltage	V_S	−0.3		V_Z	V	V_Z = Z-voltage
Inputs						
Comparator	V_{C-}	−0.3		20	V	
Operational amplifier	V_{OP-}	−0.3		20	V	
Multiplier	V_{M1}	−0.3		20	V	
Output OP	V_{QOP}	−0.3		6	V	
Z current VS-GND	I_Z	0		100	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	−0.3		V_S	V	
QSIP clamping diodes	I_{QSIP}	−10		10	mA	$V_{QSIP} > V_S$ or $V_{QSIP} < -0.3$ V
Detector input	V_{Det}	0.9		6	V	
Detector clamping diodes	I_{Det}	−10		10	mA	$V_{Det} > 6$ V or $V_{Det} < 0.9$ V
Junction temperature	T_J			150	°C	
Storage temperature	T_{stg}	−55		125	°C	
Thermal resistance system – air TDA 4817	$R_{th\ SA}$			100	K/W	P-DIP-8 package
TDA 4817G	$R_{th\ SA}$			170	K/W	P-DSO-8 package

Operating Range

Supply voltage	V_S	V_{Son}		V_Z	V	1)
Z-current	I_Z	0		100	mA	Observe P_{max}
Driver current	I_{QSIP}	−300		300	mA	Observe P_{max}
Ambient temperature	T_A	−25		85	°C	

Electrical Characteristics

$V_{Son} < V_S < V_Z$; $T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Current Consumption Without load on driver (Q_{SIP}) and V_{REF};						
Q_{SIP} Low	I_S			0.5	mA	$0\ V < V_S < V_{Son}$
	I_S		5	10	mA	$V_{Son} < V_S < V_Z$
Load on QSIP with SIPMOS gate; dynamic operation	I_S			15	mA	$V_S = 12$ V; $f_{switch} = 50$ kHz; load QSIP = 10 nF

1) For V_{Son} and V_Z values, **see characteristics**

Electrical Characteristics

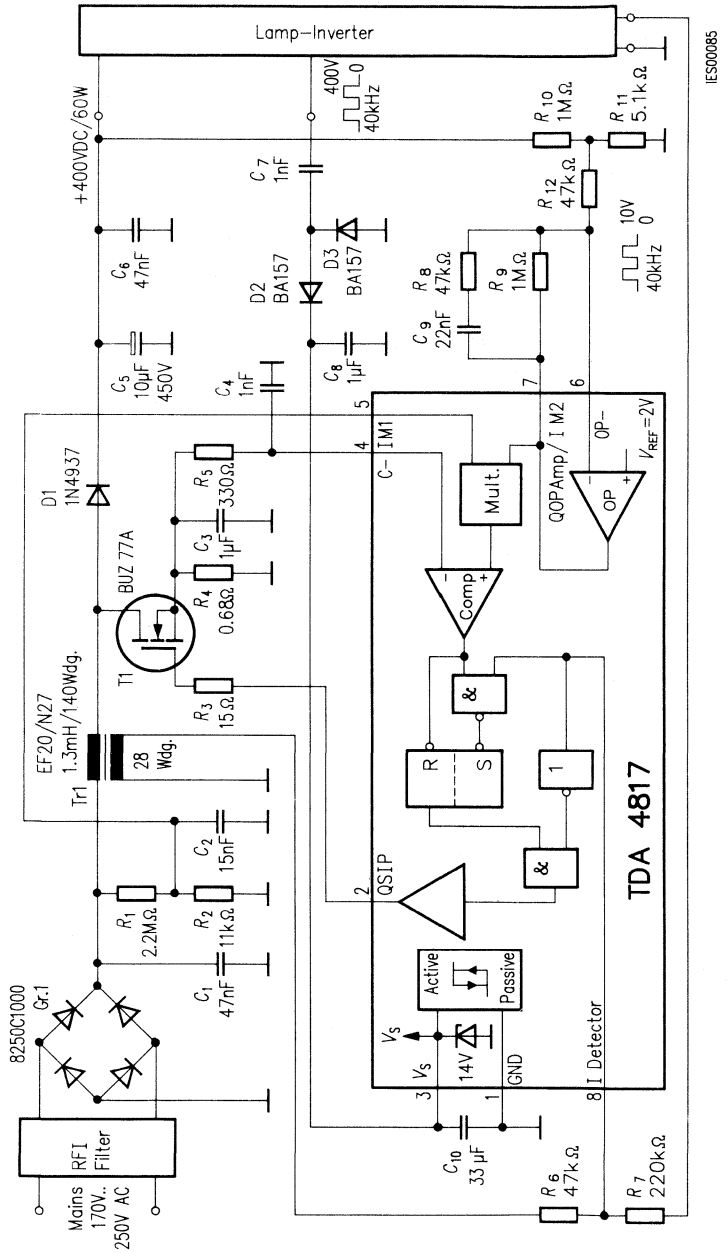
$V_{Son} < V_S < V_Z$; $T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Units	Test Conditions
Hysteresis on V_S						
Turn-on threshold for V_S rising	V_{SH}	9.6	10.4	11.2	V	
Switching hysteresis	V_{Shy}	1.0		1.7	V	
Comparator						
Input offset voltage	V_{IO}	−10		10	mV	
Input current	$-I_I$			2	µA	
Common-mode input voltage	V_{ICM}	0		3.5	V	
Operational Amplifier						
Open-loop voltage gain	G_{VO}	60	80		dB	
Input offset voltage	V_{IO}	−10		10	mV	
Input current	$-I_I$			2	µA	
Common-mode input voltage	V_{IC}	0		3.5	V	
Output current	I_Q	−3		1.5	mA	
Output voltage	V_Q	1.2		4	V	
Gain-bandwidth product	f_T		2		MHz	
Transition phase	Φ_T		120		deg	
Output Driver						
Output voltage High	V_{QSIPH}	5			V	$I_{QSIP} = -10$ mA
Output voltage Low	V_{QSIPL}			1	V	$I_{QSIP} = 10$ mA
Output current rising edge	$-I_{QSIP}$	200	300	400	mA	$C_L = 10$ nF
falling edge	I_{QSIP}	250	350	450	mA	$C_L = 10$ nF
Z-Diode (v_S)						
Z-voltage (observe P_{max})	V_Z	13	15.5	17	v	$I_Z = 200$ mA
Multiplier						
Quadrant for input voltages			I.		qu.	
Input voltage M1	V_{M1}	0		1	V	
Reference level for M1	$V_{REF\ M1}$		0		V	
Input voltage M2	V_{M2}	V_{REF}		$V_{REF}+1$	V	
Reference level for M2	$V_{REF\ M2}$		V_{REF}		V	
Input current M1, M2	$-I_I$	0		2	µA	
Output voltage	V_{QM}	650	750	850	mV	
Coefficient of output voltage	C_Q	0.4	0.6	0.8	V^{-1}	
Temperature response of coefficient	$\Delta TC/C_Q$	−0.3	−0.1	0.1	%/K	
Delay Times						
Input comparator-QSIP	t_I		200	500	ns	[1]
Detector						
Upper switching voltage for voltage rising (H)	V_{DetH}	1.0	1.3	1.6	V	
Lower switching voltage for voltage falling (L)	V_{DetL}	0.95			V	
Input current	$-I_{Det}$			10	µA	0.9 V < V_{Det} < 6 V
Clamping-diode level positive	V_{Det+}		6.9		V	$I_{Det} = 3$ mA
negative	V_{Det-}		0.6			$I_{Det} = 3$ mA
Switching hysteresis	V_{Dethy}	50		300	mV	

Calculation of output voltage V_{QM}: $V_{QM} = C \times V_{M1} \times V_{M2}$ in V.

[1]) Step function on comparator input ΔV_{Comp} from −100 mV to +100 mV

Application Circuit: Electronic Ballast



SIEMENS

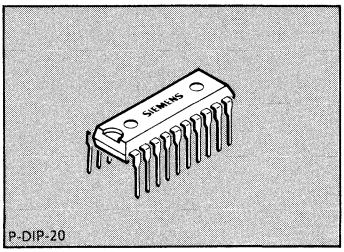
SMPS – IC with SIPMOS Driver Output

TDA 4918
TDA 4919

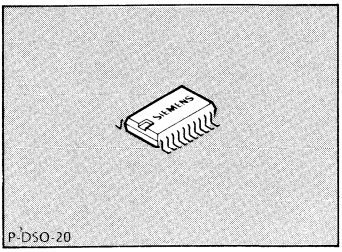
Bipolar IC

Features

- Switching frequency up to 300 kHz (TDA 4919) or 150 kHz (TDA 4918)
- Push-pull output driver with +700 mA/−500 mA
- Separate GND for the driver outputs
- Feed-forward control
- Soft start
- Hysteresis adjustable at overvoltage and undervoltage comparator
- Current-saving starting circuit
- Current mode and voltage mode operation are possible



P-DIP-20



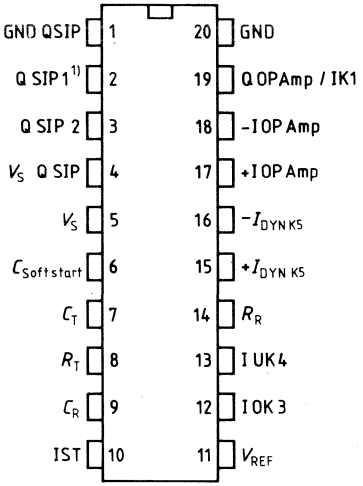
P-DSO-20

	Type	Ordering Code	Package
S	TDA 4918 A	Q67000-A8021	P-DIP-20
S	TDA 4918 G	Q67000-A8142	P-DSO-20 (SMD)
S	TDA 4919 A	Q67000-A8143	P-DIP-20
S	TDA 4919 G	Q67000-A8018	P-DSO-20 (SMD)

Functional Description

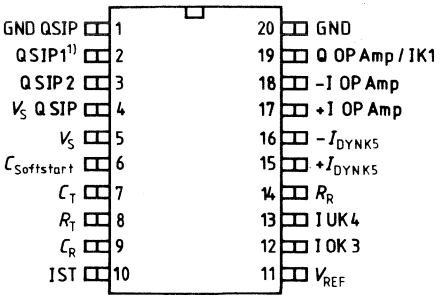
The versatile switch-mode power supply ICs for the direct control of SIPMOS power transistors comprise digital and analog functions. These functions are required for the design of high-quality flyback and forward converters during single-phase and push-pull operation in normal, half-bridge and full-bridge configurations. The ICs can also be used for transformerless voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switch-mode power supply are recognized by on-chip comparators which activate protective functions. The TDA 4918 has two driver outputs for push-pull switch-mode power supplies, as well as single-phase SMPS with a duty cycle limitation of 50%. The TDA 4919 with a driver output is suitable for single-ended SMPS with duty cycles of up to 100% approximately.

Pin Configuration TDA 4918 A/TDA 4919 A
(top view)



1) only TDA 4918A IEP00314

Pin Configuration TDA 4918 G/TDA 4919 G
(top view)



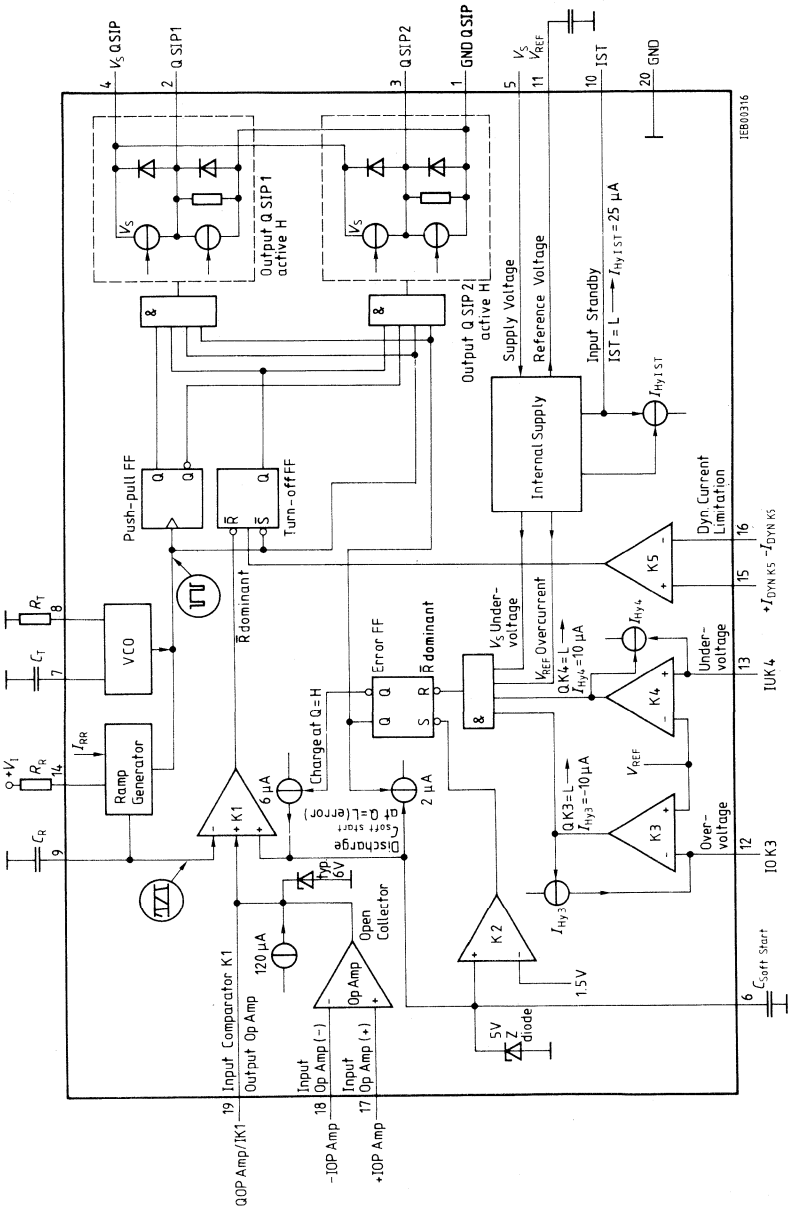
1) only TDA 4918G IEP00315

3

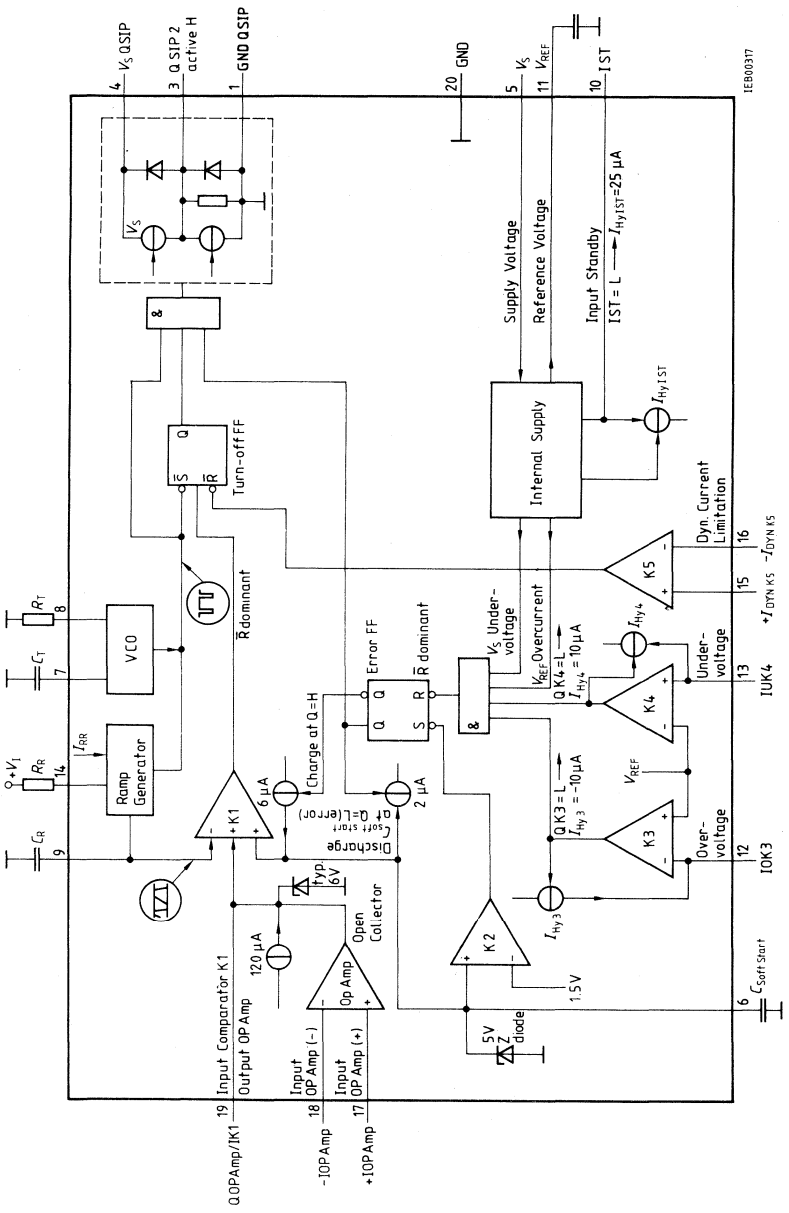
Pin Definitions and Functions

Pin	Symbol	Function
1	GND Q SIP	Ground driver
2 3	Q SIP1 Q SIP2	SIPMOS driver 1 (only TDA 4918) SIPMOS driver 2
4 5	V_S QSIP V_S	Supply voltage driver Supply voltage
6	$C_{soft\ start}$	Soft start
7 8 9	C_T R_T C_R	Frequency generator Frequency generator Ramp generator
10	I ST	Input standby
11	V_{REF}	Reference voltage
12 13	I OK3 I UK4	Input overvoltage Input undervoltage
14	R_R	Ramp generator
15 16	$+I_{DYN\ K5}$ $-I_{DYN\ K5}$	Dyn. current limitation Dyn. current limitation
17 18	I Op Amp (+) I Op Amp (−)	Input operational amplifier Input operational amplifier
19	Q Op Amp /IK1	Output operational amplifier Q Op Amp / input comparator
20	GND	Ground

Block Diagram TDA 4918



Block Diagram TDA 4919



Functional Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

The IC enables the two outputs not before the turn-on threshold ($V_{S\ ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp Generator

The ramp generator is triggered by the VCO and TDA 4919 operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-Pull Flipflop (only TDA 4918)

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two SIPMOS driver outputs is enabled at a time.

Comparator K1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-off Flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the outputs are enabled. Upon an error signal from K5 or upon a turn-off signal from K1 the flipflop disables the outputs.

Z Diode

The Z diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output it sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K1 plus inputs – compared with the ramp generator voltage – is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the outputs (low), and after elimination of the error, a restart of the outputs by soft start.

Comparators K3 (Overvoltage), K4 (Undervoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K3 and K4, that can be used to enable an adjustable hysteresis or a holding function. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K3 or K4. In the undervoltage case, the set current flows at K4 into the component in the technical direction of current flow, with overvoltage at K3 out of the component.

Comparator K5 (Dynamic Current Limiter)

K5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Standby Input (I ST)

This input switches voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S – standby input – ground.

In standby mode the component has a much lower current consumption compared to active operation. The outputs are then active low.

Should the component be operated by means of feedback supply from the switch-mode power supply, the starting phase can optimally be dimensioned.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp, the error comparators, the ramp generator, or other external components. The voltage source is short-circuit proof to ground.

SIPMOS Driver Outputs (Q SIP)

TDA 4918

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

TDA 4919

The output is active high. The duration during which the output is active can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which the output is low (dead time).

The output drivers are designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at pin I St).

Output Q SIP is connected with the supply voltage $V_{S\,Q\,SIP}$ and with ground via diodes.

The diode connected to V_S routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_S during turning on the SMPS supply voltage. The voltage at V_S can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to −0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approx. 2 V, both outputs are active low in the disabled state. The function of the diode connected to V_S is then taken over by the pull-down source.

The maximum output voltage is limited by the respectively lowest value of V_S, $V_{S\,Q\,SIP}$ or an internal Z diode. The internal Z diode limits the voltage at Q SIP to typ. 20 V.

3

Absolute Maximum Ratings

$T_A = -40$ to $+85$ °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	$V_{S\ QSIP}$, V_S	−0.3	33	V
Inputs Op Amp, K3, K5, I ST Input K4	V_I V_I	−0.3 −0.3	33 V_S	V V
Frequency Generator (VCO)				
Voltage at R_T; C_T Current at C_T $V_{CT} > 6$ V	V_{CT}, V_{RT} I_{CT}	−0.3	6 3	V mA
Ramp Generator				
C_R input R_R input	V_{CR} I_{RR}	−0.3 0	6 3	V mA
Reference voltage Output Op Amp $V_{Q\ op\ amp} > 6$ V	V_{REF} $V_{Q\ op\ amp}$ $I_{Q\ op\ amp}$	−0.3 −0.3	6 6 2	V V mA
Driver output Q SIP[1] Q SIP clamp diodes $V_{Q\ SIP} > V_S$ or $V_{Q\ SIP} < -0.3$ V	$V_{Q\ SIP}$ $I_{Q\ SIP}$	−0.3 −100	$V_{S\ QSIP}$ 100	V mA
Soft start $V_{C\ soft\ start} > 6$ V	$V_{C\ soft\ start}$ $I_{C\ soft\ start}$	−0.3 0	6 100	V µA
Junction temperature Storage temperature	T_j T_{stg}	 −65	150 125	°C °C
Thermal resistance system – air P-DIP-20 P-DSO-20	 $R_{th\ SA}$ $R_{th\ SA}$		 60 90	 K/W K/W
Operating Range				
Supply voltage	V_S $V_{S\ Q\ SIP}$	$V_{S\ ON}$[2]	30 30	V V
Frequency generator (VCO) Ramp generator	f_{VCO} f_R		300 300	kHz kHz
Ambiente temperature	T_A	−40	85	°C
Ground QSIP	GND QSIP	GND QSIP −0.3	GND QSIP +0.5	V

The characteristics refer to both the pins connected to ground.

[1]) With this, the max. power dissipation or junction temperature must be taken into account!

[2]) For $V_{S\ ON}$ values refer to characteristic data.

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test conditions
Current consumption without load at V_{REF} Q op amp, Q SIP 1/2	I_S	6		18	mA	$C_T = 1$ nF frequency generator with 100 kHz outputs active
Standby operation	I_{ST}			3.5	mA	$V_S = 20$ V
Hysteresis at V_S						
Turn-on threshold for V_S rising	$V_{S\,H}$			9.6	V	$V_{I\,ST} \geq V_{IST\,H}$
Turn-off threshold for V_S falling	$V_{S\,L}$	7.8			V	
Reference						
Voltage	V_{REF}	2.475	2.5	2.525	V	$I_{REF} = 1$ mA $T_A = 25$ °C $V_S = 15$ V
Load current	$-I_{REF}$	0		3	mA	
Voltage change	ΔV_{REF}			10	mV	$I_{REF} = 1$ mA ± 20%
Voltage change	ΔV_{REF}			3	mv	$V_S = 15$ V ± 20%
Temperature response	$\Delta V_{REF}/\Delta T\Delta$	−0.3		0.3	mV/K	
Response threshold for V_{REF} overcurrent	$-I_{REF\,O}$	4	7	10	mA	
Frequency Generator (VCO)						
Frequency range	f_{VCO}			300	kHz	
Frequency change	$\Delta f/f_{VCO}$			1	%	$V_S = 15$ V ± 20%
Tolerance	$\Delta f/f_{VCO}$	−7		7	%	$C_T = 1$ nF $f_{VCO} = 100$ kHz; $T_A = 25$ °C
Charge current for C_T (perm.) = current at pin R_T	$-I_{RT}$	0		1	mA	$I_{RT} = V_{REF/RT}$
Discharge current for C_T	I_{dch}		2		mA	internally fixed
C_T range		0.47		68	nF[2])	
Dead time	τ_t		350	450	ns	$C_T = 470$ pF, $f_{VCO} = 100$ kHz
			400	500	ns[2])	$C_T = 470$ pF, $f_{VCO} = 300$ kHz

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2]) The time of the falling edge (fall time) is proportional to C_T, if the discharge current largely exceeds the charge current. The fall time is proportional to the minimum dead time at the outputs.

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test conditions
Ramp Generator						
Frequency range	f_R			300	kHz	
Maximum voltage at C_R Minimum voltage at C_R	$V_{CR\,H}$ $V_{CR\,L}$	5.4 1.65	6.1 1.8	6.7 1.95	V V	
Charge current for C_R (perm) = current at pin R_R Discharge current for C_R	I_{ch} I_{dch}	0 1.3	2	1 2.7	mA mA	V_{RR} approx. 0.7 V internally fixed
Ratio $I_{RR}/I_{CR\,charge}$		0.95		1.1		$I_{RR} = 0.5$ mA
Capacitance	C_R	100			pF	
Duty cycle (active time/ period at output)	t_V		5/20			
Temperature coefficient of duty cycle	T_C		0.2		%/K	
Comparator K1						
Input current	$-I_{K1}$			2	µA	
Common-mode input voltage range	V_{IC}	0		$V_{CR\,H}$	V	
Turn-off delay time	t			500	ns[2])	Rated load 3 nF at Q SIP
Operational Amplifier						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	−10		10	mV	Pin 19 n.c.
Input current	$-I_{I\,op\,amp}$			2	µA	
Common-mode input voltage range	V_{IC}	0		4	V	
Output current	$I_{Q\,op\,amp}$	0		2	mA	
Output voltage range	V_Q	0.5		$V_{CR\,H}$	V	0 mA < I_Q < 2 mA
Transition frequency Transition phase	f_T Φ_T		3 120		mHz deg.	
Temperature coefficient of V_{IO}	TC	−30		30	µV/K	Pin 19 n.c.; $V_{IC} = 3$ V
Source current at Q Op Amp	$I_{op\,amp}$	70	100	130	µA	0.5 V < V_Q < $V_{CR\,H}$

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2]) Step function $V_{REF} = -100$ mV ⇝ $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to 85 °C

Parameter	Symbol	Test Conditions	Limit Values min.	typ.	max.	Unit
Soft Start						
Charge current for $C_{soft\ start}$	$-I_{ch}$		4	6	8	µA
Discharge current for $C_{soft\ start}$	I_{dch}		1	2	3.2	µA
Upper limiting voltage	V_{lim}		4.4	4.8	5.0	V
Switching voltage of K2	V_{K2}		1.3	1.5	1.7	V
Dynamic Current Limitation K5						
Input current	$-I_{I\,DYN}$				2	µA
Input offset voltage	V_{IO}		−10		10	mV
Common-mode input voltage range	V_{IC}		0		V_S-3	V
Turn-off delay time	t	Rated load 3 nF at QSIP		250	400	ns[2])
Undervoltage K4						
Input current at K4	$-I_{I\,K4}$				0.2	µA
Switching voltage at K4	V_{sw}		V_{REF} −0.01		V_{REF} +0.01	V
Hysteresis current	$I_{Hy\,4\,H}$	$V_{(+\,K4)} < V_{sw}$	11	17	22	µA
	$I_{Hy\,4\,L}$	$V_{(+\,K4)} > V_{sw}$			0.1	µA
Turn-off delay time	t				3	µs[2])
Overvoltage K3						
Input current	$-I_{I\,K3}$				0.2	µA
Switching voltage	V_{sw}		V_{REF} −0.01		V_{REF} +0.01	V
Turn-off delay time	t				3	µs[2])
Hysteresis current	$-I_{Hy\,4\,H}$	$V_{(-K6)} > V_{sw}$	6	9	12	µA
	$-I_{Hy\,4\,L}$	$V_{(-K6)} < V_{sw}$			0.1	µA

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2]) Step function $V_{REF} = -100$ mV ⌐→ $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics

$V_{S\,ON} < V_S < 40$ V[1]), $T_A = -40$ to 85 °C

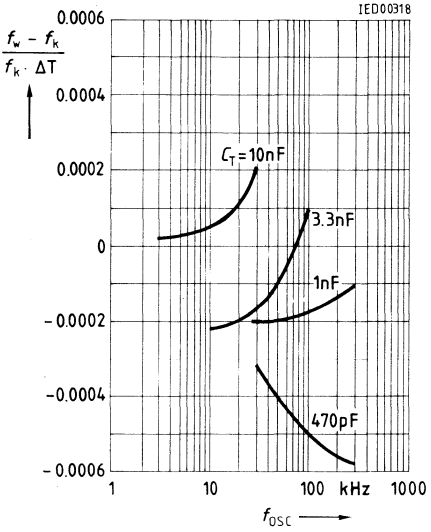
Parameter	Symbol	Test Conditions	Limit Values min.	typ.	max.	Unit
Output Driver QSIP 1/2						
Output voltage high	V_{QH}	$I_{Q\,SIP} = -250$ mA; $V_S = V_{SQSIP}$	$V_S - 3$			V
Output voltage low	V_{QL}	$I_{Q\,SIP} = +250$ mA; $V_S = V_{SQSIP}$			2.1	V
	V_{QL}	$I_{Q\,SIP} = +10$ mA; $V_S = V_{SQSIP}$			1.4	V
Output current	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 20$ V	500	700		mA[2]
	$-I_{Q\,SIP}$		300	500		mA[2]
	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 15$ V		600		mA[2]
	$-I_{Q\,SIP}$			500		mA[2]
	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 10$ V		400		mA[2]
	$-I_{Q\,SIP}$			400		mA[2]
Input Standby IST						
Turn-on threshold for $V_{I\,ST}$ rising	$V_{I\,ST\,H}$	$V_S > V_{S\,ON}$; $T_A = 25$ °C	6.1	6.8	7.5	V
Temperature response	$\Delta V_{ISTH}/\Delta T$			−0.023		%/K
Turn-off threshold for $V_{I\,ST}$ falling	$V_{I\,ST\,H}$		5.5	6.1	6.7	V
Temperature response	$\Delta V_{ISTL}/\Delta T$			0.047		%/K
Hysteresis current	$-I_{Hy\,IST\,H}$	$V_{IST} > V_{IST\,H}$			2	µA
	$I_{Hy\,IST\,L}$	$V_{ISTL} \le V_{IST} \le V_{ISTH}$; $T_A = 25$ °C	35	50	65	µA
Temperature response	$\Delta I_{Hy\,ISTL}/\Delta T$			0.01		%/K

[1] $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2] Dynamic maximum current during rising or falling edge

Diagrams

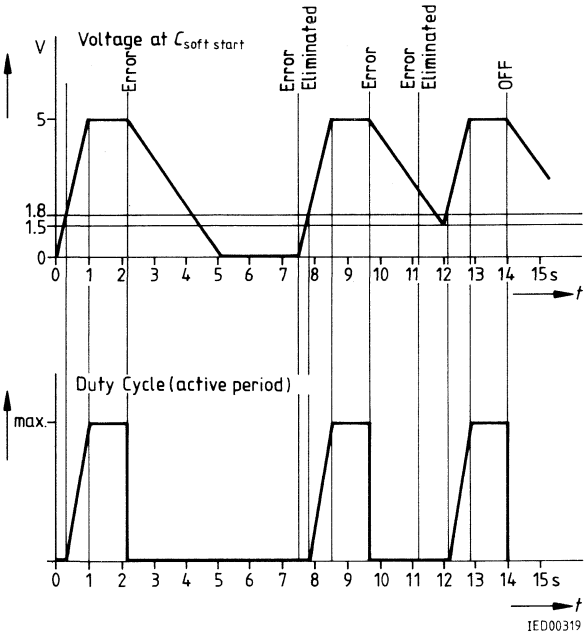
Typical temperature dependance of the frequency generator at different C_T values.



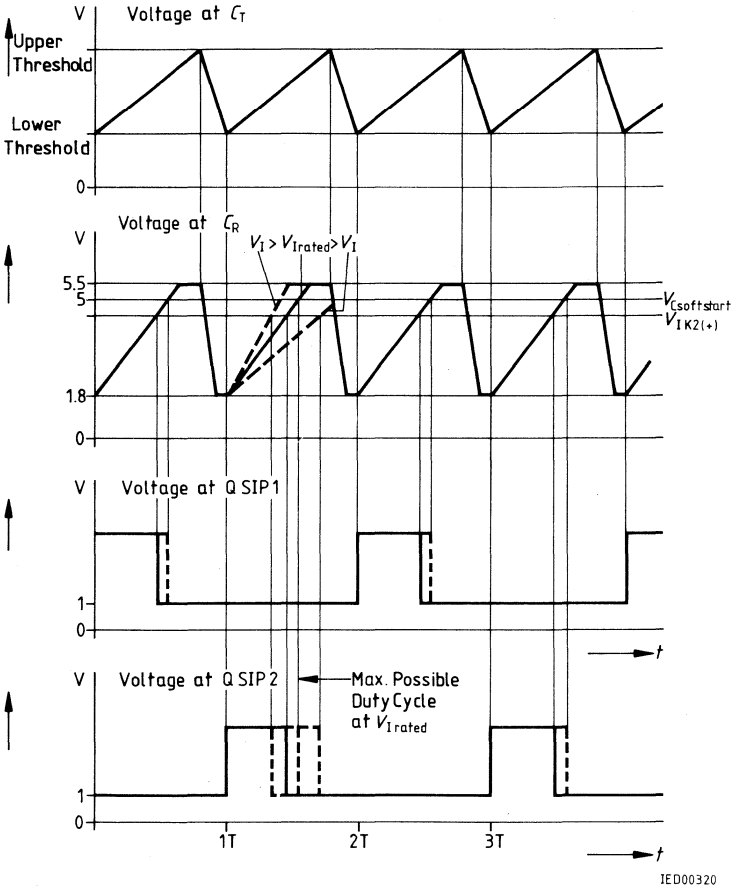
f_k = Frequency at room temperature
f_w = Frequency at thermal increase

Pulse Diagram

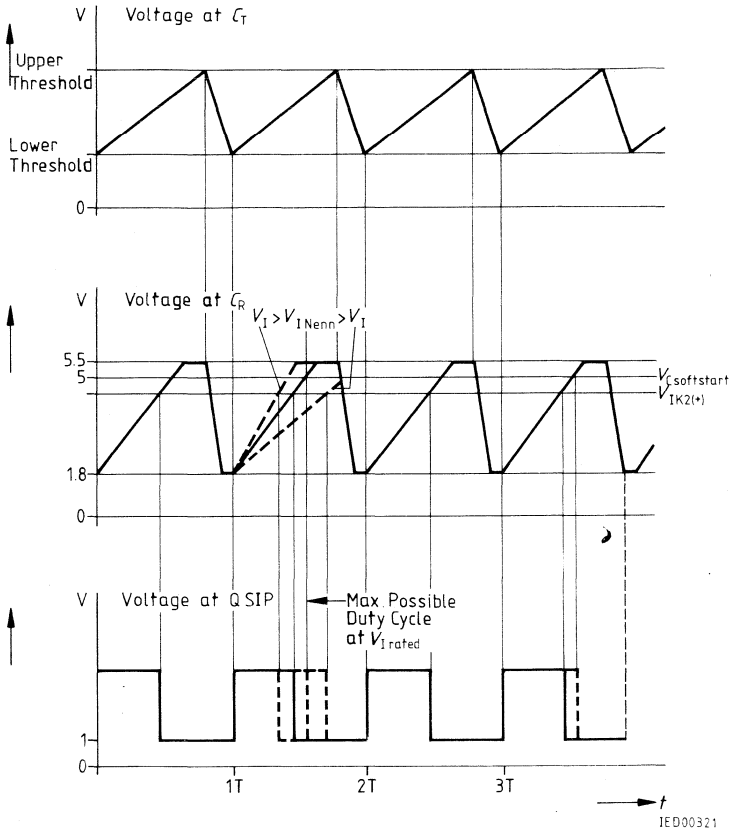
Soft Start/Error/ON-OFF



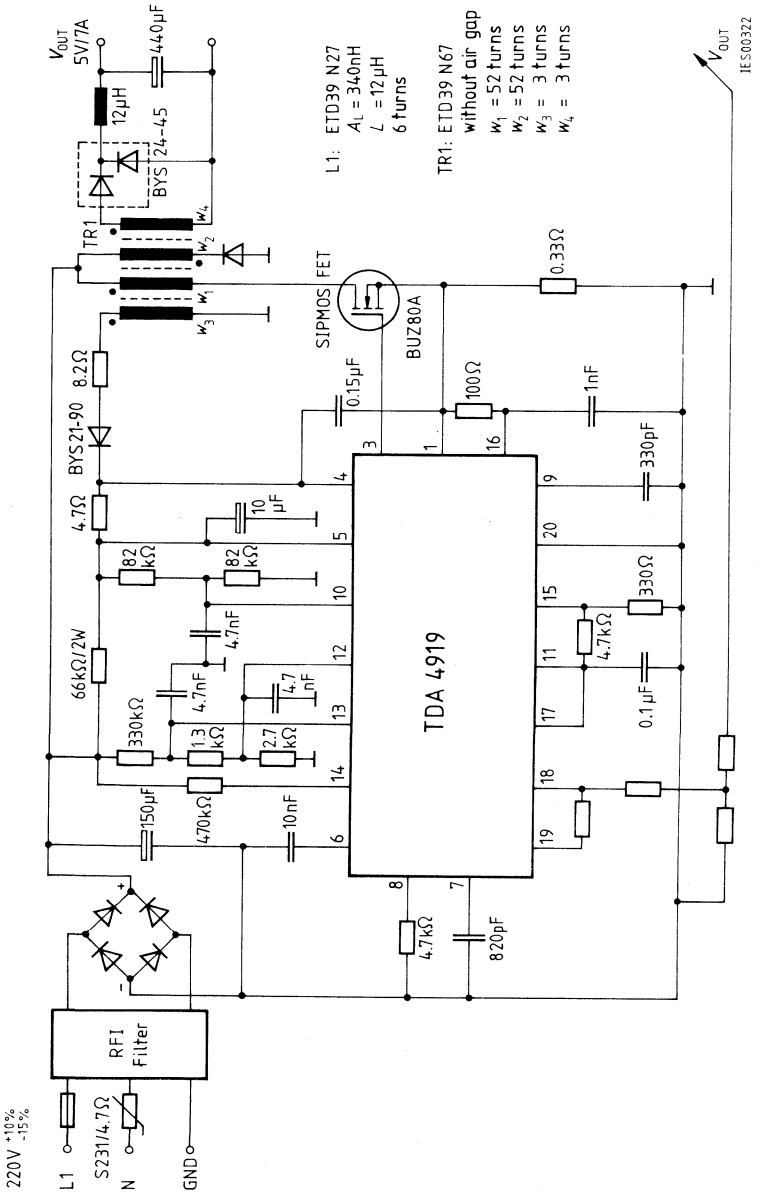
Pulse Diagram TDA 4918



Pulse Diagram TDA 4919



Application Circuit



SIEMENS

5-V Low-Drop Voltage Regulator

TLE 4258

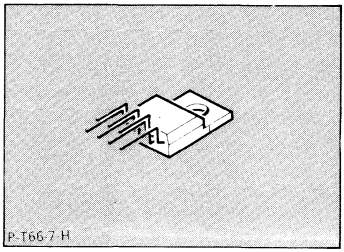
Preliminary Data

Bipolar IC

3

Features

- Low-drop voltage
- Low quiescent current
- Reset output
- Protection against reverse polarity
- Overvoltage protection 70 V
- Short-circuit proof
- Suited for automotive electronics
- Inhibit input
- Wide temperature range



Type	Ordering Code	Package
S TLE 4258	Q67000–A8238	P-T66-7-H (similar to TO-220)

The TLE 4258 is a very-low-drop voltage regulator which provides two regulated 5-V output voltages. The main regulator can be loaded with 750 mA and is turned on and off by pin 5 (pin 5 unconnected = main regulator off). In addition, the main regulator incorporates a short-circuit current limitation and is turned off in case of overvoltage ($V_I > V_{I\ OFF}$). The standby regulator can be loaded with 35 mA, it does not incorporate a short-circuit current limitation and remains permanently active at positive input voltage independent of the turn-off functions of the main regulator.

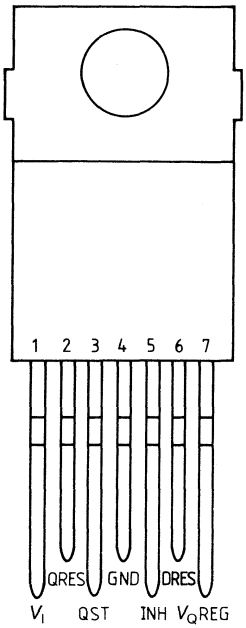
If the main regulator output voltage is less than 4.5 V, the reset output is switched to low without delay. As soon as the reset threshold has been exceeded, a delay time to be set by an external capacitor expires and afterwards the reset output switches to high again.

If the lines to the controller are long, the oscillating circuit of line inductance and input capacitance C_I can be attenuated by a resistor $\leq 1\ \Omega$ connected in series to C_I.

Circuit Description

The TLE 4258 incorporates a main and standby-control regulator: The amplifiers regulate the output voltage by comparing the output voltage (from the voltage divider) with a highly precise reference voltage. The standby regulator directly controls the base of a PNP series transistor and the main regulator via a buffer that can be turned off with inhibit pulse at pin 5. If the output voltage V_Q at pin 7 drops below 4.5 V, a reset signal is released which can only be disabled after a delay time to be set at pin 6. The main output is current-limited and remains active up to the input voltage $V_{I\ OFF}$.

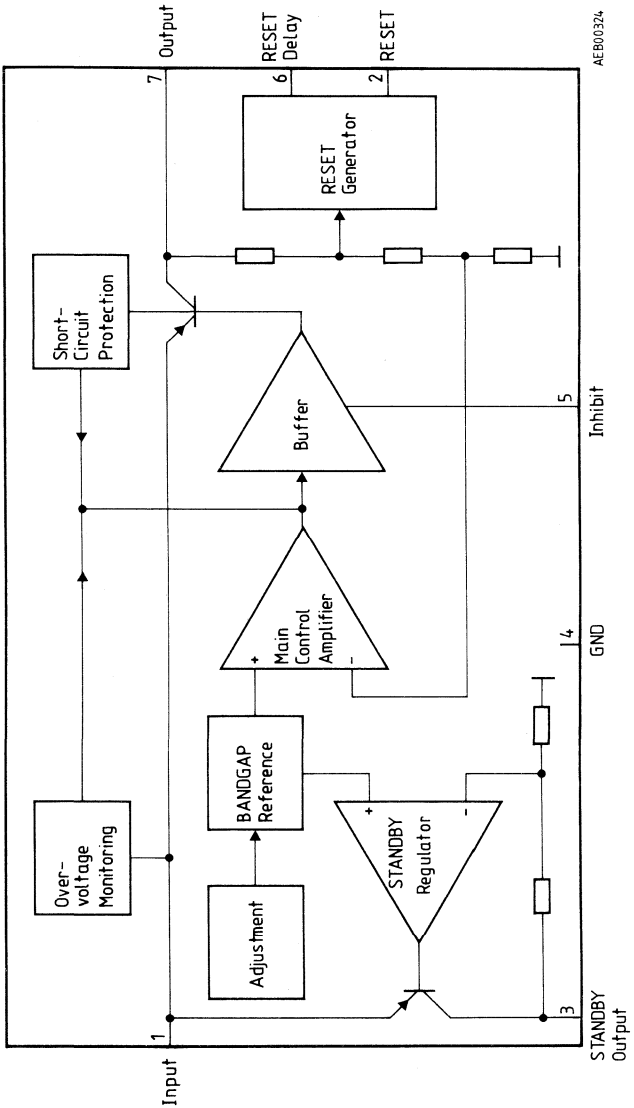
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_I	**Input** of voltage regulator
2	Q RES	**Reset output;** open-collector output NPN to pin 4. If the output voltage V_Q drops below the reset threshold, the output stage becomes conductive.
3	Q ST	**Standby output,** connect with a capacitor ≥ 10 µF
4	GND	**Ground;** reference potential
5	INH	**Inhibit (main regulator on/off),** input for turning on/off main regulator, connected to a 22-kΩ series resistor. With open input, the main regulator remains turned off.
6	D RES	**Reset delay;** pin for reset capacitor; the size of this capacitor determines the delay time of the reset signal typ. 175 ms/µF.
7	V_Q REG	**Main regulator output,** connected to a capacitor ≥ 22 µF.

Block Diagram



Absolute Maximum Ratings

$T_j = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Input (Pin 1)				
Supply voltage	V_I	−15	+36	V
Polarity reversal with test pulse $t_2 \leq 100$ ms see test circuit	V_I	−70		V
Load-dump with pulse shape $t_2 \leq 400$ ms see test circuit	V_I		70	V
Slew rate $0\,V \leq V_I \leq 24\,V$	SR		100	V/µs
Slew rate $24\,V \leq V_I \leq 70\,V$	SR		10	V/µs
Current	I_I		2.5	A
Reset Output (Pin 2)				
Voltage	V_R		8	V
Current	I_R		10	mA
Standby Output (Pin 3)				
Voltage	V_{ST}		6	V
Current	I_{ST}		50	mA
Ground (Pin 4)				
Current	I_{GND}		1.8	A
Inhibit (main regulator on/off), (Pin 5) Current	I_{INH}		±7.5	mA
Reset delay (Pin 6) Voltage	V_C		V_Q	V
Main regulator output (Pin 7) Voltage $V_I \geq V_Q$	V_Q		18	V
Current	I_Q		1.8	A
Temperature				
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	150	°C
Operating Range				
Input voltage	V_I	6	24	V
Junction temperature	T_j	−40	150	°C
Thermal resistance system – air	$R_{th\ SA}$		65	K/W
system – case	$R_{th\ SC}$		4	K/W

Characteristics

$V_I = 13.5$ V; $T_j = 25$ °C; $V_5 > 3.5$ V (unless otherwise specified)

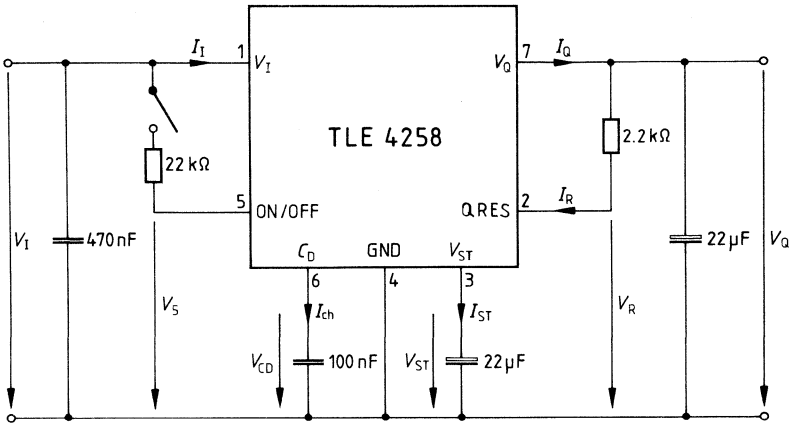
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Main Regulator						
Output voltage	V_Q	4.85		5.15	V	$0\ mA \le I_Q \le 750\ mA$ $6\ V < V_I < V_{I\,off}$ $-40\ °C \le T_j \le 125\ °C$
Input current Current consumption without load	I_Q I_Q I_Q I_Q			30 150 300 300	mA mA mA mA	$I_Q = 0$ mA; $I_{ST} = 0$ mA $I_Q = 450$ mA; $I_{ST} = 0$ mA $I_Q = 750$ mA; $I_{ST} = 0$ mA $V_I = 5.8$ V; $I_Q = 750$ mA; $I_{ST} = 0$ mA
Turn-off voltage	$V_{I\,off}$	25			V	$V_I > V_{I\,off}$
Output current Short-circuit current	I_Q I_{SC}	 0.75	 1	20 1.8	mA A	$V_I > V_{I\,off}$ $V_Q = 0$ V; $6\ V \le V_I < 13.5$ V
Drop voltage	V_{Dr} V_{Dr}		0.3 0.5	0.5 0.75	V V	$V_I = 4.5$ V; $I_Q = 450$ mA $V_I = 4.5$ V; $I_Q = 750$ mA
Static load regulation	$\Delta V_Q / \Delta I_Q$			0.2	Ω	$6\ V \le V_I \le 16\ V$ $0\ mA \le -I_Q \le 750\ mA$
Dynamic load regulation	ΔV_Q			150	mV	$I_Q = 75$ mA of $I_Q = 750$ mA $C_Q \ge 50\ \mu F$
Supply voltage-rejection	α_{SVR}	60			dB	$I_Q = 750$ mA; $V_I = 12\ V + 1\ V \cdot \cos(2\pi \times 120\ Hz \cdot t)$; $\alpha_{SVR} = 20 \log (1\ V / \Delta V_Q)$
Reverse output current	$-I_{QR}$		5	30	mA	$V_I = 0$; $0\ V \le V_Q \le 4.85$ V
Temperature drift of output voltage	α_{VQ}	−0.5		0.5	mV/K	$6\ V \le V_I \le V_{I\,off}$ $\Delta T_j > 50$ K
Reset Generator						
Switching threshold Switching voltage	V_{RT} V_R V_R	4.4 4.4	4.5	4.6 0.8 V_Q	V V V	 $V_Q < V_{RT}$; $I_R = 10$ mA $V_Q > V_{RT}$
Reverse current Change current	I_R I_{ch}	 10		5 30	µA µA	$V_R > 4.6$ V; $0.5\ V < V_{Cd} < (0.75 \cdot V_Q)$
Reset delay time	t_D / C_D		175		ms/µF	

Characteristics

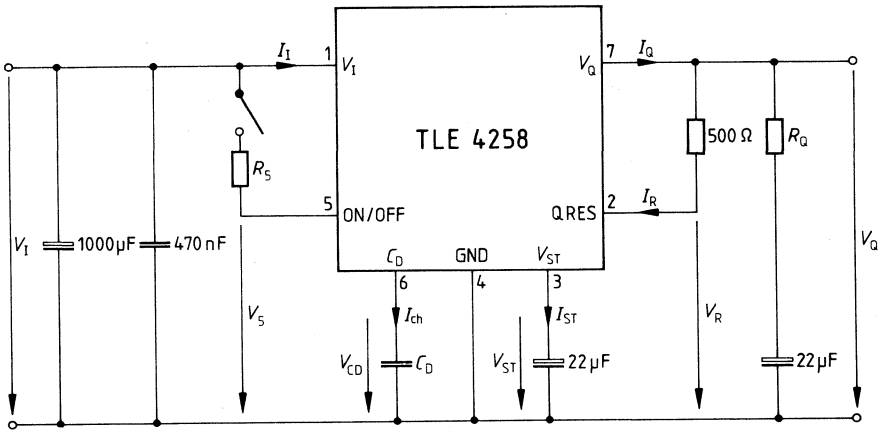
$V_I = 13.5$ V; $T_j = 25$ °C; $V_5 > 3.5$ V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Standby Regulator						$V_5 \leq 0.5$ V
Output voltage	V_{ST}	4.7		5.3	V	0 mA $\leq I_{ST} \leq$ 35 mA 6 V $\leq V_I \leq V_{I\,off}$
	V_{ST}	4.5		6.0	V	0 mA $\leq I_{ST} \leq$ 35 mA $V_{I\,off} \leq V_I \leq$ 70 V; $t_2 \leq$ 400 ms
Current consumption without load	I_{QST}			2	mA	$I_Q = 0$ mA; $I_{ST} = 0$ mA
	I_{QST}			15	mA	$I_Q = 0$ mA; $I_{ST} = 35$ mA
Drop voltage	V_{DrST}			0.75	V	$V_I = 4.5$ V; $I_{ST} = 35$ mA
Static load regulation	$\Delta V_{ST}/\Delta I_{ST}$		1		Ω	6 V $\leq V_I < V_{I\,off}$ 0 mA $\leq I_{ST} \leq$ 35 mA
Supply voltage rejection	$\alpha_{SVR\,ST}$	60			dB	$I_{ST} = 35$ mA; $V_I = 12$ V + 1 V · cos (2 π x 120 Hz · t)
Reverse current	$-I_{ST}$			2	mA	$V_I = 0$ V; 0 V $\leq V_{ST} \leq$ 4.7 V
General Ratings						
Reverse polarity	$-V_Q$		0	0.7	V	$V_I = -15$ V
	$-I_Q$		0	0.5	mA	$V_I = -15$ V
	$-V_{ST}$		0	0.7	V	$V_I = -15$ V
	$-I_{ST}$		0	0.5	mA	$V_I = -15$ V
Synchronous operation V_{ST}; V_Q	$V_{ST}-V_Q$	−200		200	mV	0 mA $\leq I_{ST} \leq$ 35 mA 0 mA $\leq I_Q \leq$ 750 mA 6 V $\leq V_I < V_{I\,off}$
Necessary series resistance	R_5	12	22	24	kΩ	
Switching threshold for main regulator	V_5	3.5			V	$V_Q > 3$ V; $I_Q = 0.5$ A
	V_5			0.5	V	$V_Q < 3$ V; $I_Q = 1$ mA
Load impedance	R_Q		0	2	Ω	$Z_Q = R + (j\ \omega C)^{-1}$

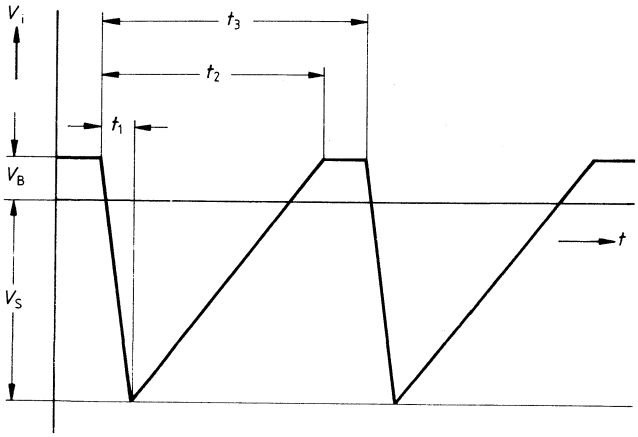
Application Circuit



Test Circuit

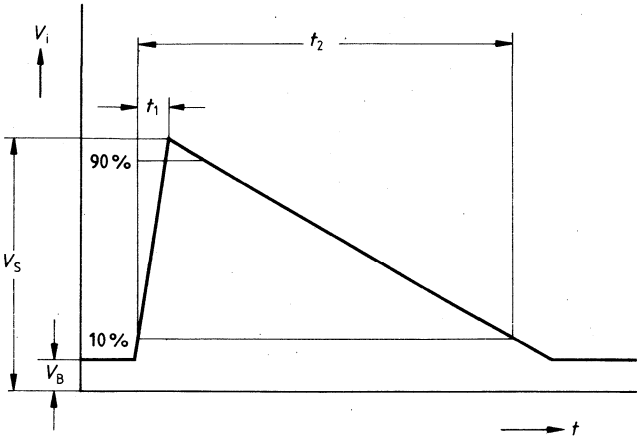


1. Test pulse for negative interference voltages V_i



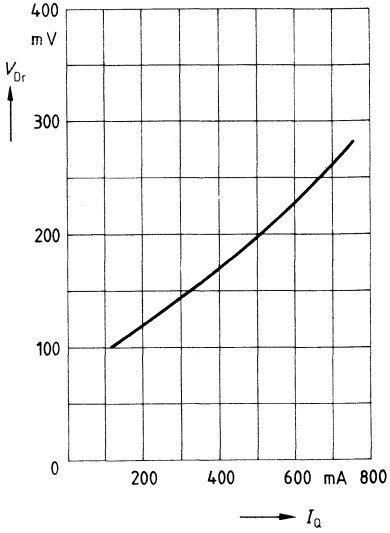
V_B = 14 V t_1 = 10 µs
$|V_S|$ = 70 V t_2 = 2 ms
R_i = 10 Ω t_3 = 0.5 s to 5 s

2. Pulse for load dump at V_{14}

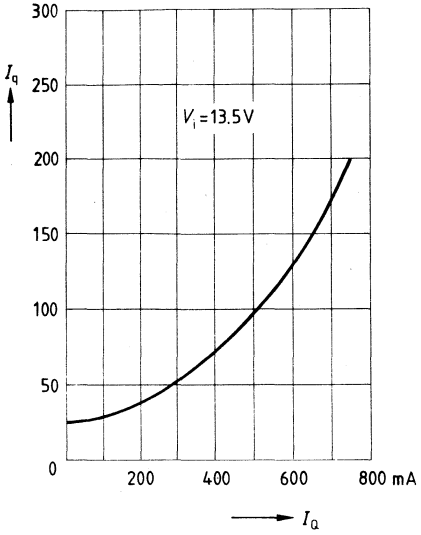


V_B = 14 V t_1 = 5 ms
V_S = 70 V t_2 = 400 ms
R_i = 0.5 Ω

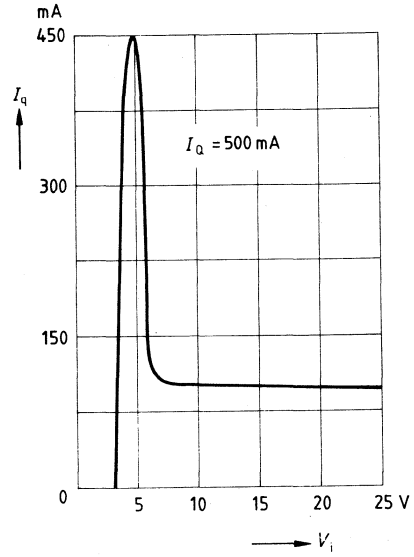
Minimum drop voltage versus output current
$T_V = 25\,°C$; $V_i = 4.5\,V$



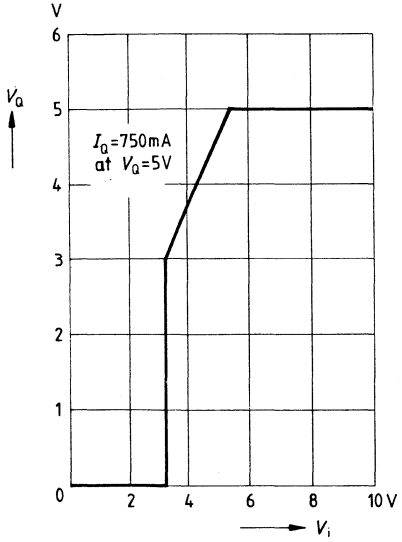
Current consumption without load versus output current
$T_C = 25\,°C$



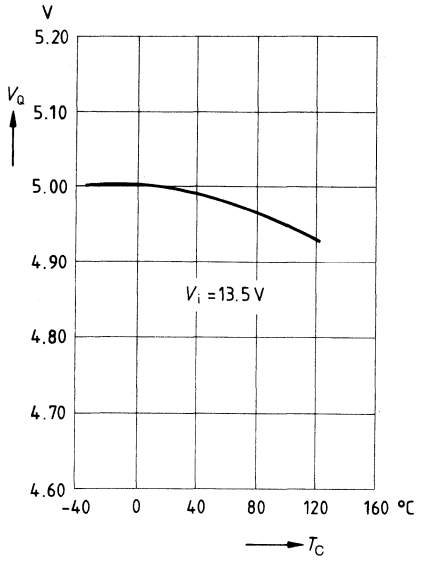
Current consumption without load versus input voltage
$T_C = 25\,°C$



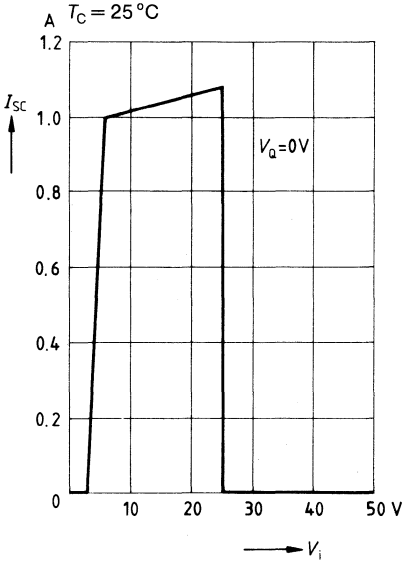
Output voltage versus input voltage
$T_C = 25\,°C$



Output voltage versus temperature



Short-circuit current versus input voltage



SIEMENS

5-V Low-Drop Voltage Regulator

TLE 4260

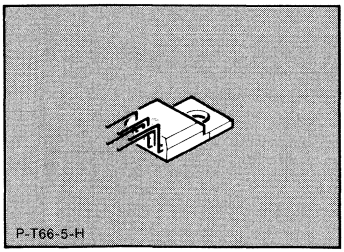
Preliminary Data

Bipolar IC

3

Features

- Low drop voltage
- Very low quiescent current
- Low starting current consumption
- Integrated temperature protection
- Protection against reverse polarity
- Input voltage up to 40 V
- Overvoltage protection up to 65 V
- Short-circuit proof
- Suited for automotive electronics
- Wide temperature range



Type	Ordering Code	Package
S TLE 4260	Q67000-A8187	P-T66-5-H (similar to TO-220)

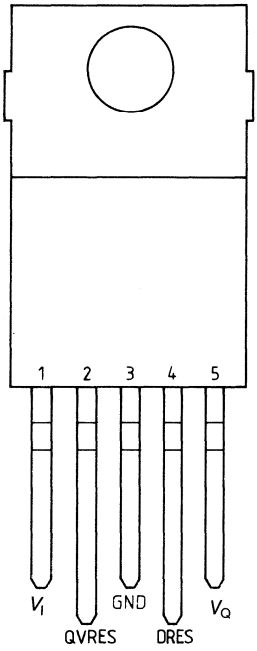
Functional Description

TLE 4260 is a 5-V low-drop fixed-voltage regulator in a P-T66-5-H package. The maximum input voltage is 35 V. The device can produce an output current of more than 500 mA. It is shortcircuit-proof and incorporates temperature protection that disables the circuit at unpermissibly high temperatures.

Due to the wide temperature range of −40 °C to 150 °C, the TLE 4260 is also suitable for use in automotive electronics.

The IC regulates an input voltage V_I in the range $6 < V_I < 35$ V to $V_{Qrated} = 5.0$ V. A reset signal is generated for an output voltage of $V_Q < 4.75$ V. The reset delay can be set externally with a capacitor. If the output current is reduced below 10 mA, the regulator switches internally to standby and the reset generator is turned off. The standby current drops to max. 700 µA.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_I	**Input voltage;** block directly to ground on the IC with a 470-nF capacitor
2	QVRES	**Reset output;** open-collector output controlled by the reset delay
3	GND	**Ground**
4	DRES	**Reset delay;** wired to ground with a capacitor
5	V_Q	**5-V output voltage;** block to ground with a 22-µF capacitor

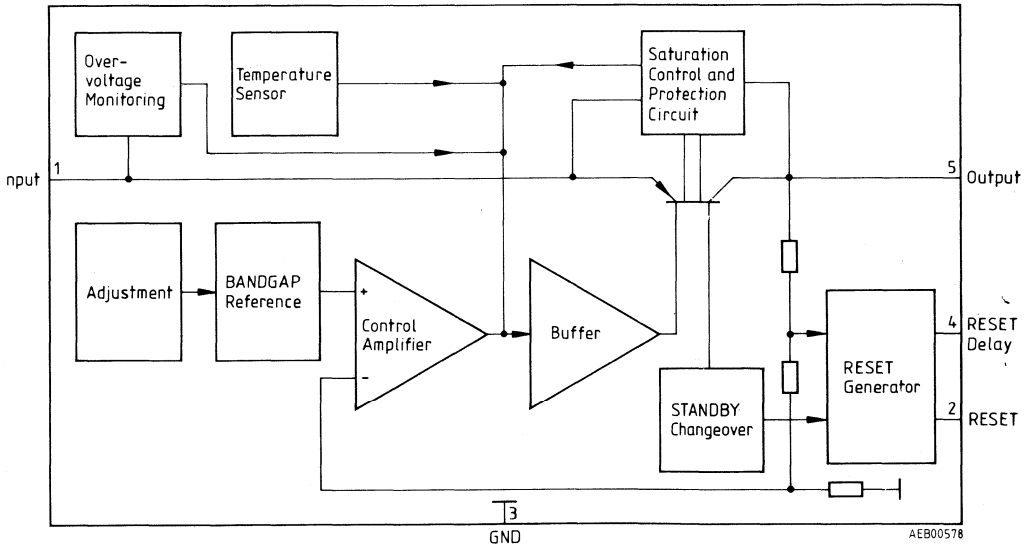
Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage goes below 96% of its typical value, an external capacitor is discharged on pin 4 by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is issued on pin 2 and not cancelled again until the upper threshold V_{DT} is exceeded. For an output current of less than $I_{QN\ Off}$ = 10 mA the standby changeover turns off the reset generator. The latter is turned on again when the output current increases, the output voltage drops below 4.2 V or the delay capacitor is discharged by external measures.

The IC also incorporates a number of internal circuits for protection against:

- overload,
- overvoltage,
- overtemperature,
- reverse polarity.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Input (Pin 1)					
Input voltage	V_I	−42	42	V	
	V_I		65	V	$t \leq 400$ ms
Input current	I_I		1.6	A	
Reset Output (Pin 2)					
Voltage	V_R	−0.3	42	V	
Current	I_R				internally limited
Ground (Pin 3)					
Current	I_{GND}	−0.5		A	
Reset Delay (Pin 4)					
Voltage	V_D	−0.3	42	V	
Current	I_D				internally limited
Output (Pin 5)					
Differential voltage	$V_I - V_Q$	−5.25	V_I	V	
Current	I_Q		1.4	A	
Temperature					
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−50	150	°C	
Operating Range					
Input voltage	V_I		32	V	*)
Junction temperature	T_j	−40	150	°C	
Thermal resistance					
system – air	$R_{th\ SA}$		65	K/W	
system – case	$R_{th\ SC}$		3	K/W	

*) **See diagram** "Output Current versus Input Voltage"

Characteristics

$V_I = 13.5$ V; $T_j = 25$ °C (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.75	5.00	5.25	V	25 mA ≤ I_Q ≤ 500 mA; 6 V ≤ V_I ≤ 28 V; −40 °C ≤ T_j ≤ 125 °C
Output current	I_Q			50	µA	0 V ≤ V_I ≤ 2 V; −40 °C ≤ T_j ≤ 125 °C
Shortcircuit current	I_{SC}	500	1000		mA	V_I = 17 V to 28 V; V_Q = 0 V
Current consumption; $I_q = I_I - I_Q$	I_q		8.5	10	mA*)	6 V ≤ V_I ≤ 28 V; I_Q = 150 mA
Current consumption; $I_q = I_I - I_Q$	I_q		50	65	mA*)	6 V ≤ V_I ≤ 28 V; I_Q = 500 mA
Current consumption; $I_q = I_I - I_Q$	I_q			80	mA*)	V_I ≤ 6 V; I_Q = 500 mA
Drop voltage	V_{Dr}		0.35	0.5	V	V_I = 4.5 V; I_Q = 0.5 A
Drop voltage	V_{Dr}		0.2	0.3	V	V_I = 4.5 V; I_Q = 0.15 A
Load regulation	ΔV_Q		15	35	mV	I_Q = 25 mA to 500 mA
Supply-voltage regulation	ΔV_Q		15	50	mV	V_I = 6 V to 28 V; I_Q = 100 mA
Supply-voltage regulation	ΔV_Q		5	25	mV	V_I = 6 V to 16 V; I_Q = 100 mA
Hum suppression	SVR		54		dB	f_r = 100 Hz; V_r = 0.5 V_{pp}
Temperature drift of output voltage	α_{VQ}		2×10^{-4}		1/°C	
Standby Operation						
Quiescent current; $I_q = I_I - I_Q$	I_q		500	700	µA	10 V < V_I < 16 V; I_Q = 0 mA
Current consumption; $I_q = I_I - I_Q$	I_q		750	850	µA	10 V < V_I < 16 V; I_Q = 5 mA

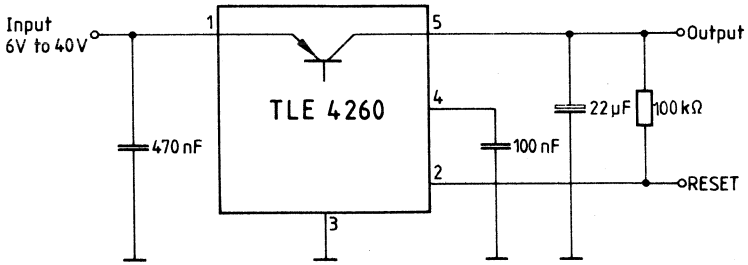
*) **See diagram**

Characteristics

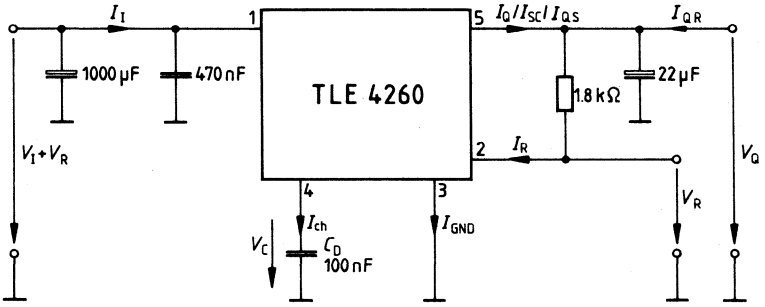
$V_I = 13.5$ V; $T_j = 25$ °C (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Standby Off/Normal On						
Current consumption	I_{qSOff}		1.0	1.2	mA	**see diagram 1**
Current consumption	I_{qNOn}		1.7	2.2	mA	**see diagram 1**
Normal Off/Standby On						
Current consumption	I_{qNOff}		1.55	2.00	mA	**see diagram 1**
Current consumption	I_{qSOn}		850	1050	µA	**see diagram 1**
Switching threshold	I_{QNOff}	7.5	10	12.5	mA	**see diagram 1**
Switching hysteresis	ΔI_Q	2.25	3	4	mA	**see diagram 1**
Reset Generator						
Switching threshold	V_{RT}	94	96	97	%	in % of V_Q $I_Q > 500$ mA; $V_I = 6$ V
Switching voltage	V_R		0.25	0.40	V	$I_R = 3$ mA
Reverse current	I_R			1	µA	$V_R = 5$ V
Charge current	I_{ch}	7	10	13	µA	
Switching threshold	V_{ST}	0.9	1.1	1.3	V	
Delay switching threshold	V_{DT}	2.15	2.50	2.75	V	
Delay time	t_D		25		ms	$C_D = 100$ nF
Delay time	t_t		5		µs	$C_D = 100$ nF
General Data						
Turnoff voltage	V_{IOff}	40	43	45	V	$I_Q < 1$ mA
Turnoff hysteresis	ΔV_I		3.0		V	
Reverse current	I_{QS}		500		µA	$V_Q = 0$ V; $V_I = 45$ V
Reverse output current	I_{QR}			1.5	mA	$V_Q = 5$ V; $V_I =$ open

Application Circuit



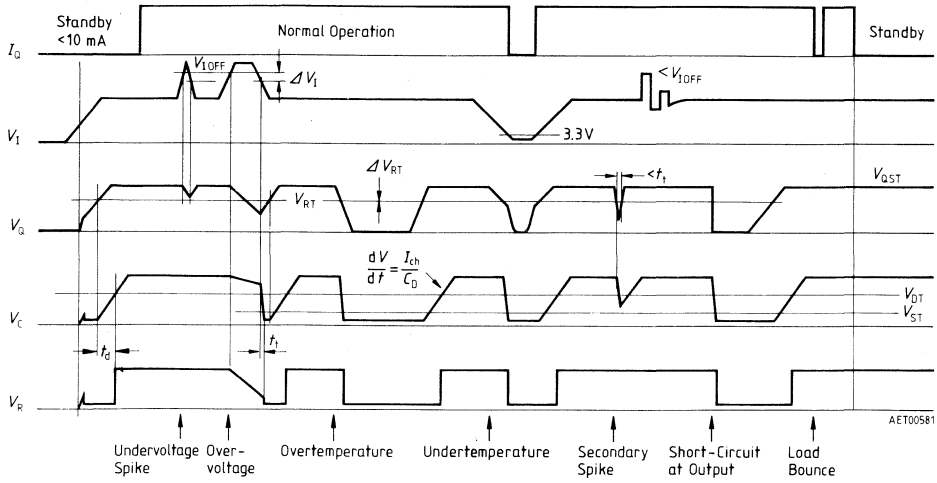
Test Circuit



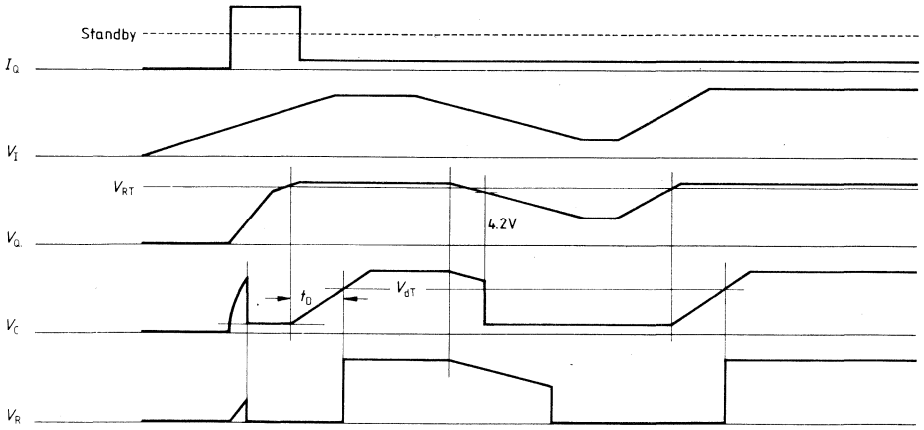
$V_{Dr} = V_I - V_Q$

$SVR = 20 \log \frac{V_R}{\Delta V_Q}$

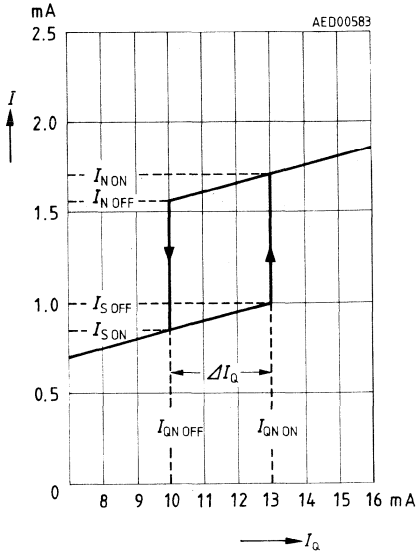
Time Response



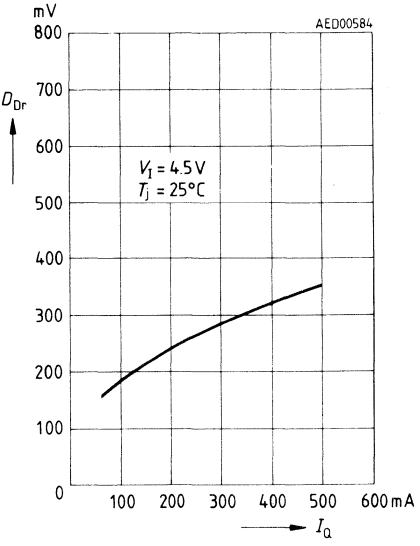
Time Response in Standby Condition



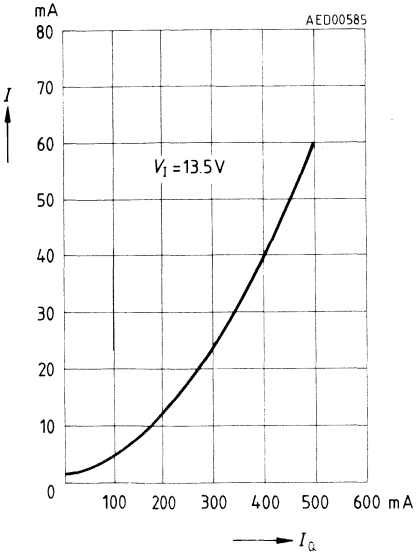
Standby/Normal changeover



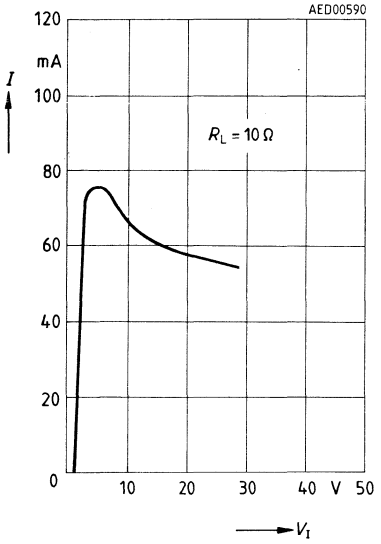
Drop voltage versus output current



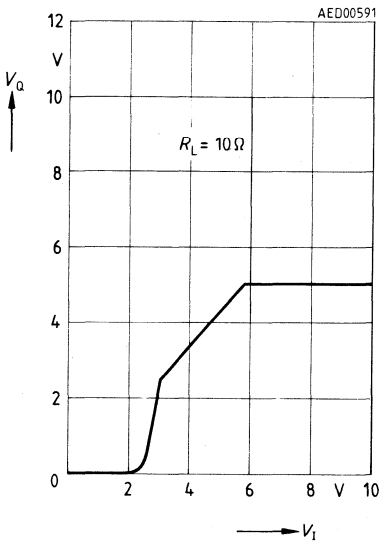
Current consumption versus output current



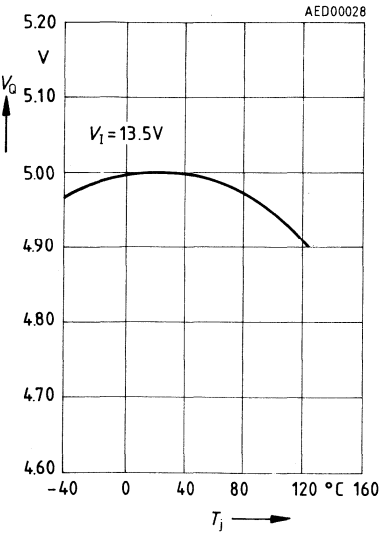
Current consumption versus input voltage



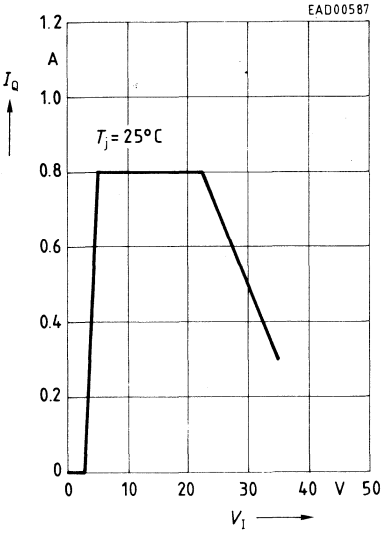
Output voltage versus input voltage



Output voltage versus temperature



Output current versus input voltage



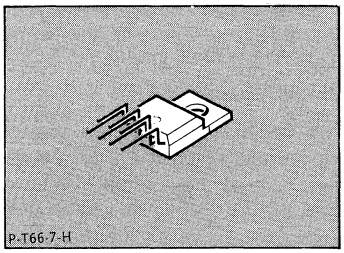
SIEMENS

5-V Low Drop Voltage Regulator

TLE 4261

Preliminary Data

Bipolar IC



Features

- Very low-drop voltage
- Very low quiescent current
- Low starting-current consumption
- Proof against reverse polarity
- Input voltage up to 42 V
- Overvoltage protection up to 65 V
- Shortcircuit-proof
- External setting of reset delay
- Integrated watchdog circuit
- Wide temperature range
- Overtemperature protection
- Suitable for automotive use

Type	Ordering Code	Package
▼ S TLE 4261	Q67000–A9003	P-T66-7-H

▼ New type

Functional Description

TLE 4261 is a 5-V low-drop fixed voltage regulator in a P-T66-7-H package. The maximum input voltage is 40 V. The device can produce an output current of more than 500 mA. It is shortcircuit-proof and incorporates temperature protection that disables the circuit at impermissibly high temperatures.

Application Description

The IC regulates an input voltage V_I in the range V_I = 6 to 40 V to V_{Qrated} = 5.0 V. A reset signal is generated for a maximum output voltage of V_Q less than 4.75 V. The reset delay can be set externally with a capacitor. A connected microprocessor is monitored by the integrated watchdog circuit. Connecting this input to the input voltage makes the watchdog function inactive. The presence of a voltage less than 2 V on the inhibit input disables the regulator. The current consumption drops to max. 50 µA.

Design Notes for External Components

The input capacitor C_I causes a low-resistant powerline and limits the rise times of the input voltage. The IC is protected against rise times up to 100 V/µs. It is possible to damp the tuned circuit consisting of supply inductance and input capacitance with a resistor of approx. 1 Ω in series to C_I.

The output capacitor maintains the stability of the regulating loop. Stability is guaranteed with a rating of 22 µF min. at an ESR of 3 Ω max. in the operating temperature range.

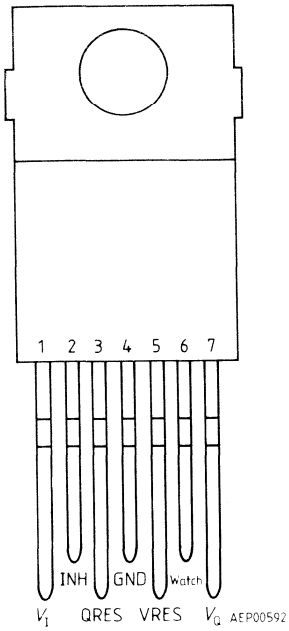
Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and controls the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage drops below 95.5% of its typical value for more than 2 µs, a reset signal is triggered on pin 3 and an external capacitor discharged on pin 5. The reset signal is not cancelled until the voltage on the capacitor has exceeded the upper switching threshold V_{DT}. A positive-edge-triggered watchdog circuit monitors the connected microprocessor and will likewise trigger a reset if pulses are missing. The IC can be disabled by a low level on the inhibit input and the current consumption drops to < 50 µA.

The IC also incorporates a number of circuits for protection against:

- overload,
- overvoltage,
- overtemperature,
- reverse polarity.

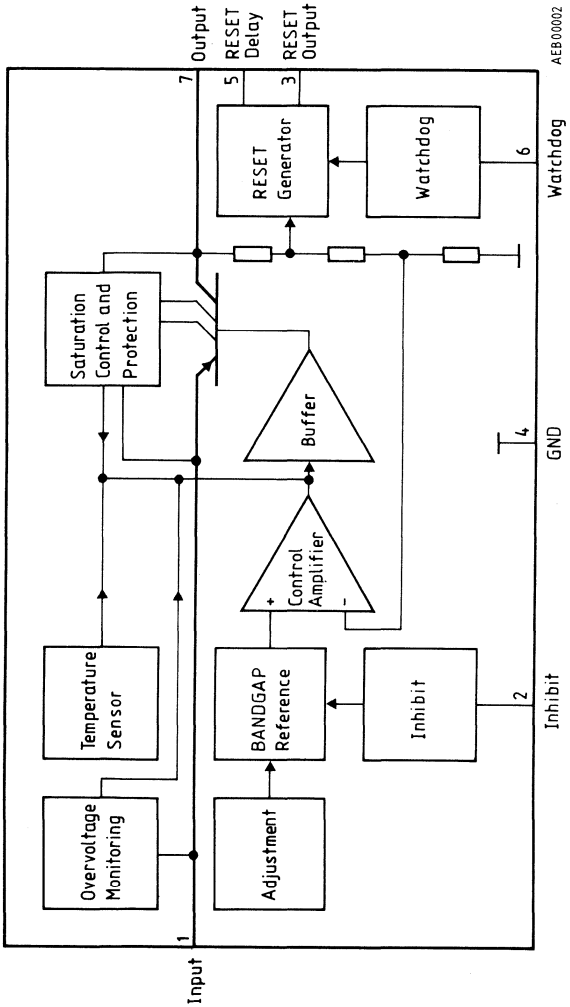
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_I	Input voltage; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vehicle electrical system. Oscillation of the input voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
2	INH	Inhibit; switches off the IC when low.
3	QRES	Reset output; open-collector output controlled by the reset delay.
4	GND	Ground
5	VRES	Reset delay; wired to ground using a capacitor.
6	Watch	Watchdog; monitors the microprocessor when active.
7	V_Q	5 V output; block to ground using a capacitor of ≥ 22 µF. ESR is ≤ 3 Ω in the operating temperature range.

Block Diagram



Absolute Maximum Ratings

$T_j = -40$ to 150 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Input (pin 1)					
Input voltage	V_I	−42	42	V	
Input voltage	V_I		65	V	$t \leq 400$ ms
Input current	I_I		1.6	A	
Inhibit (pin 2)					
Voltage	V_3	−0.3	42	V	
Current	I_3		5	mA	
Reset Output (pin 5)					
Voltage	V_R	−0.3	42	V	
Current	I_R				limited internally
Ground (pin 4)					
Current	I_{GND}		0.5	A	
Reset Delay (pin 3)					
Voltage	V_D	−0.3	42	V	
Current	I_D				limited internally
Watchdog (pin 6)					
Voltage	V_w	−0.3	V_I	V	
Output (pin 7)					
Differential voltage	$V_I - V_Q$	−5.25	V_I	V	
Current	I_Q		1.4	A	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−50	150	°C	
Operating Range					
Input voltage	V_I*		32	V	
	V_I			V	
Junction temperature	T_j	−40	150	°C	
Thermal Resistances					
System-air	$R_{th\ SA}$		65	K/W	
System-case	$R_{th\ SC}$		3	K/W	

*** See diagram**

Characteristics

$V_I = 13.5$ V; $T_j = 25$ °C; $V_2 \geq 6$ V (unless specified otherwise)

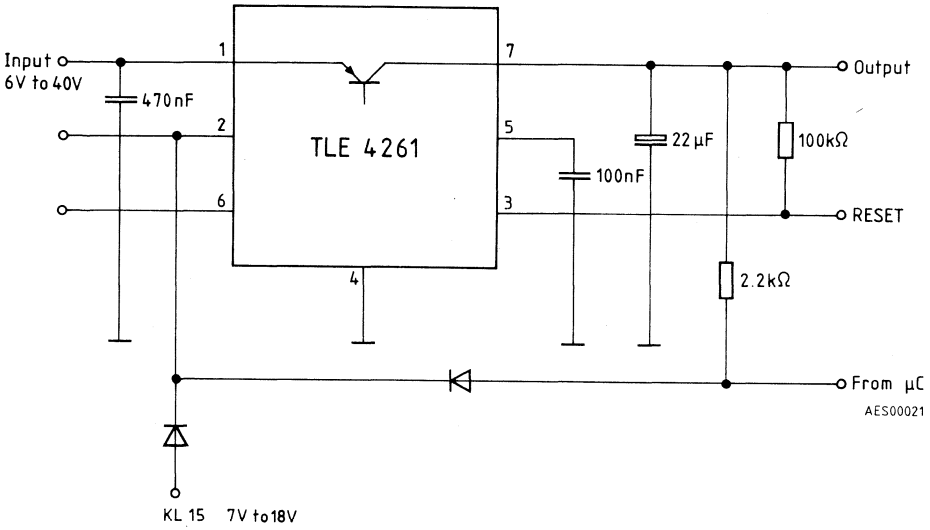
Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.75	5.00	5.25	V	25 mA ≤ I_Q ≤ 500 mA; 6 V ≤ V_I ≤ 28 V; −40 °C ≤ T_j ≤ 125 °C
Output voltage	V_Q	4.85	5.00	5.15	V	25 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 40 V
Output current	I_Q			50	µA	0 V ≤ V_I ≤ 2 V; $V_2 = V_I$; −40 °C ≤ T_j ≤ 125 °C
Output current	I_Q	500	1000		mA	V_I = 17 V to 28 V
Current consumption; $I_q = I_I - I_Q$	I_q		3.5		mA	$I_Q = 0$
Current consumption; $I_q = I_I - I_Q$	I_q		5.0	10	mA	6 V ≤ V_I ≤ 28 V; I_Q = 150 mA
Current consumption; $I_q = I_I - I_Q$	I_q		40	65	mA	6 V ≤ V_I ≤ 28 V; I_Q = 500 mA
Current consumption; $I_q = I_I - I_Q$	I_q		45	80	mA	V_I < 6 V; I_Q ≤ 500 mA
Drop voltage	V_{Dr}		0.35	0.5	V	V_I = 4.5 V; I_Q = 0.5 A
Drop voltage	V_{Dr}		0.2	0.3	V	V_I = 4.5 V; I_Q = 0.15 A
Load regulation	ΔV_Q		15	35	mV	25 mA ≤ I_Q ≤ 500 mA
Supply voltage regulation	ΔV_Q		15	50	mV	6 V ≤ V_I ≤ 28 V I_Q = 100 mA
Supply voltage regulation	ΔV_Q		5	25	mV	6 V ≤ V_I ≤ 16 V I_Q = 100 mA
Hum suppression	SVR		54		dB	f_r = 100 Hz; V_r = 0.5 V_{pp}
Temperature drift of output voltage	α_{VQ}		2×10^{-4}		1/°C	−40 °C < T_j < 150 °C
Inhibit Operation						
Current consumption	I_I			50	µA	V_2 < 2 V; $I_Q = 0$
Current consumption	I_2			600	µA	V_2 = 6 V
Switching threshold for inhibit	V_2	5.0	5.5	6.0	V	IC turned on
Switching threshold for inhibit	V_2	2.0	2.7	3.7	v	IC turned off

Characteristics

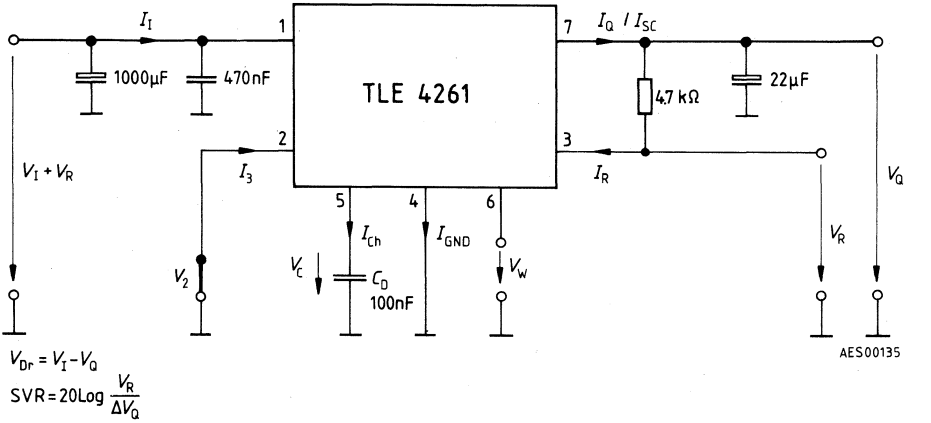
$V_I = 13.5$ V; $T_j = 25$ °C; $V_2 \geq 6$ V (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Reset Generator						
Switching threshold	V_{RT}	94	95.5	97	%	in % of V_Q $I_Q > 500$ mA; $V_I = 6$ V
Saturation voltage, reset output	V_R		0.25	0.40	V	$I_R = 1$ mA
Reverse current	I_R			1	µA	$V_R = 5$ V
Charge current	I_{ch}	18.75	25	31.25	µA	
Switching threshold	V_{ST}	0.9	1	1.1	V	
Delay switching threshold	V_{DT}	2.25	2.50	2.75	V	
Saturation voltage, delay output	V_C			100	mV	$V_I = 4.5$ V and I_{ch}
Delay time	t_D		10		ms	$C_D = 100$ nF
Delay time	t_t		2		µs	
Watchdog						
Turnoff voltage	V_w	5.2	5.6	6.0	V	
Discharge current	I_{CD}		7.5		µA	$V_C = 1.5$ V
Switching voltage	V_{CD}		3.05		V	
Pulse interval	T_w		35		ms	$C_D = 100$ nF
General Data						
Turnoff voltage	V_{IOff}	41	43	45	V	$I_Q < 1$ mA
Turnoff hysteresis	ΔV_I		6.5		V	
Reverse current	I_{QS}			50	µA	$V_Q = 0$ V; $V_I = 45$ V
Reverse output current	I_{QR}			1.5	mA	$V_Q = 5$ V; V_I and V_2 open

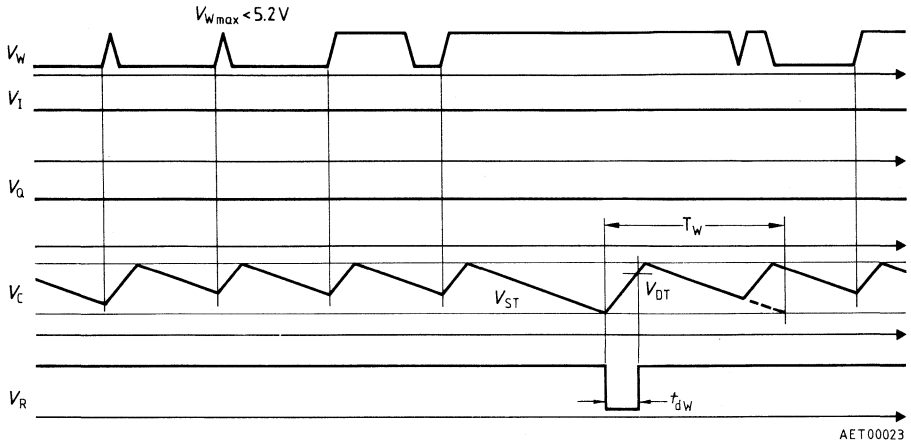
Application Circuit



Test Circuit 1

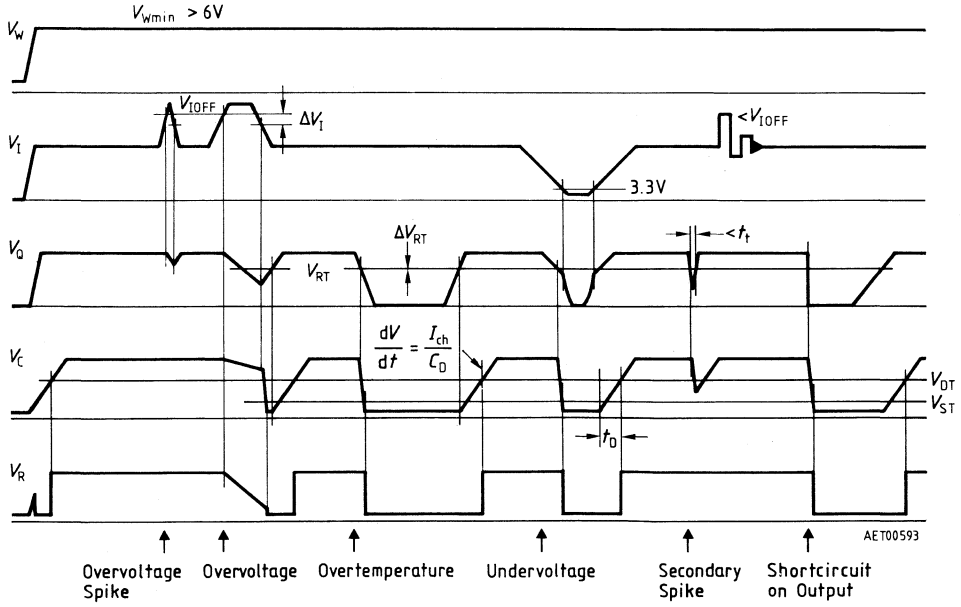


Time Response in Watchdog Condition

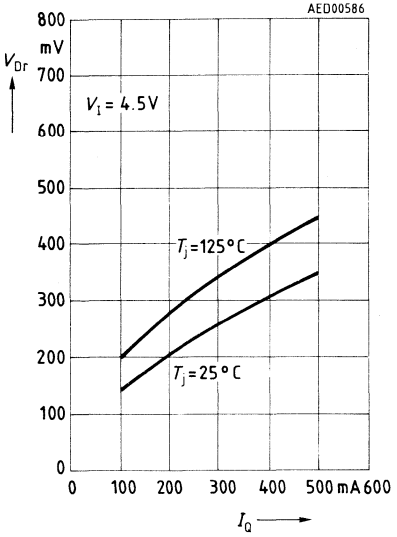


$$t_W = \frac{(V_{CD} - V_{ST})\,(I_{CD} + I_D)}{I_D \times I_{CD}}\ C_D;\ t_{dw} = \frac{(V_{DT} - V_{ST})}{I_D}\ C_D$$

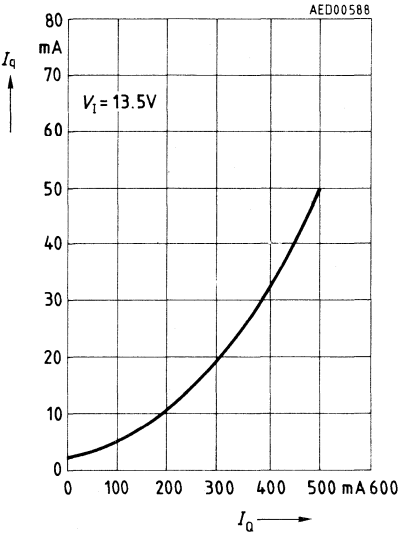
Timing with Watchdog Off



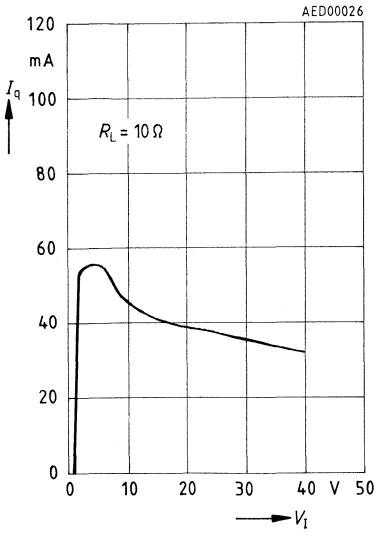
Drop voltage versus output current



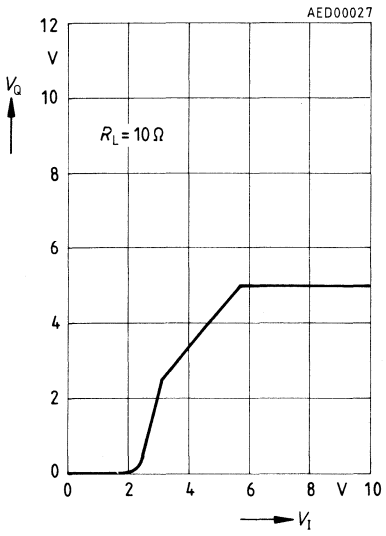
Current consumption versus output current



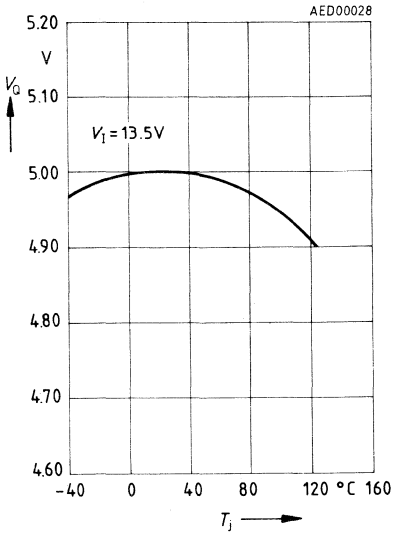
Current consumption versus input voltage



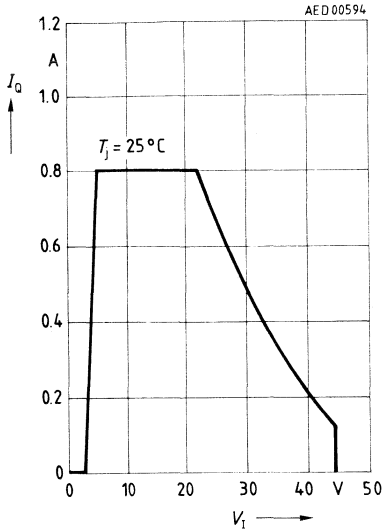
Output voltage versus input voltage



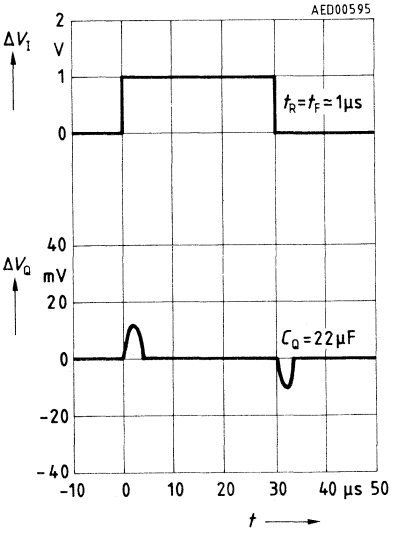
Output voltage versus temperature



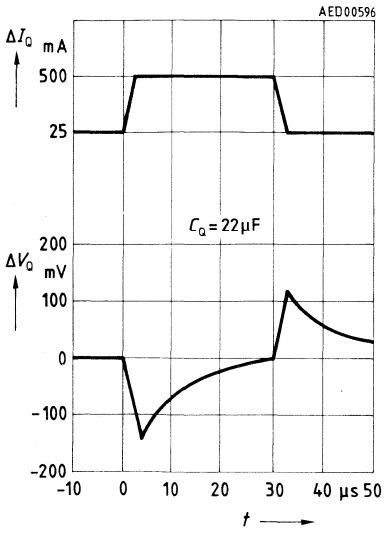
Output current versus input voltage



Input step response



Load step response



Treiber und Interfaceschaltungen
Transistor Arrays

Drivers and Interface Circuits,
Transistor Arrays

Selector Guide

Type	Package	Function	Supply voltage V_S (V_{CEO}) V	Temperature range T_A °C	Page
Driver and Interface Circuits					
FZL 4145 D	P-DIP-18	Short-circuit proof driver for power transistors with short-circuit signaling output	4.5 to 35	−25 to 85	289
Transistor Arrays					
TCA 671	P-DIP-14	Transistor array 5 NPN transistors	42	−25 to 85	297
TCA 671 G	P-DSO-14 (SMD)		42	−25 to 85	297
TCA 871	P-DIP-14		32	−25 to 85	297
TCA 871 G	P-DSO-14 (SMD)		32	−25 to 85	297
TCA 971	P-DIP-14		42	−25 to 85	297
TCA 971 G	P-DSO-14 (SMD)		42	−25 to 85	297
TCA 991	P-DIP-14		32	−25 to 85	297
TCA 991 G	P-DSO-14 (SMD)		32	−25 to 85	297

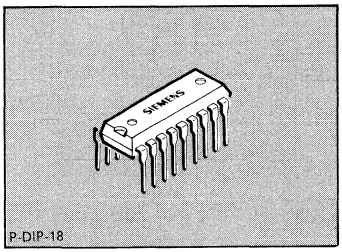
Quad Drivers Incl. Short-Circuit Signalling

FZL 4145 D

Bipolar IC

Features

- Short-circuit shutdown with clock generator
- Four driver circuits for controlling power transistors
- Overload and short-circuit signalling



Type	Ordering Code	Package
S FZL 4145 D	Q67000-H8437	P-DIP-18

General Description

The IC comprises four driver circuits capable of driving power transistors for high output currents. The output transistors are protected against short-circuit to ground and supply voltage. The input threshold can be adjusted between 1.5 V and 7 V. Overload or short-circuit failure at an output will be indicated at pin SQ (signalling output).

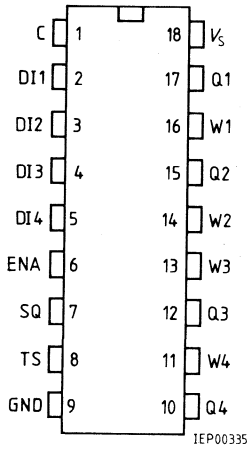
Functional Description

Each driver circuit has one active high driver input DI and a common enable input (ENA) (active high) is provided for all stages. The (Q) outputs are designed to drive the output transistors. The load current is sampled via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-on again is provided by the built-in clock generator. Its operation requires an external capacitor C_T at pin C. If C_T is bridged by a break-key, switching on can only be carried out by operating a key. The duty cycle of the clock generator is 1:50 (e.g. 40 µs/2 ms with $C_T = 33$ nF).

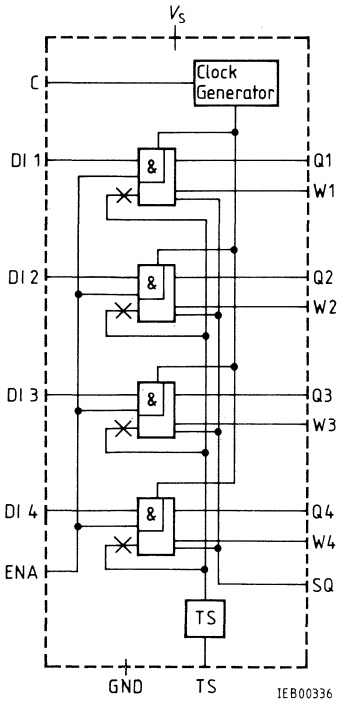
In case of overcurrent or short-circuit failure at any output stage the signalling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching on by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload exists. SQ is an open-collector output.

Unused W pins must be connected to V_S. Open W pins would simulate a short-circuit and activate the signalling output.

Pin Configuration
top view



Block Diagram



DI	Driver inputs
ENA	Enable input
C	Clock capacitor
Q	Outputs
TS	Input for threshold switching
W	Input for output current limiter
SQ	Signalling output
GND	Ground

The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

$V_{TS} = 0$ V; input threshold = 1.5 V (for 5 V logic)
$V_{TS} = 0$ to 5 V; input threshold = V_{TS} +1.5 V
$V_{TS} = V_S$: input threshold = 7 V (for 12/15 V and 24/28 V logic)

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between $V_S = 0$ V and $V_S = 35$ V.

The inputs are protected with clamp diodes.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage	V_S	−0.3	35	V	
	V_S	−0.3	45	V	100 ms duration, 1 s interval
Input voltage at DI and ENA	$V_{DI, ENA}$	−0.3	35	V	1)
Voltage at TS and SQ	$V_{TS, SQ}$	−0.3	45	V	
Output voltage V_Q and voltage at C	V_Q, V_C	−0.3	V_S	V	
Voltage at W	V_W	V_S −5	V_S	V	3)
Input current at DI and ENA	$I_{DI, ENA}$	−3	1	mA	2)
	$I_{DI, ENA}$	−6	2	mA	2) 100 ms duration, 1 s interval
	$I_{DI, ENA}$	−6	5	mA	2) 100 µs duration, 1 ms interval
Output current at SQ	I_{SQ}		8	mA	
Power dissipation of all input diodes	P_{tot}		50	mW	
Storage temperature	T_{stg}	−65	125	°C	
Thermal resistance system – air	$R_{th\ SA}$		65	K/W	
system – case	$R_{th\ SC}$		45	K/W	

Operating Range

Supply voltage for input threshold 1.5 V	V_S	4.5	35	V	$V_{TS} = 0$ V
1.5 V to 6.5 V	V_S	V_{TS} +4.5	35	V	$V_{TS} = 0$ V to 5 V
7 V	V_S	10	35	V	$V_{TS} = V_S$
Ambient temperature	T_A	−25	85	°C	

Notes: 1) $V_{DI, ENA} > 35$ V requires a protective resistor before DI, ENA.
2) $V_{DI, ENA}$ may increase to more than 35 V during current nodes.
3) Unused W connections must be connected to V_S.

Characteristics

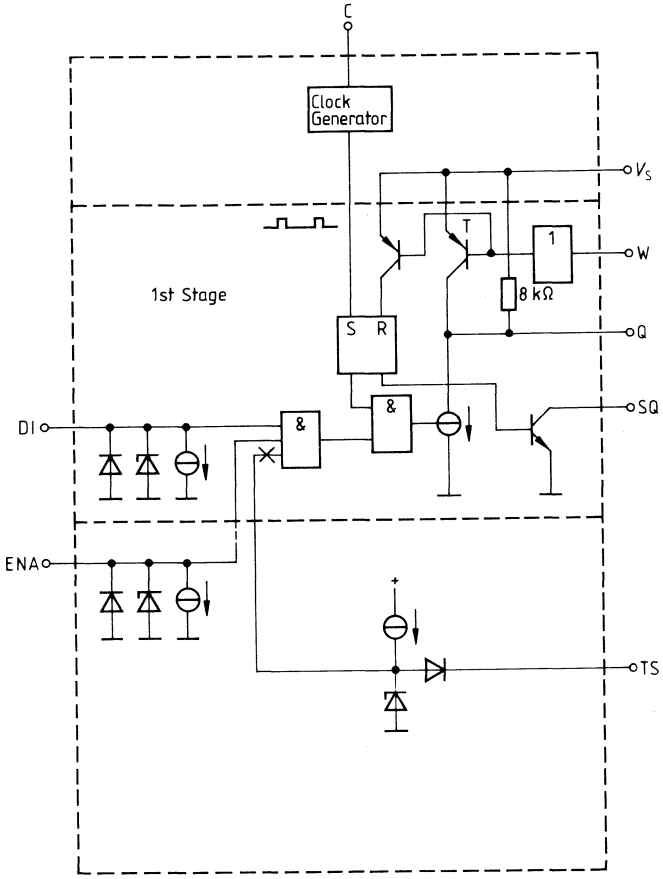
Supply voltage $4.5\ V \leq V_S \leq 30\ V$

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_S		6	8.5	mA	$V_{ENA} = 0\ V$, $V_W = V_S$
H-input voltage at DI, ENA	V_{IH}	2			V	$V_{TS} = 0\ V$
H-input voltage at DI, ENA	V_{IH}	8			V	$V_{TS} = V_S$
L-input voltage at DI, ENA	V_{IL}			0.7	V	$V_{TS} = 0\ V$
L-input voltage at DI, ENA	V_{IL}			6	V	$V_{TS} = V_S$
Input current at DI, ENA	$I_{DI, ENA}$	50		200	µA	$0.5\ V \leq V_{DI, ENA} \leq 30V$
L-output voltage at SQ	V_{SQL}			0.5	V	$I_{SQ} = 5\ mA$
Output current available[1]	I_Q	1.5	2.5		mA	$V_Q = V_S - 1.5\ V$
	I_Q	1.7			mA	$T_A = 0\,°C$, $V_Q = V_S - 1.5\ V$
Current from TS	$-I_{TS}$		2	10	µA	$V_{TS} = 0\ V$
Switching threshold at W	V_W	$V_S-0.6$	$V_S-0.5$	$V_S-0.4$	V	
Current in W	I_W			100	µA	
Current from C	$-I_C$	12	20	34	µA	$T_A = 20\,°C$
Current in C	I_C	0.6	1	1.7	mA	$T_A = 20\,°C$
Upper switching threshold at C	V_{CU}	1.6	2.1	1.7	V	$T_A = 20\,°C$
Lower switching threshold at C	V_{CL}	0.6	0.9	1.2	V	$T_A = 20\,°C$
Saturation voltage at T[2]	V_{QR}		$V_S-0.3$		V	$V_W = V_S-2V$, $I_Q=0$
H-output voltage	V_{QH}	$V_S-0.25$	$V_S-0.02$		V	$V_{ENA} = 0\ V$

[1] The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.

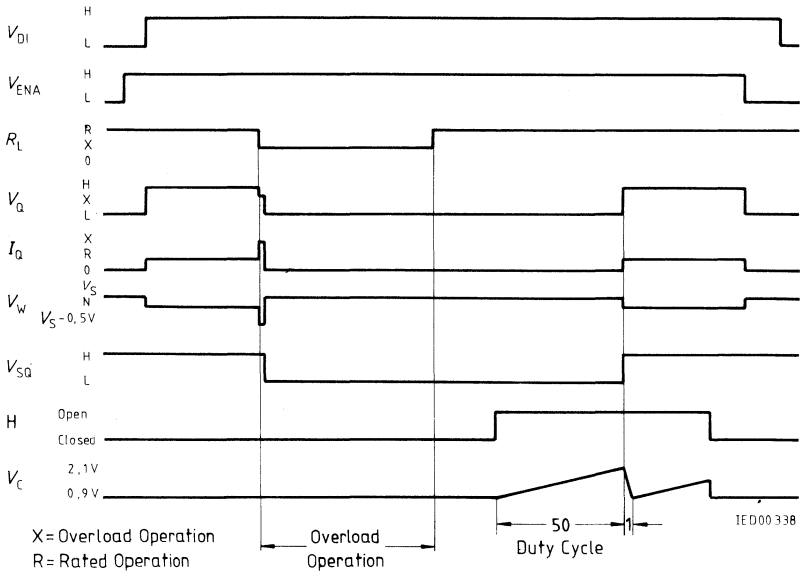
[2] See block diagram

Schematic Circuit Diagram of One Stage

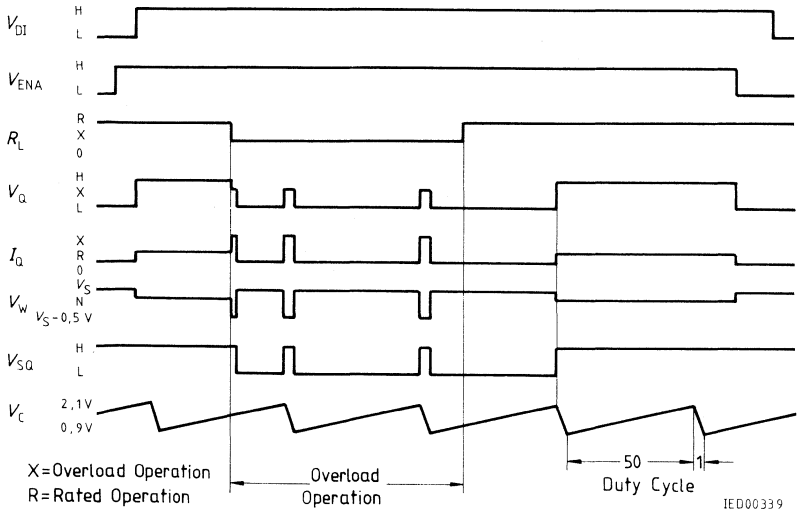


DI Driver input
ENA Enable input
C Clock capacitor
SQ Signalling output
Q Output
TS Input for threshold switching
W Input for output current limiter

Mode of Operation: Switching-On again after Overload with Key H



Mode of Operation: Automatic Switching-On again after Overload



Typical Application Circuits

The load conditions at Q depend on the permissible power dissipation of the used power transistors. The pulsed power dissipation in case of a short circuit must be observed.

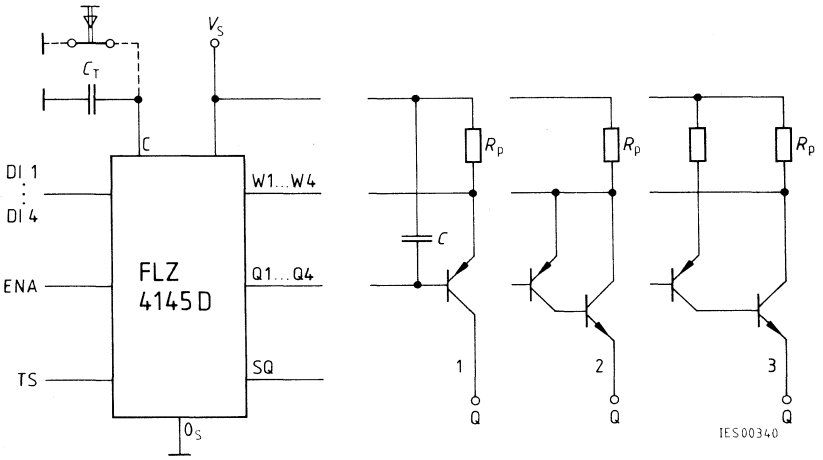
In order to suppress oscillations of the power stage in case of a short circuit, a capacitor C at Q1 to Q4 is necessary if e.g. fast switching transistors are used.

Typical value X of C: approx. 20 nF.

The output circuit 1 is suited for currents up to approx. $I_Q = 100$ mA.

The output circuits 2 and 3 are suited for currents up to approx. $I_Q = 2$ A. A minimum power dissipation can be achieved with circuit 3.

A break key in parallel to C_T allows a manual switch-on in case of short-circuit.



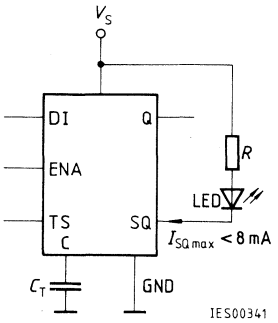
R_P = Precision resistor (current measurement)
$C_T = 0.8 \times t_p$ (nF, µs)
t_p = Short-circuit current pulse length

Note

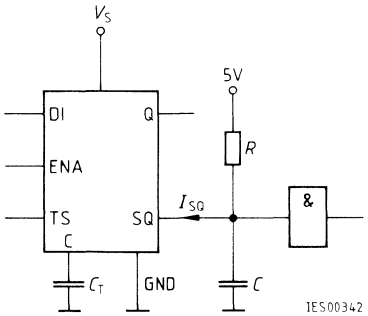
Circuit 1 does not permit a capacitor between Q1 and Q4 and the collector.
Circuit 2 does not permit a capacitor between Q1 and Q4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

Typical Application of Short-Circuit Signalling Output SQ

1. LED Display



2. TTL/CMOS/LSL Driving



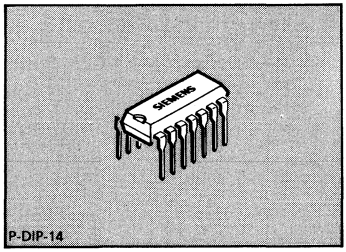
If the pulses appearing at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of $I_{SQ} = 1$ mA a capacitor C of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on C_T) to 1 V. Signalling occurs after approx. 50 µs.

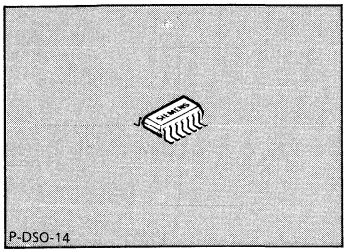
Transistor Array with 5 NPN Transistors

TCA 671
TCA 871
TCA 971
TCA 991
Bipolar IC

Features

- Versatile use
- Slight V_{BE} and B deviations
- High output current
- Good thermal matching
- TCA 971; G/TCA 991; G compatible with 3045/46/86 and 3146





Type	Ordering Code	Package
TCA 671	Q67000-T1	P-DIP-14
TCA 671 G	Q67000-A2366	P-DSO-14 (SMD)
TCA 871	Q67000-T2	P-DIP-14
TCA 871 G	Q67000-A2367	P-DSO-14 (SMD)
TCA 971	Q67000-T11	P-DIP-14
TCA 971 G	Q67000-A8075	P-DSO-14 (SMD)
TCA 991	Q67000-T12	P-DIP-14
TCA 991 G	Q67000-A8076	P-DSO-14 (SMD)

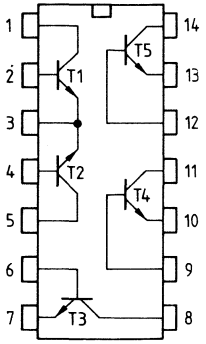
TCA 671, TCA 871, TCA 971, and TCA 991 are monolithic integrated transistor arrays each consisting of five NPN transistors. The arrays are well suited for switching and amplifying applications up to approx. 30 MHz. Due to a uniform design, the transistor characteristics show only slight deviations. The arrays are preferably intended for lamp drivers, amplifiers, pulse generators, and types TCA 971 and TCA 991 especially for discrete differential amplifiers.

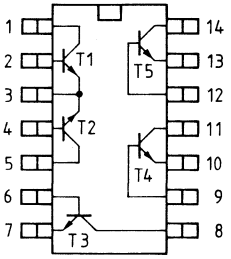
Pin Configurations
(top view)

TCA 671, TCA 871 substrate = pin 3
TCA 971, TCA 991 substrate = pin 13

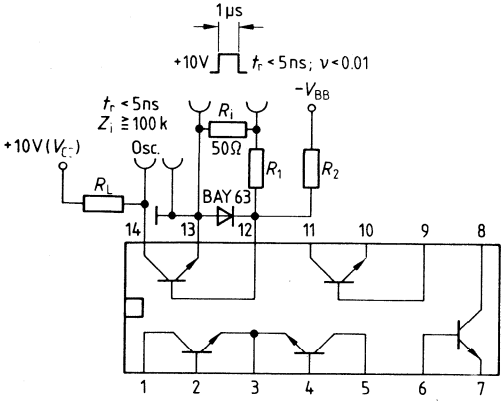
TCA 671 G, TCA 871 G,
TCA 971 G, TCA 991 G

Substrate connection has to be on the most negative potential.





Test Circuit for Switching Times



Switching Times

I_C: I_{B1}: $-I_{B2} \approx 10:1:1$ mA; $R_1 = 5$ kΩ; $R_2 = 5$ kΩ; $V_{BB} = 3.5$ V; $R_L = 990$ Ω
t_{ON} 85 (< 150) ns t_{OFF} 480 (< 800) ns

I_C: I_{B1}: $-I_{B2} \approx 100:10:10$ mA; $R_1 = 500$ Ω; $R_2 = 700$ Ω; $V_{BB} = 5$ V; $R_L = 98$ Ω
t_{ON} 55 (< 150) ns t_{OFF} 450 (< 800) ns

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		TCA 671 TCA 971	TCA 871 TCA 991	
Collector-base breakdown voltage	V_{CB0}	45	35	V
Collector-emitter breakdown voltage	V_{CE0}	42	32	V
Emitter-base breakdown voltage	V_{EB0}	6	6	V
Collector-substrate voltage ($I_C = 100\ \mu A$)	V_{CS}	70	60	V
Collector current	I_C	200	200	mA
Base current	I_B	10	10	mA
Permissible power dissipation for a single transistor	P_{tot}	300	300	mW
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−40 to 125	−40 to 125	°C
Thermal resistance system – air TCA 671 G; TCA 871 G;	$R_{th\ SA}$	85	85	K/W
TCA 971 G; TCA 991 G	$R_{th\ SA}$	145	145	K/W

Operating Range

Ambient temperature	T_A	−25 to 85	−25 to 85	°C

Characteristics

$T_A = 25\,°C$

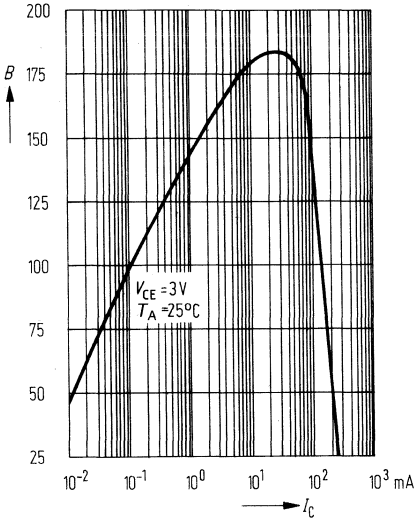
Parameter	Symbol	Limit Values TCA 671 TCA 971			Limit Values TCA 871 TCA 991			Unit
		min.	typ.	max.	min.	typ.	max.	
Differential base current for transistors T1 = T2 at $V_{CE} = 3$ V, $I_C = 1$ mA	I_{BD}		0.5	1		1		µA
Base-emitter voltage at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BE}		0.65			0.65		V
Differential base-emitter voltage for transistors T1 + T2 at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BED}		2	5		4		mV
Differential base-emitter voltage for transistors T3 to T5 at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BED}		4	10		6		mV
Temperature coefficient of base-emitter voltage at $V_{CE} = 3$ V, $I_C = 1$ mA	$\frac{\Delta V_{BE}}{\Delta T}$		−2			−2		mV/K
Transition frequency	f_T	300	550		300	550		MHz

Characteristics

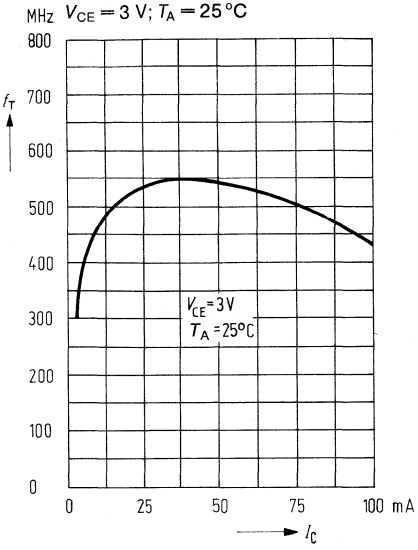
$T_A = 25\,°C$

Parameter	Symbol	Limit Values TCA 671 TCA 971			Limit Values TCA 871 TCA 991			Unit
		min.	typ.	max.	min.	typ.	max.	
Collector-base breakdown voltage at $I_C = 100\ \mu A$, $I_E = 0$	V_{CB0}	45			35			V
Collector-emitter breakdown voltage at $I_C = 100\ \mu A$, $I_B = 0$	V_{CE0}	42			32			V
Collector-substrate breakdown voltage at $I_C = 100\ \mu A$, $I_{CS} = 0$	V_{CS}	70			60			V
Emitter-base breakdown voltage at $I_E = 100\ \mu A$, $I_C = 0$	V_{EB0}	6			6			V
Collector-emitter saturation voltage at $I_C = 50$ mA; $I_B = 5$ mA	$V_{CE\ Sat}$		200	350		200	350	mV
Collector-base cutoff current at $V_{CB} = 25$ V, $I_E = 0$	I_{CB0}		0.02	1		0.02	10	µA
Collector-emitter cutoff current at $V_{CE} = 25$ V, $I_B = 0$	I_{CE0}			1			10	µA
Static current gain	B							
at $V_{CE} = 3$ V, $I_C = 100\ \mu A$		40	80		40	80		
at $V_{CE} = 3$ V, $I_C = 1$ mA		100	140		100	140		
at $V_{CE} = 3$ V, $I_C = 10$ mA		100	160		100	160		
at $V_{CE} = 3$ V, $I_C = 100$ mA		40	100		40	100		

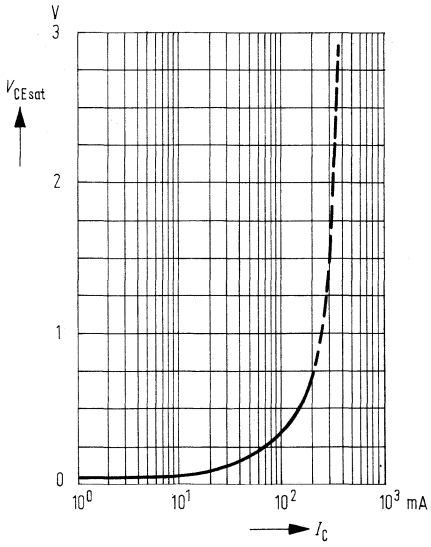
Current gain versus collector current
$V_{CE} = 3$ V; $T_A = 25$ °C



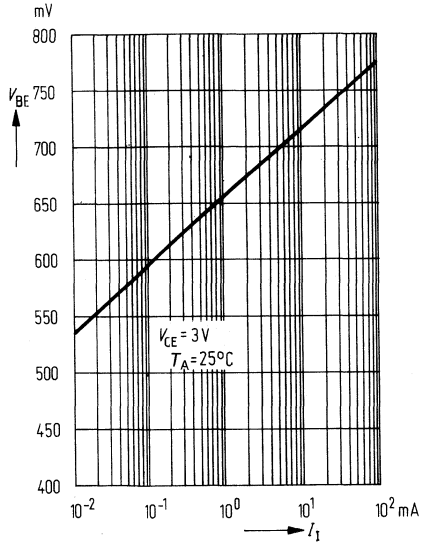
Transition frequency versus collector current
$V_{CE} = 3$ V; $T_A = 25$ °C



Collector-emitter saturation voltage versus collector current
$B = 20$

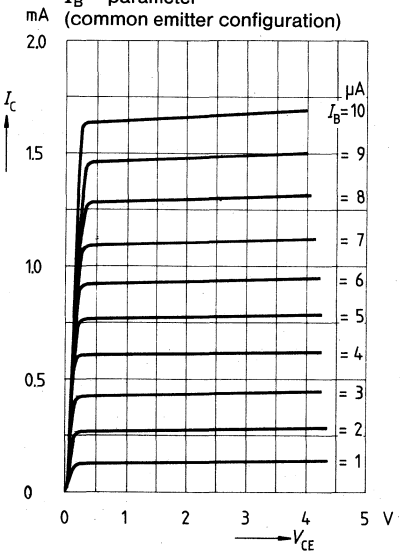


Base-emitter voltage versus input current
$V_{CE} = 3$ V; $T_A = 25$ °C

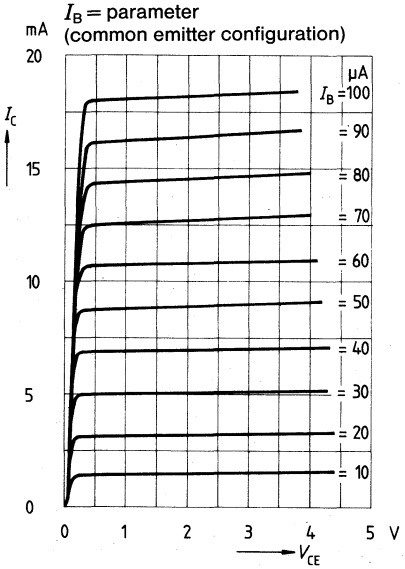


4

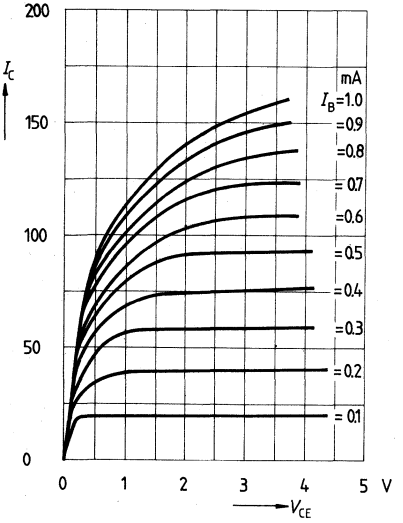
Output characteristics
Collector current versus collector-emitter voltage
I_B = parameter
(common emitter configuration)



Output characteristics
Collector current versus collector-emitter voltage
I_B = parameter
(common emitter configuration)



Output characteristics
Collector current versus collector-emitter voltage
I_B = parameter
(common emitter configuration)



Selector Guide

Type	Package	Function	Technical Data		Page
			Supply voltage V_S (V_{CEO}) V	**Temperature range** T_A °C	
TCA 785	P-DIP-16	Phase control for thyristors, triacs, transistors, 250 mA output current	8 to 18	−25 to 85	305
TLE 3101 TLE 3102 TLE 3103 TLE 3104	P-DIP-18 P-DIP-14 P-DIP-14 P-DIP-8	Phase control for design of control ICs. Typical applications: motor control for kitchen appliances, brightness and temperature control	V_S = 10 to 30 V I_S = typ. 2.4 mA		320
SLB 0586 A	P-DIP-8	Electronic CMOS brightness control	V_S = −4.8 to −5.8 V		337
SLB 0586 G	P-DSO-8	Electronic CMOS brightness control	V_S = −4.8 to −5.8 V		337

= SMD

SIEMENS

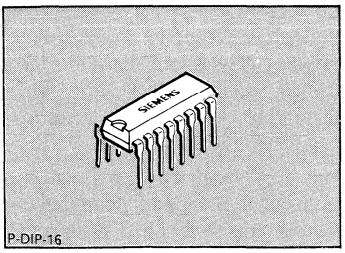
Phase Control IC

TCA 785

Bipolar IC

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range



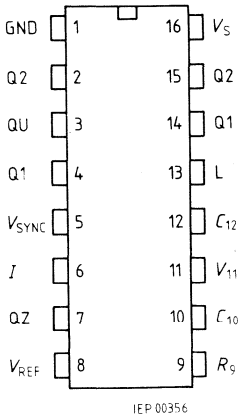
Type	Ordering Code	Package
TCA 785	Q67000-A2321	P-DIP-16

5

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0° and 180°. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.

Pin Configuration



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$\overline{Q}$ 2	Output 2 inverted
3	Q U	Output U
4	$\overline{Q}$ 1	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	Q Z	Output Z
8	V_{REF}	Stabilized voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q 1	Output 1
15	Q 2	Output 2
16	V_S	Supply voltage

Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q1 and Q2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

Outputs $\overline{Q}1$ and $\overline{Q}2$ supply the inverse signals of Q1 and Q2.

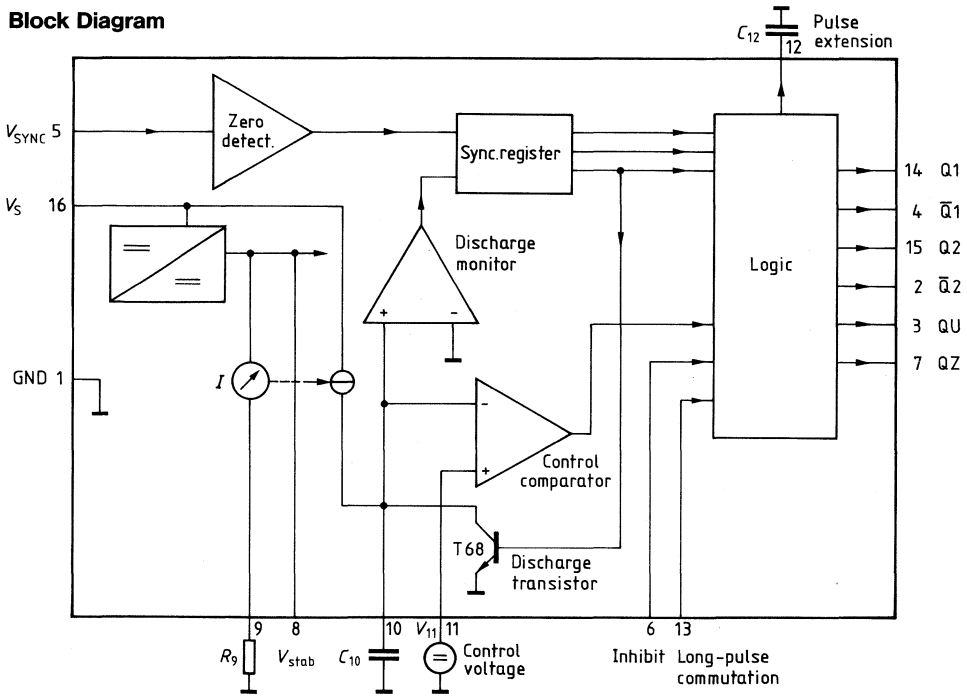
A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.

A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

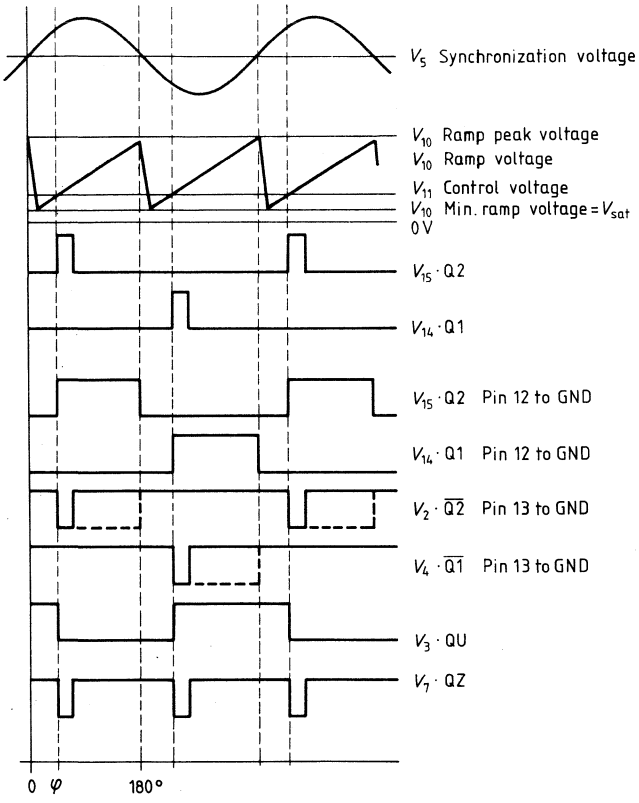
The inhibit input can be used to disable outputs Q1, Q2 and $\overline{Q}1$, $\overline{Q}2$.

Pin 13 can be used to extend the outputs $\overline{Q}1$ and $\overline{Q}2$ to full pulse length (180° – φ).

Block Diagram



Pulse Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S	−0.5	18	V
Output current at pin 14, 15	I_Q	−10	400	mA
Inhibit voltage Control voltage Voltage short-pulse circuit	V_6 V_{11} V_{13}	−0.5 −0.5 −0.5	V_S V_S V_S	V V V
Synchronization input current	I_5	−200	±200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature Storage temperature	T_j T_{stg}	 −55	150 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$		80	K/W

Operating Range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature	T_A	−25	85	°C

Characteristics

$8 \le V_S \le 18$ V; $-25\,°C \le T_A \le 85\,°C$; $f = 50$ Hz

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Circuit
Supply current consumption S1...S6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	4.5	6.5	10	mA	1
Synchronization pin 5 Input current R_2 varied Offset voltage	 $I_{5\ rms}$ ΔV_5	 30 	 30	 200 75	 µA mV	 1 4
Control input pin 11 Control voltage range Input resistance	 V_{11} R_{11}	 0.2 	 15	 $V_{10\ peak}$ 	 V kΩ	 1 5
Ramp generator Charge current Max. ramp voltage Saturation voltage at capacitor Ramp resistance Sawtooth return time	 I_{10} V_{10} V_{10} R_9 t_f	 10 100 3 	 225 80	 1000 V_2-2 350 300 	 µA V mV kΩ µs	 1 1.6 1 1

Characteristics

$8 \le V_S \le 18$ V; $-25\,°C \le T_A \le 85\,°C$; $f = 50$ Hz

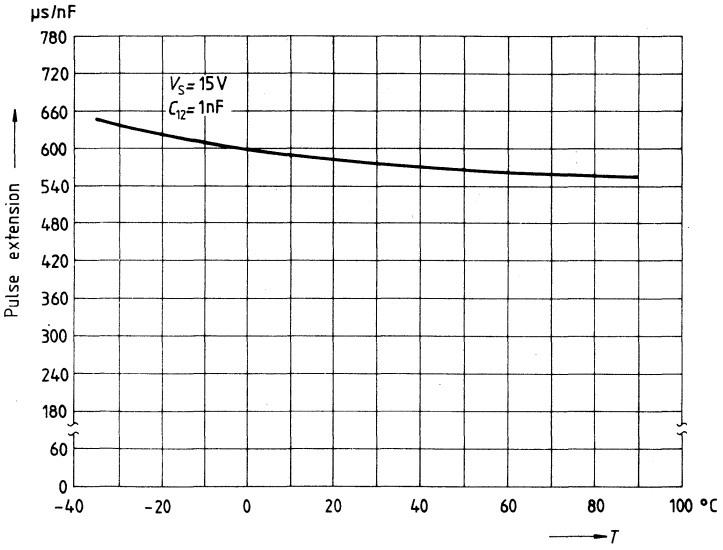
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Inhibit pin 6						
switch-over of pin 7						
Outputs disabled	$V_{6\,L}$		3.3	2.5	V	1
Outputs enabled	$V_{6\,H}$	4	3.3		V	1
Signal transition time	t_r	1		5	µs	1
Input current $V_6 = 8$ V	$I_{6\,H}$		500	800	µA	1
Input current $V_6 = 1.7$ V	$-I_{6\,L}$	80	150	200	µA	1
Deviation of I_{10} R_9 = const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	−5		5	%	1
Deviation of I_{10} R_9 = const. $V_S = 8$ V to 18 V	I_{10}	−20		20	%	1
Deviation of the ramp voltage between 2 following half-waves, V_S = const.	$\Delta V_{10\,max}$		±1		%	
Long pulse switch-over pin 13						
switch-over of S8						
Short pulse at output	$V_{13\,H}$	3.5	2.5		V	1
Long pulse at output	$V_{13\,L}$		2.5	2	V	1
Input current $V_{13} = 8$ V	$I_{13\,H}$			10	µA	1
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	45	65	100	µA	1
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CE0}			10	µA	2.6
Saturation voltage $I_Q = 2$ mA	V_{sat}	0.1	0.4	2	V	2.6
Outputs pin 14, 15						
H-output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	V_S-3	$V_S-2.5$	$V_S-1.0$	V	3.6
L-output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	0.3	0.8	2	V	2.6
Pulse width (short pulse) S9 open	t_p	20	30	40	µs	1
Pulse width (short pulse) with C_{12}	t_p	530	620	760	µs/nF	1
Internal voltage control						
Reference voltage	V_{REF}	2.8	3.1	3.4	V	1
Parallel connection of 10 ICs possible						
TC of reference voltage	α_{REF}		2×10^{-4}	5×10^{-4}	1/K	1

5

Application Hints for External Components

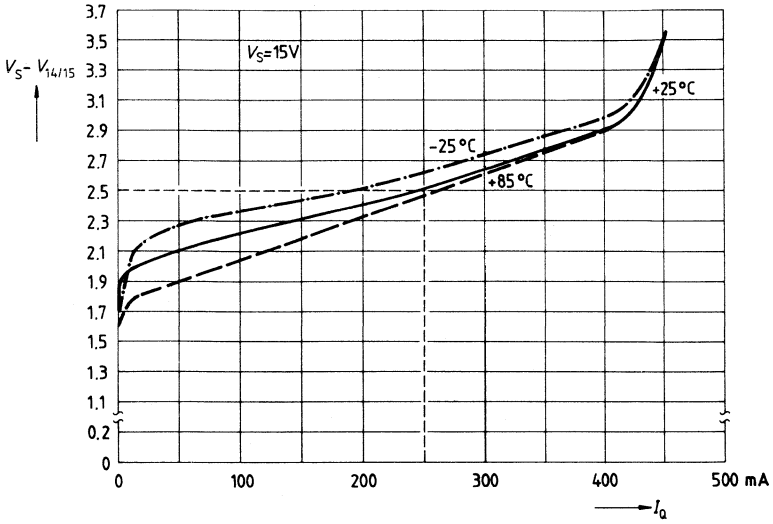
		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$		[2]	
Charge current	$I_{10} = \frac{V_{REF} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2\,V$ $V_{10} = \frac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ [2]

Pulse extension versus temperature

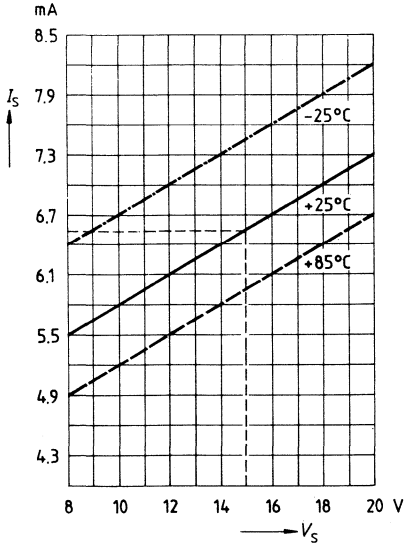


1) Attention to flyback times
2) $K = 1.10 \pm 20\%$

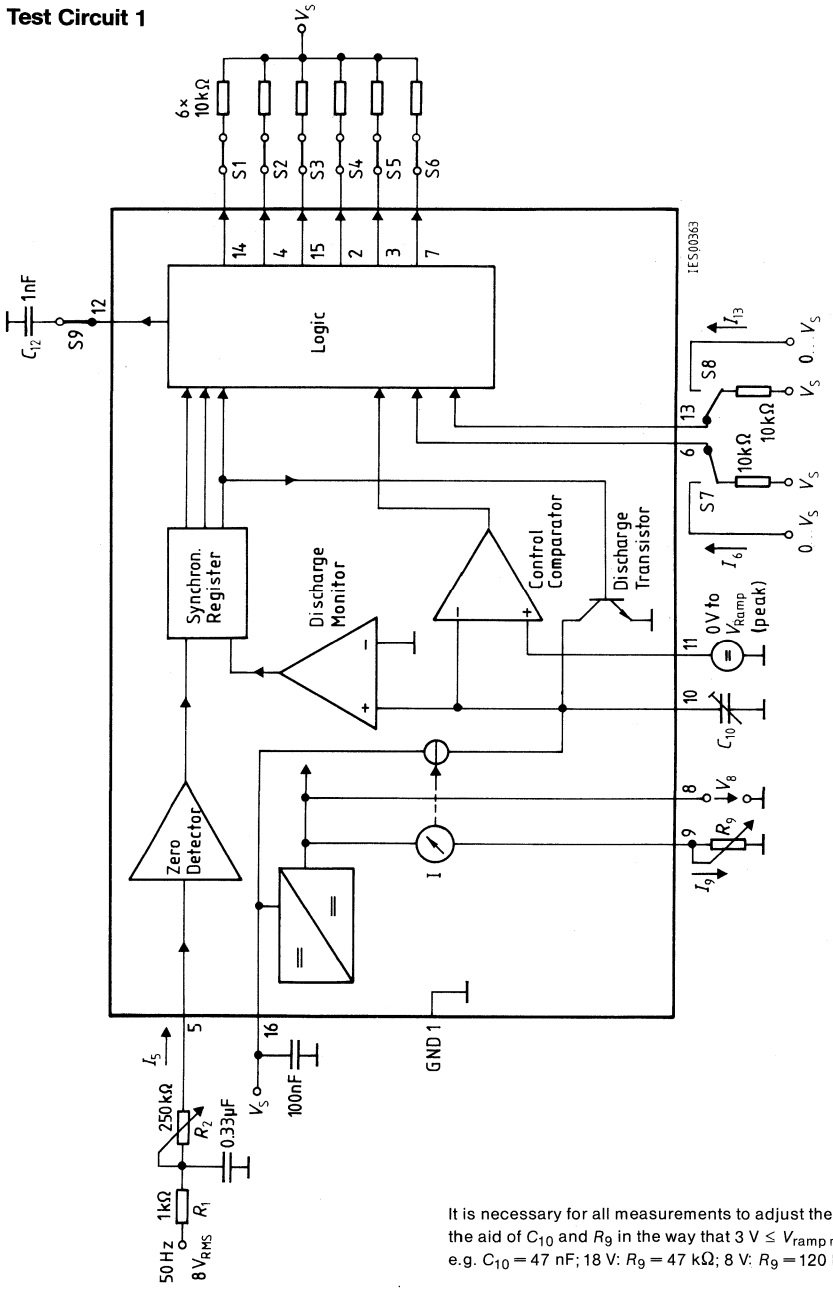
Output voltage measured to + V_S



Supply current versus supply voltage

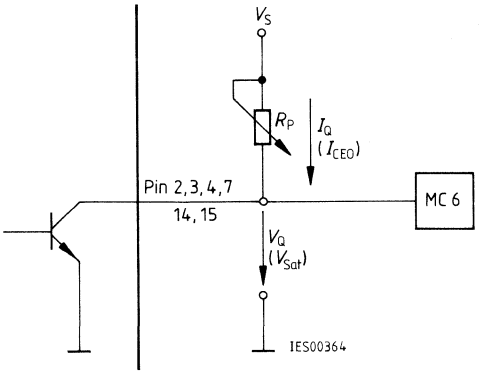


Test Circuit 1



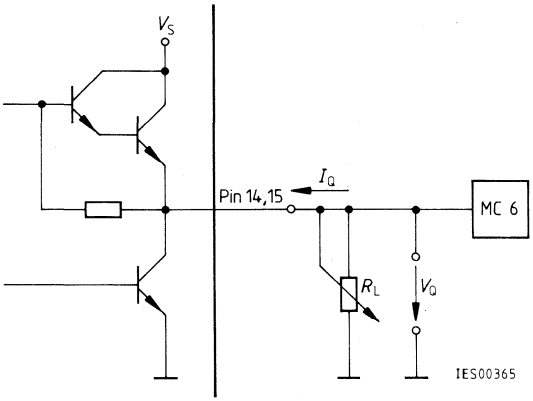
It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\ V \leq V_{ramp\ max} \leq V_S - 2\ V$
e.g. $C_{10} = 47$ nF; 18 V: $R_9 = 47$ kΩ; 8 V: $R_9 = 120$ kΩ

Test Circuit 2



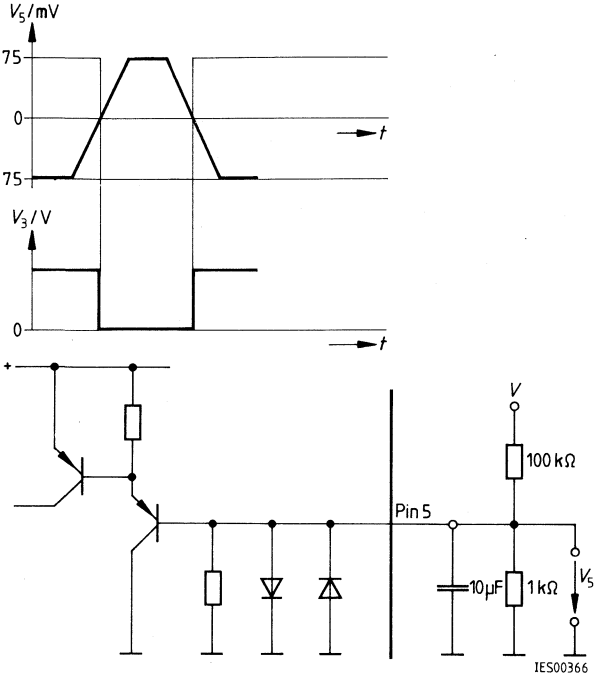
The remaining pins are connected as in test circuit 1

Test Circuit 3



The remaining pins are connected as in test circuit 1

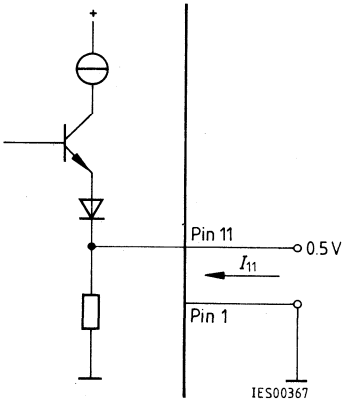
Test Circuit 4



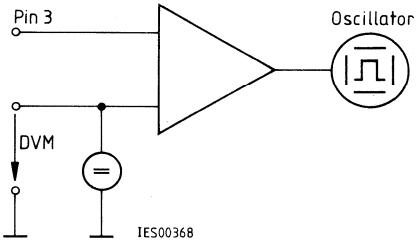
Remaining pins are connected as in test circuit 1

The 10 µF capacitor at pin 5 serves only for test purposes

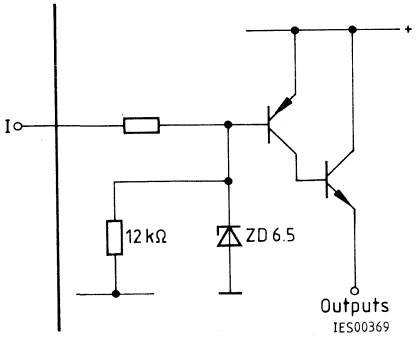
Test Circuit 5



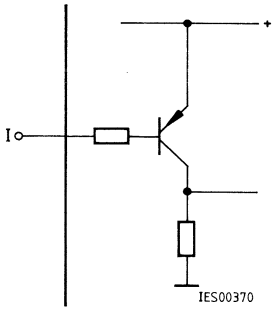
Test Circuit 6



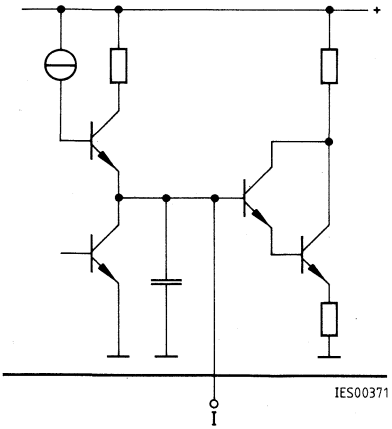
Inhibit 6



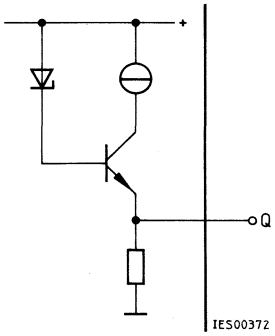
Long pulse 13



Pulse extension 12

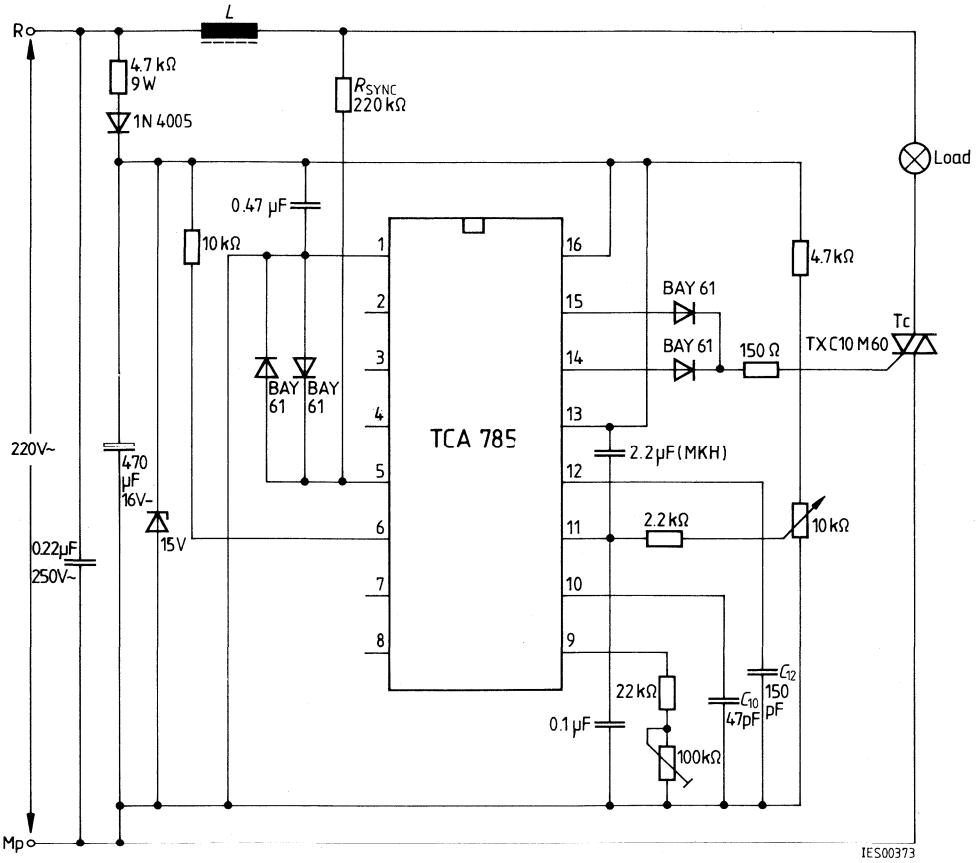


Reference voltage 8



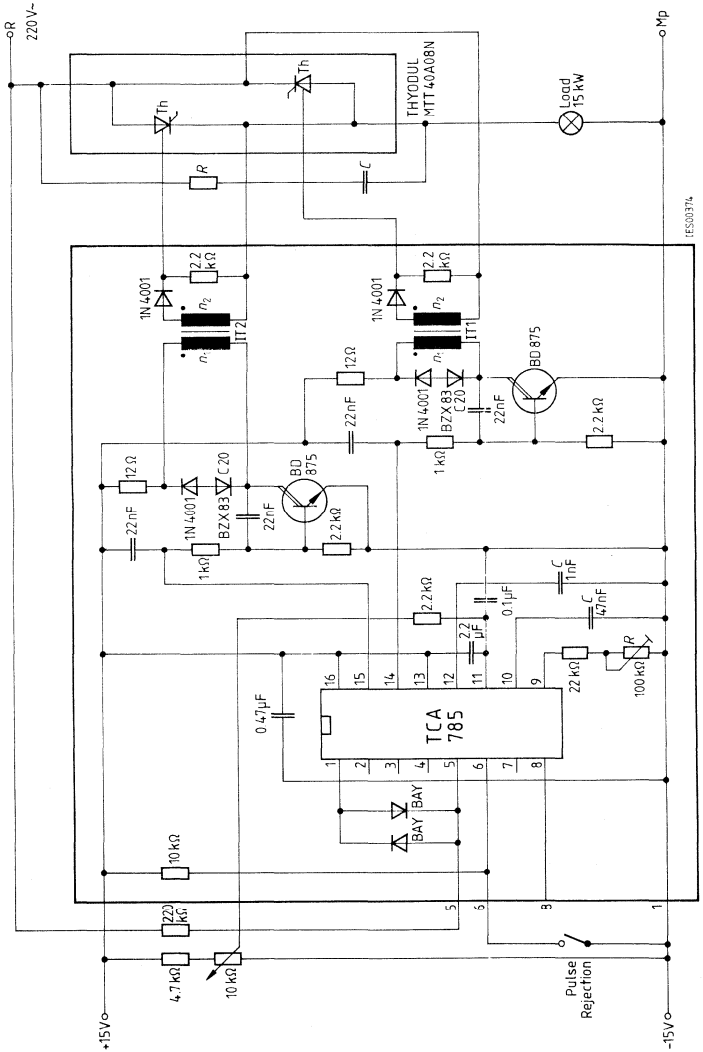
Application Examples

Triac Control for up to 50 mA Gate Trigger Current



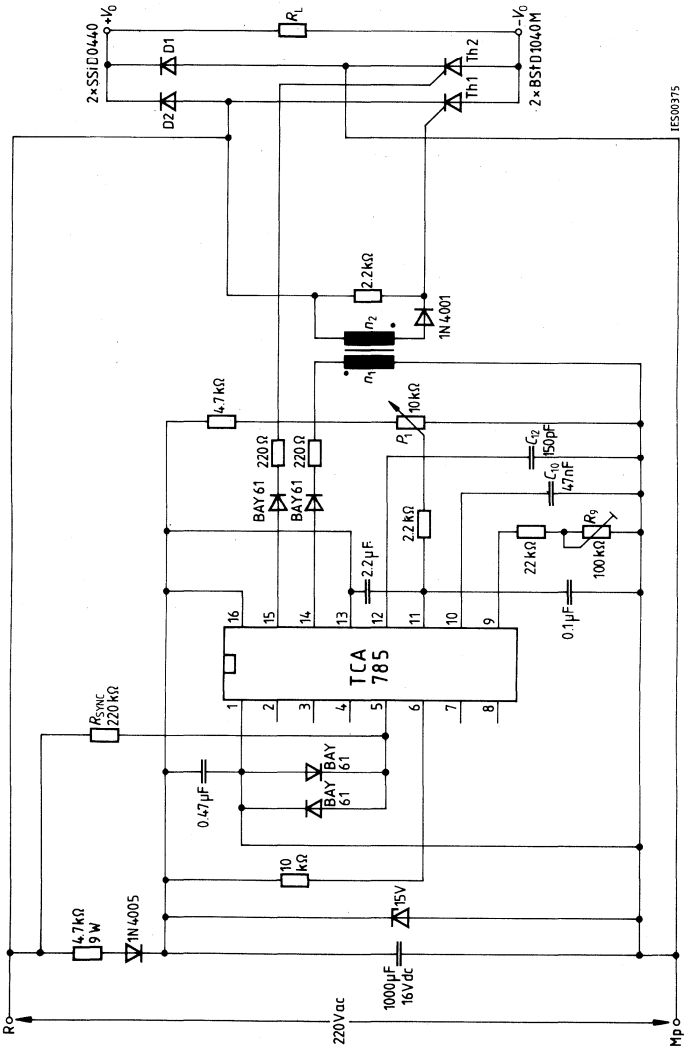
A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. Trigger pulse width is approx. 100 µs.

Fully Controlled AC Power Controller
Circuit for Two High-Power Thyristors

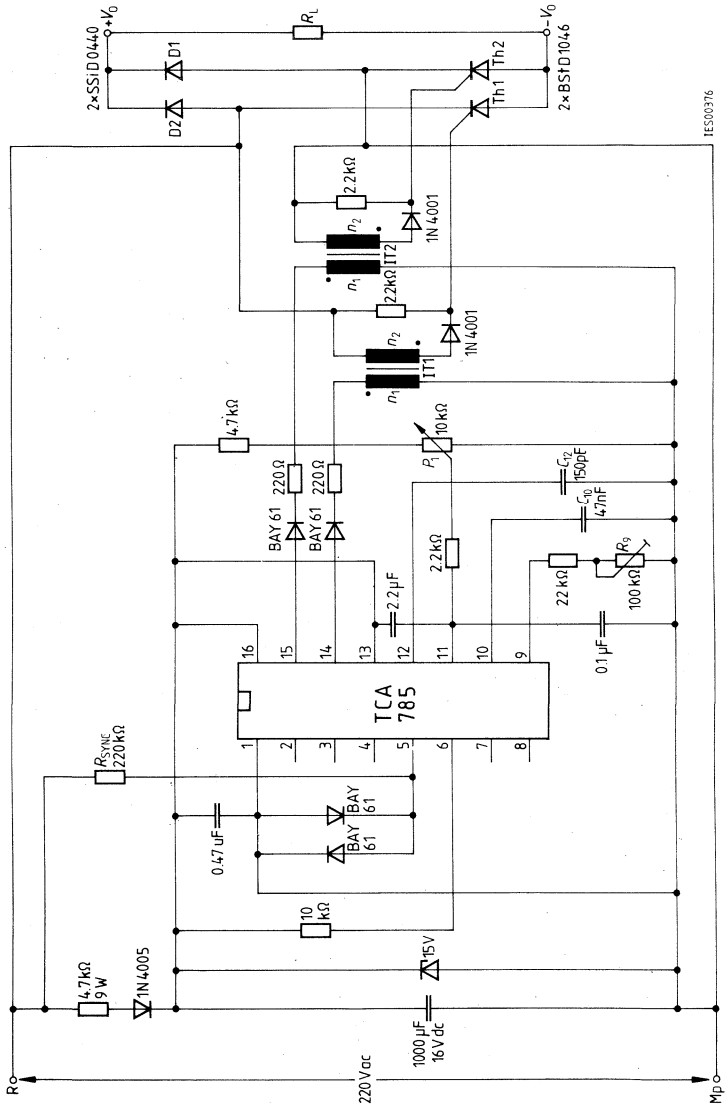


Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors



Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors

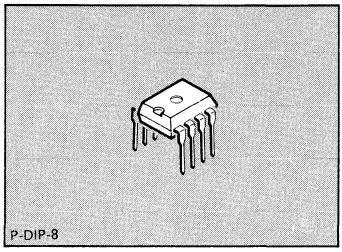


TLE 3101
TLE 3102
TLE 3103
TLE 3104

Bipolar IC

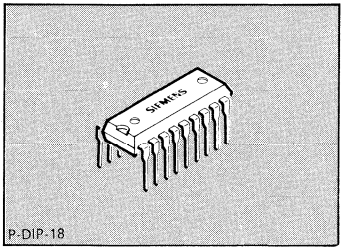
Features

- Direct supply from ac line possible
- Low power consumption, typically 2.4 mA
- Only one capacitor for trigger pulse width and phase angle
- Highly stabilized reference voltage
- Negative triac gate trigger current, 100 mA max.
- No triac drive pulses during supply undervoltage
- Optional voltage or current synchronization
- TLE 3101 with independent on-chip op amp OP and comparator K3



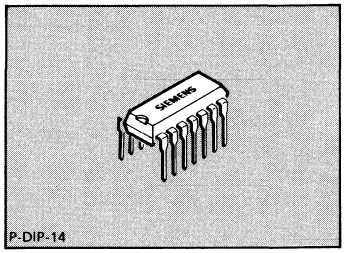
The following versions were produced from that basic IC:

- TLE 3102 without comparator K3
- TLE 3103 without op amp
- TLE 3104 without K3, enable input E/A, control input $V_{control}$, and without Z diode output



Type	Ordering Code	Package
S TLE 3101	Q67000-A2337	P-DIP-18
■ S TLE 3102	Q67000-A2338	P-DIP-14
■ S TLE 3103	Q67000-A2339	P-DIP-14
S TLE 3104	Q67000-A2312	P-DIP-8

■ = Not for new design



These simplified versions are provided for less complex low-cost applications.

These bipolar phase control ICs require, for most applications, only a minimum number of external components. Typical applications are motor control, brightness control, temperature control, cos φ optimization for squirrel-cage motors, and starting current limitation.

Thanks to their high efficiency, the TLE 310 x ICs are particularly suitable for consumer goods, such as kitchen appliances and washing machines, vacuum cleaners, electric irons and hobbyist appliances.

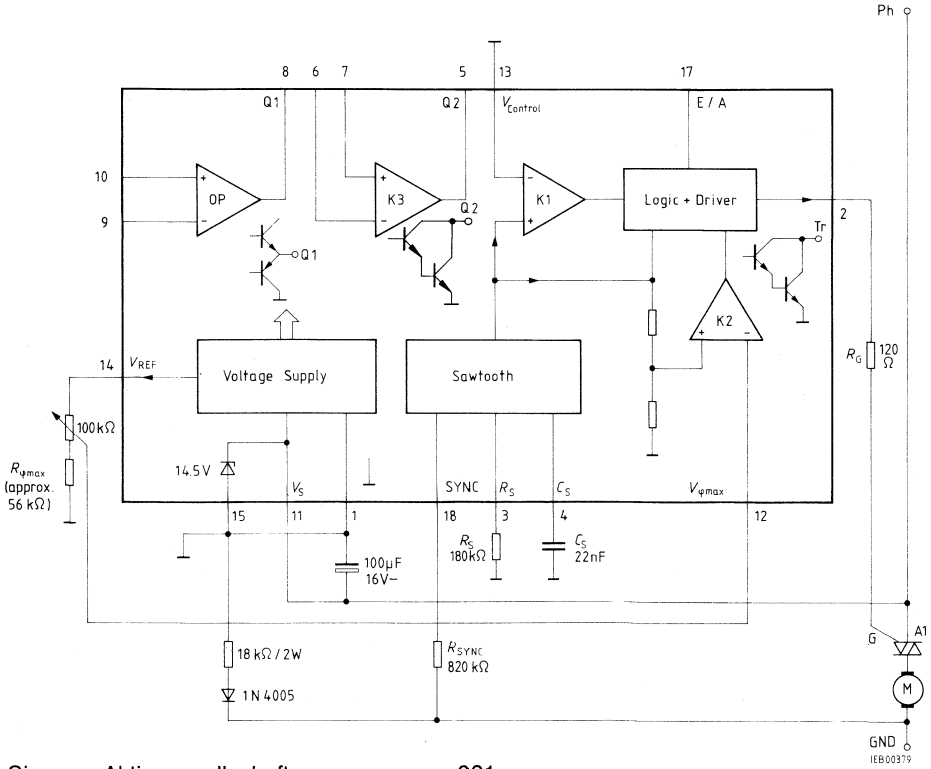
A special feature is the soft start which requires only straightforward wiring, and is e.g. used in portable drills for center punching.

Pin Definitions and Functions for TLE 3101

Pin	Function	Pin	Function
1	Ground	10	+input op amp
2	Triac trigger output	11	V_S
3	R_S	12	$V_{\varphi max}$
4	C_S	13	$V_{control}$, K1
5	Output Q2, K3	14	V_{REF}
6	−input K3	15	Z diode
7	+input K3	16	N.C.
8	Output Q1, op amp	17	Enable input E/A
9	−input op amp	18	Synchronization input (SYNC)

5

Block Diagram with External Components for Motor Control

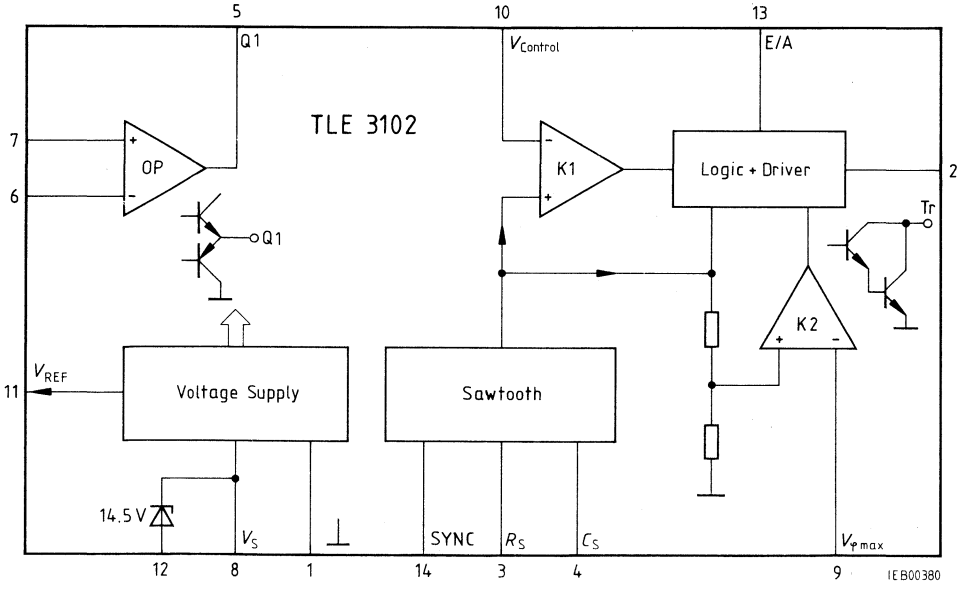


The **TLE 3102** with on-chip op amp for external use is particularly suitable as a speed controller with P, PI, or PID characteristic; the op amp serves as adjustable gain amplifier. An acutal value which is proportional to speed can be formed by rectification of the tacho amplitude.

Pin Definitions and Functions for TLE 3102

Pin	Function	Pin	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{REF}
5	Output Q1, op amp	12	Z diode
6	−input op amp	13	Enable input E/A
7	+input op amp	14	Synchronization input (SYNC)

Block Diagram



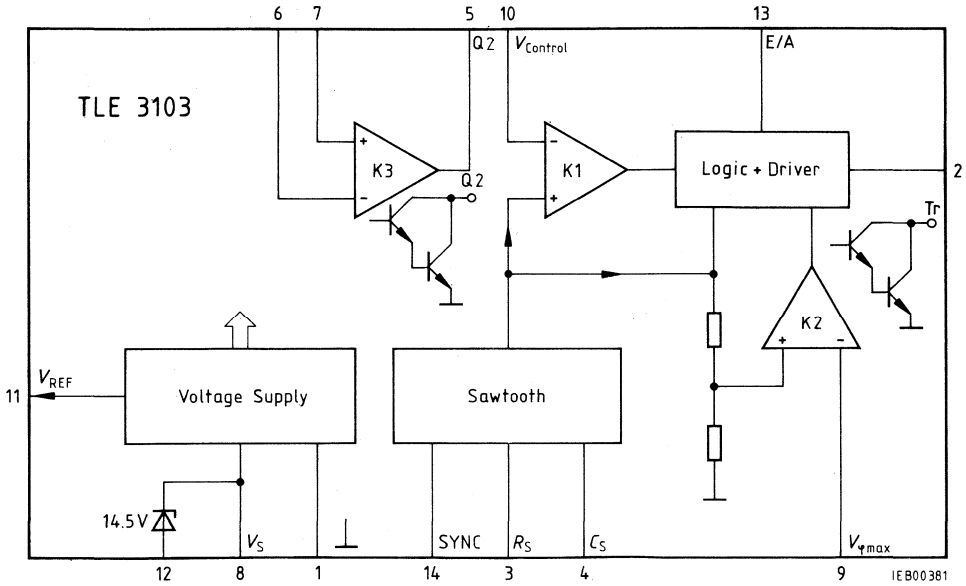
The **TLE 3103** with on-chip comparator for external use is particularly suitable for phase control systems in which special functions, such as blocking protection or overtemperature protection, are required.

Pin Definitions and Functions for TLE 3103

Pin	Function	Pin	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{REF}
5	Output Q2, K3	12	Z diode
6	−Input K3	13	Enable input E/A
7	+Input K3	14	Synchronization input (SYNC)

5

Block Diagram

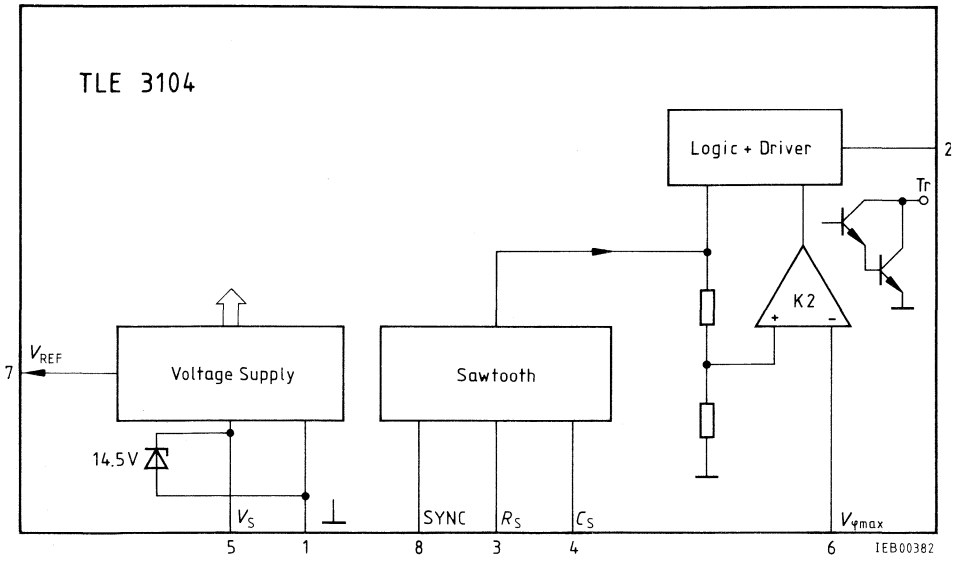


The **TLE 3104** ist particularly suitable for simple, low-cost phase control and motor control systems, in which the actual value is formed by rectification of the tacho amplitude.

Pin Definitions and Functions for TLE 3104

Pin	Function	Pin	Function
1	Ground	5	V_S
2	Triac trigger output	6	$V\varphi_{max}$
3	R_S	7	V_{REF}
4	C_S	8	Synchronization input (SYNC)

Block Diagram



Functional Description

The following is a description of the individual functional units (refer to block diagram) and their interactions:

Operational Amplifier op amp

Two inputs and the output are available. The op amp is internally compensated and has a push-pull output. Should the op amp not be required, the +input must be connected to ground (the TLE 3101 and TLE 3102 then consume minimum current).

Comparator K 3

Comparator K3 is not frequency-compensated. The output is an open NPN collector which in switching operation may drive an LED, for example. Should the comparator not be required, the −input must be connected to ground. K3 then has minimum current consumption.

Reference Voltage Source

A temperature-stabilized voltage source is available for control and regulating circuits.

Sawtooth Generator

In this unit, a sawtooth synchronized to the line is generated by the external R_S and C_S. The phase angle of the triac is determined by comparison of the sawtooth voltage and the control voltage. The trigger pulse width for the driver is provided by the falling edge of the sawtooth generator. The charge of C_S determines the trigger pulse width. A special circuit ensures the release of only one trigger pulse per line half period.

Comparators K1, K2

Sawtooth voltage and control voltage are compared by means of comparators K1 and K2. Comparator K2 receives only half the sawtooth voltage. The phase angle limit can be adjusted within the complete phase angle range by applying a reduced reference voltage to input "$V_{\varphi max}$". Comparator K2 provides starting current limitation and/or phase angle limitation for inductive loads. Both comparator outputs are fed to the logic and driver unit.

The comparator with the smaller conduction angle is the dominating one. With $V_{\varphi max}$ dominating, the trigger pulse width is doubled – compared with the trigger pulse width in case of a dominating $V_{control}$.

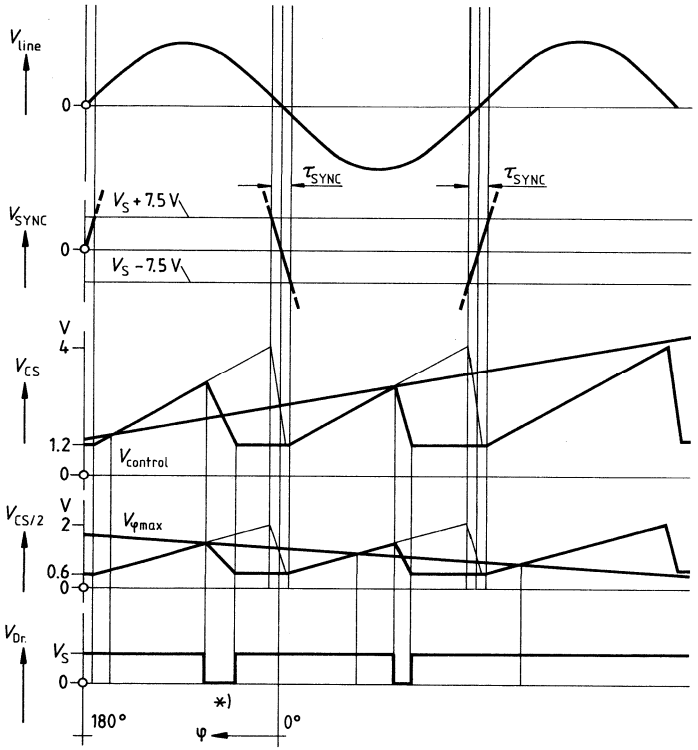
Logic + Driver

The logic and driver unit for triac triggering is controlled by comparators K1, K2, and the enable input E/A. The E/A input is TTL-compatible and may disable or enable the trigger pulse. Logic + driver obtain information on the trigger pulse width from the sawtooth. The undervoltage monitoring enables the driver output only if the IC's supply voltage has reached the permissible minimum value. The driver output to the triac supplies negative pulses.

Synchronization

At the sync input, the phase angle is synchronized to the zero crossing point of the line voltage. The sync pulse width τ_{SYNC} has to be twice as large as the trigger pulse width.

Pulse Diagram



Conduction angle (with resistive load)

*) With $V_{\varphi max}$ dominating, the trigger pulse width is doubled.

Absolute Maximum Ratings

$T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S	−0.3	33	V
Inputs op amp K3	V_I	−0.3	33	V
Output op amp	V_{Q1}	−0,3	V_S	V
	I_{Q1}	−5	3	mA
Output K3 (disabled)	V_{Q2}	−0.3	33	V
(enabled)	I_{Q2}	0	40	mA
Output V_{REF}	V_{REF}	−0.3	5	V
Z diode	I_Z	−35	35	mA
Input SYNC	I_{SYNC}	−10	10	mA
Input R_S	V_{RS}	−0.3	5	V
Input C_S	V_{CS}	−0.3	5	V
Input $V_{control}$	$V_{control}$	−0.3	V_S	V
Input $V\varphi_{max}$	$V\varphi_{max}$	−0.3	V_S	V
Enable input E/A	$V_{E/A}$	−0.3	33	V
Output driver (disabled)	$V_{Q\,dr}$	−0.3	33	V
(enabled)	$I_{Q\,dr}$	0	120	mA
Total power dissipation (time integral)	P_{tot}		700	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
system – air P-DIP- 8 – TLE 3104	$R_{th\,SA}$		100	K/W
P-DIP-14 – TLE 3102, TLE 3103	$R_{th\,SA}$		70	K/W
P-DIP-18 – TLE 3101	$R_{th\,SA}$		70	K/W

Operating Range

Supply voltage	V_S	10	30	V
Ambient temperature	T_A	−25	85	°C
Input SYNC	I_{SYNC}	−3.5	3.5	mA

Characteristics

$V_S = 10$ to 30 V, $T_V = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Current Consumption without output load at op amp, K3, driver, V_{REF}, without R_{SYNC} current	I_S		2.4	3.2	mA	$V_S = 14.5$ V
Reference voltage	V_{REF}	1.8	2.0	2.2	V	
Load current	$-I_L$	0		3	mA	
Stability $V_S = 10$ to 30 V	ΔV_{REF}			10	mV	
$I_{REF} = 0$ to 3 mA	ΔV_{REF}			20	mV	
Temperature coefficient	$\Delta V_{REF}/\Delta T$	−0.5		0.5	mV/K	
Operational Amplifier op amp						
Open-loop voltage gain	G_{V0}	60	90		dB	
Input offset voltage	V_{IO}	−10		10	mV	
Input current	$-I_I$			2	µA	
Common-mode input voltage range	V_{IC}	0		V_S-3	V	
Output current	I_{Q1}	−3		1.5	mA	
Transition frequency	f_T		2		MHz	
Transition phase	φ_T		120		deg.	
Output voltage	V_{Q1}	1.0		V_S-3	V	
Comparator K3						
Input current	$-I_I$			2	µA	
Input offset voltage	V_{IO}	−20		20	mV	
Output enabled	V_{Q2}		1.0	1.5	V	$I_{Q2} = 20$ mA
disabled	I_{Q2}			5	µA	$V_{Q2} = 30$ V
Common-mode input voltage range	V_{IC}	0		V_S-3	V	
Input K1 ($V_{control}$)						
Input current	$-I_S$			2	µA	
Control range:						
Conduction angle = 0°			4		V	
(dependent on R_S and C_S)						
Conduction angle = 175°			1.2		V	
Max. perm. conduction angle				SYNC pulse end −5	deg.	
Input K2 ($V\varphi_{max}$)						
Input current	$-I_S$			2	µA	
Control range:						
Conduction angle = 0°			2		V	
(dependent on R_S and C_S)						
Conduction angle = 175°			0.6		V	
Max. perm. conduction angle				SYNC pulse end −5	deg.	

Characteristics

$V_S = 10$ V to 30 V, $T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Z Diode						
Z voltage	V_Z	13	14.5	16	V	$I_Z = 5$ mA
Enable Input E/A						
Input current	$-I_I$			2	µA	
H input voltage for driver output, active	V_{IH}	2.8			V	
L driver output disabled	V_{IL}			0.8	V	
Triac Trigger Output						
Output, enabled	V_L	1.4	2	2.5	V	$I_Q =$ 10 mA
		1.4	2	2.5	V	20 mA
		1.4	2	3.0	V	50 mA
		1.4	4	6.0	V	100 mA
Output, disabled	I_Q			10	µA	$V_Q = 30$ V
Input SYNC						
Switching current	I_{SYNC}		±20		µA	
Switching threshold	V_{SYNC}		$V_S \pm 7.5$		V	
Output disconnection at V_S undervoltage	V_S	7.5	8	10	V	
Input R_S, C_S (refer to calculation formulae)						
Limit value C_S	C_S	5		100	nF	
Limit value R_S	R_S	33			kΩ	

5

Dimensioning notes and calculation formulae

1. Select trigger pulse width according to triac type and load.

2. **Calculate** C_S (for a $V_{control}$ domination)
   C_S (nF) = trigger pulse width (µs) x 0.2
   The formula yields the typical value
   e.g. T = 50 µs results in C_S = 10 nF

3. **Calculate** R_S (for 4 V max. sawtooth voltage)

$$R_S\ (k\Omega) = \frac{1}{\text{trigger pulse width } (\mu s)} \times 2 \times 10^4$$

   The formula yields the typical value
   e.g. T = 50 µs results in R_S = 400 kΩ

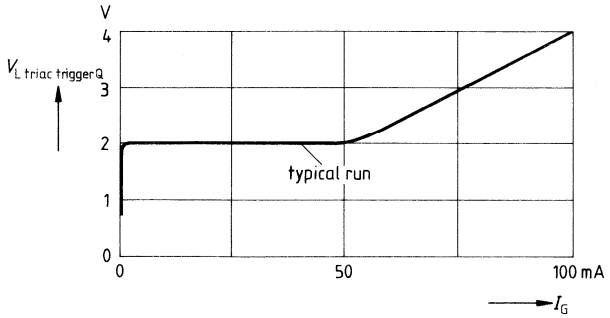
4. **Select R_{SYNC} resistance at SYNC input**
   The sync pulse width (from V_S ± 7.5 V, I_{SYNC} = ± 20 µA) has to be twice as large as the trigger pulse width.

4.1 Sync pulse width ≥ 2 x trigger pulse width x safety factor (according to component deviation and line voltage variation).

4.2 R_{SYNC} (kΩ) = [sync pulse width (µs) x line voltage (V rms) x 2.23×10^{-4} – 7.5] x 50
e.g. 560 µs sync pulse width and 220 V rms result in R_{SYNC} = 1 MΩ.
With 220 V rms line voltage, the minimum permissible resistance R_{SYNC} is 100 kΩ corresponding to a pulse width of 195 µs.

5. **Calculate** R_G

$$R_G = \frac{V_S - \text{triac gate voltage} - \text{low-voltage triac trigger output}}{I_G}$$



6. **Calculate** R_S

6.1 Calculation of R_S requires first of all the determination of the total current consumption. Insert the arithmetic mean values of the currents for one line cycle.

6.2 $\bar{I}_{tot} = \bar{I}_S = 3.2\ mA + \bar{I}(V_{ref}) + \bar{I}_{Q1}$ (OP) $+ \bar{I}_{Q2}$ (K3) $+ \bar{I}$(driver output) $+ \bar{I}$ (additional external circuit currents) $+ |\bar{I}|$ (R_{SYNC}).

6.3 $R_S\ (k\Omega) = \dfrac{\text{rms line voltage (V)}}{\bar{I}_{tot}\ (mA)} \times 0.455 \times \text{safety factor}$

(corresponding to component deviation and line voltage variation)

e.g. $\bar{I}_{tot} = 5$ mA und $V_{line} = 220$ V result in $R_S = 20\ k\Omega$.

Employing the internal Z diode reduces the IC's V_S voltage to 14.5 V.

7. **Calculate** C_G

7.1 Selection of the maximum permissible ripple at the V_S input, based on the desired functional quality and the special external components.

7.2 The ripple amplitude at the V_S input of the unit should not exceed $V_{pp} = 2$ V.

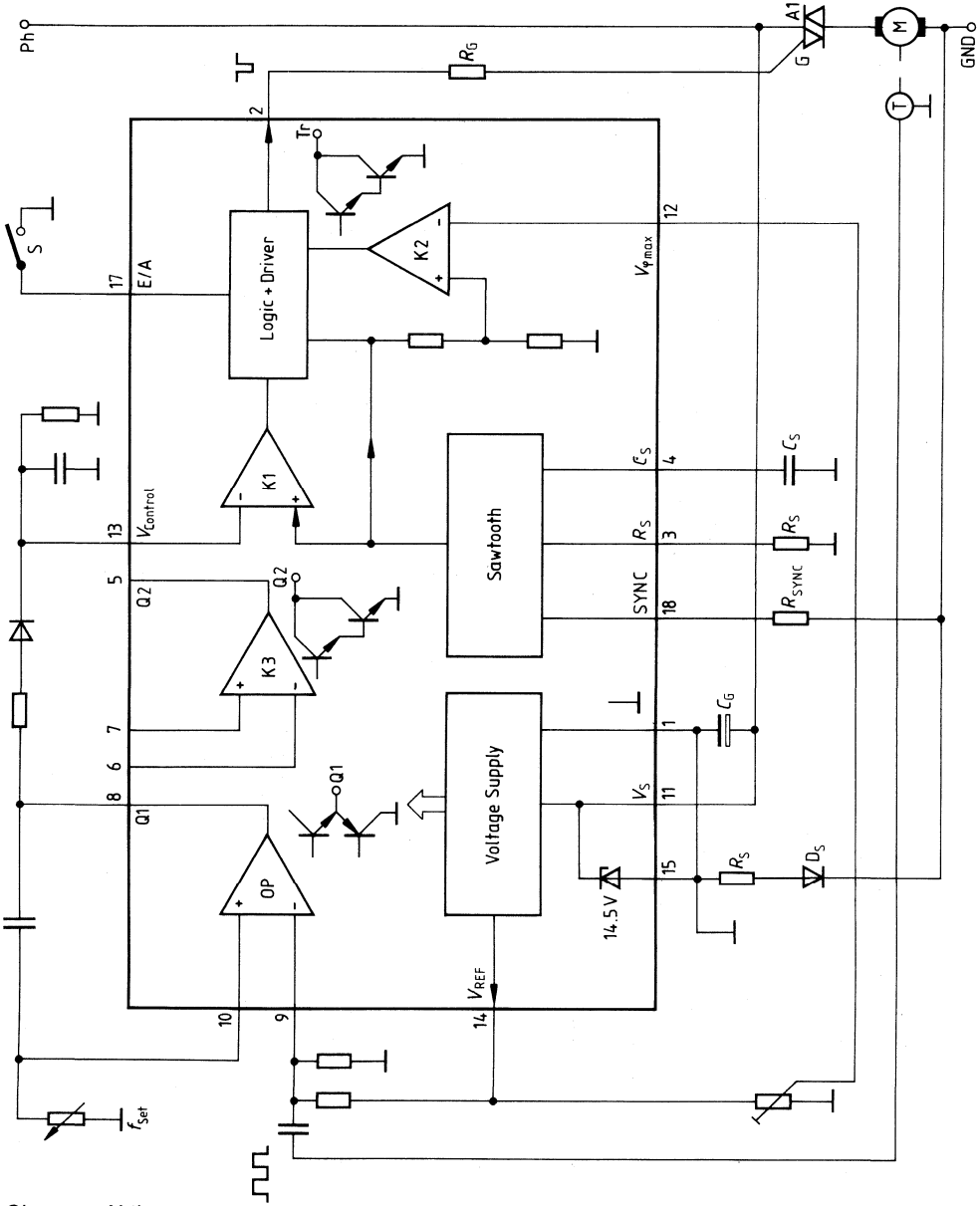
7.3 $C_G\ (\mu F) \geq \dfrac{\bar{I}_{tot}\ (mA)}{V_{pp}} \times 15$

e.g. ripple $V_{pp} = 0.75$ V; $\bar{I}_{tot} = 5$ mA results in $C_G = 100\ \mu F$

Application Examples

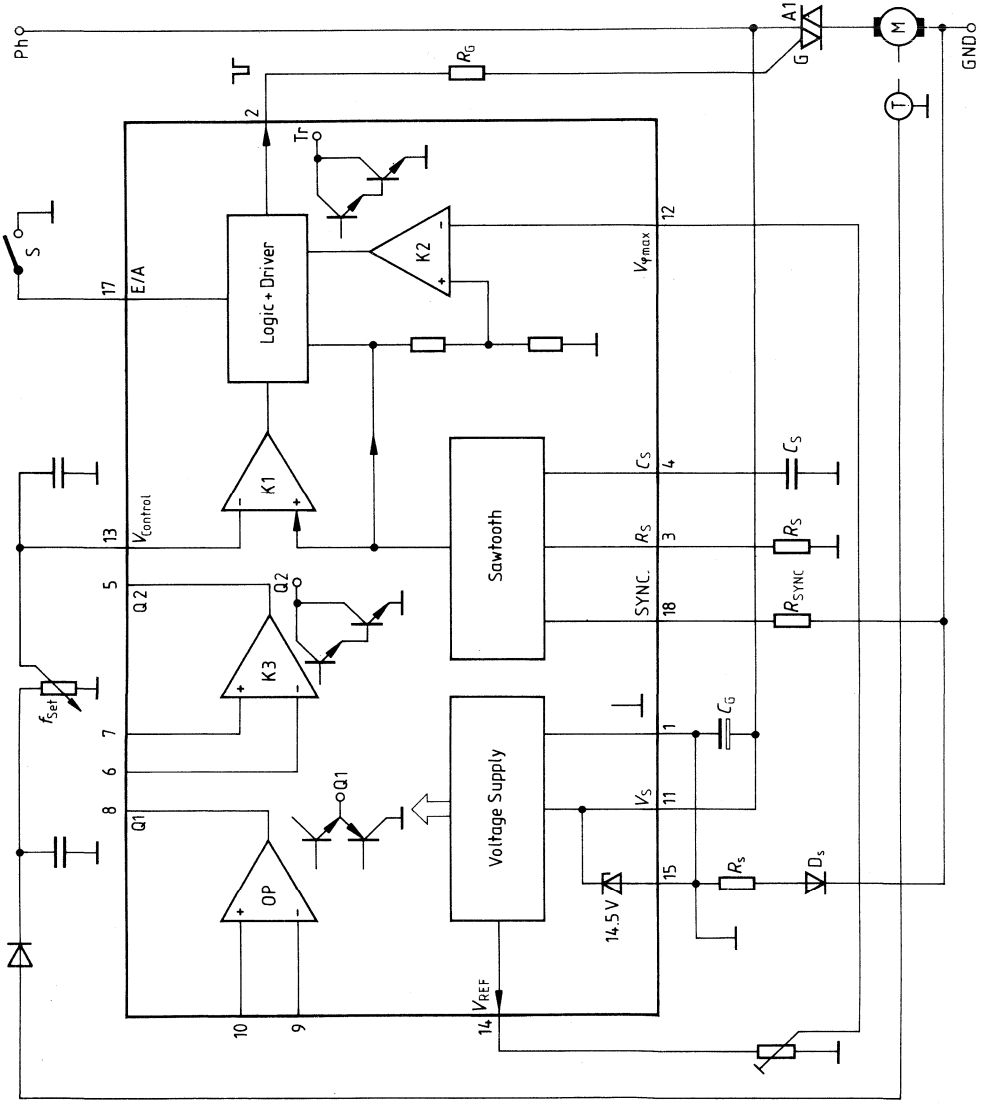
Schematic Circuit Diagram for Motor Control Using TLE 3101

The tachogenerator provides a **frequency** processed by the op amp (monoflop).

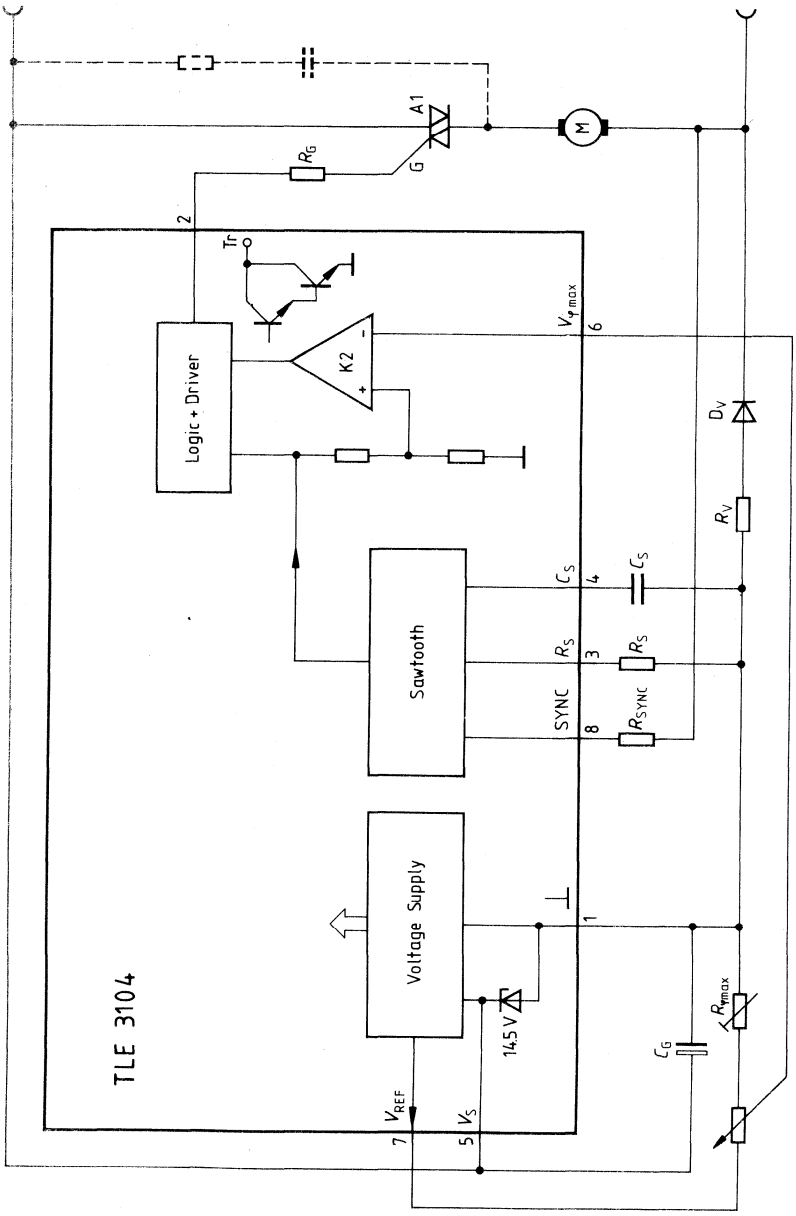


Schematic Circuit Diagram for Motor Control Using TLE 3101

The tachogenerator provides a **voltage** which is rectified and stabilized, and then fed to input $V_{control}$.

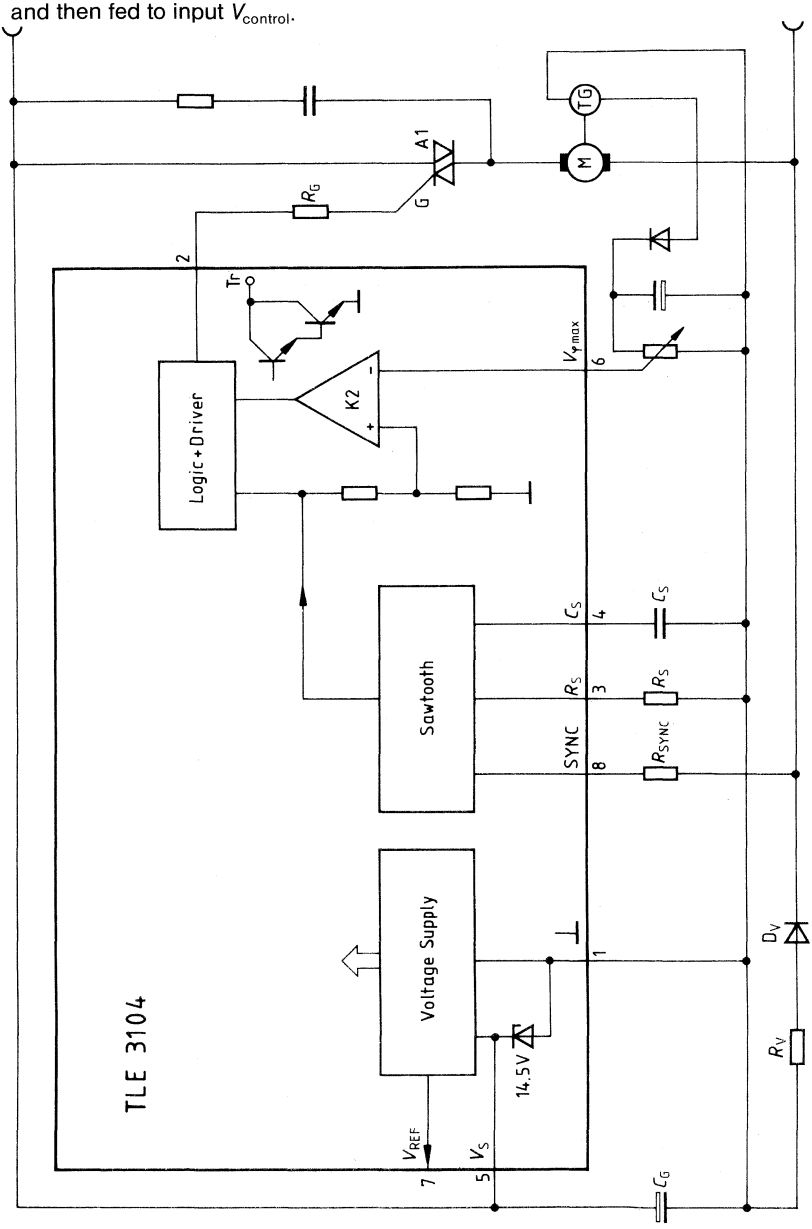


Schematic Circuit Diagram for Motor Control Using TLE 3104



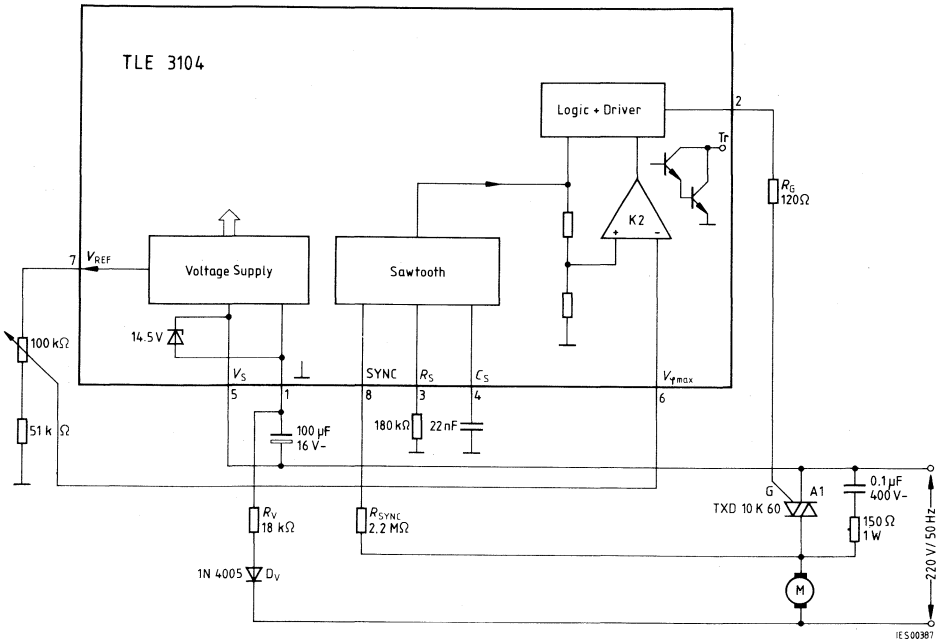
Schematic Circuit Diagram for Motor Control Using TLE 3104

The tachogenerator supplies a **voltage,** which is rectified and stabilized and then fed to input $V_{control}$.



Current Synchronization in Case of Inductive Load Control Using TLE 3104

Particularly in case of phase control of inductive loads, such as transformers and shaded-pole motors, there is a risk of half-wave operation as a result of the phase shift between voltage and current. In order to avoid this condition, the synchronization resistor is connected to A 2 of the triac (this method cannot be applied in the event of severe brush sparking of the motor).



Notes

The pulse width selected for the trigger pulse must be so great that the triac reaches its holding current, even with a great phase angle (critical: positive half-wave). For this reason, it may be necessary to select a lower value for the ac line series resistor.

The sync pulse must be at least twice as wide as the trigger pulse.

SIEMENS

Dimmer IC

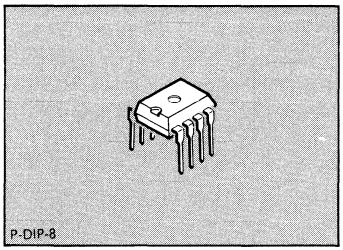
SLB 0586 A

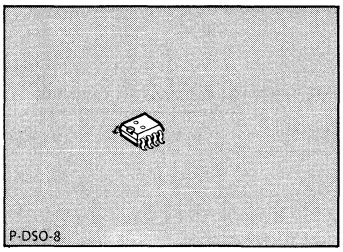
Preliminary Data

CMOS IC

Features

- Sensor operation – no mechanically moved switching elements
- Operation is also possible from several extensions by means of sensors or push buttons
- Can replace electromechanical wall switches in conventional light installations
- Brightness control with a physiologically approximated linear characteristic
- Very high interference immunity, also against ripple control signals
- Very few peripheral components
- Programming input permits selection of three different functions (MODE A/B/C)
- "Soft" turn-on with MODE A and C





Type	Ordering Code	Package
S ▼ SLB 0586 A	Q67000-H8721	P-DIP-8
S ▼ SLB 0586 G	Q67100-H8720	P-DSO-8 (SMD)

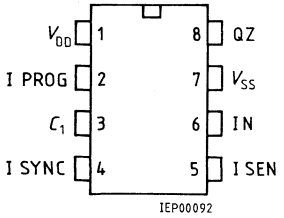
▼ New type

The SLB 0586 A and SLB 0586 G are integrated circuits in CMOS technology that permit the design of digital electronic dimmers. A single sensor or an equivalent extension input are used to turn the dimmer on and off and to set the required brightness. The types SLB 0586 A and SLB 0586 G are similar except of the package.

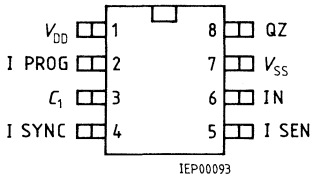
(The SLB 0586 A replaces the SLB 0586 and the S 576 A/B/C family).

Pin Configuration
(top view)

P-DIP-8



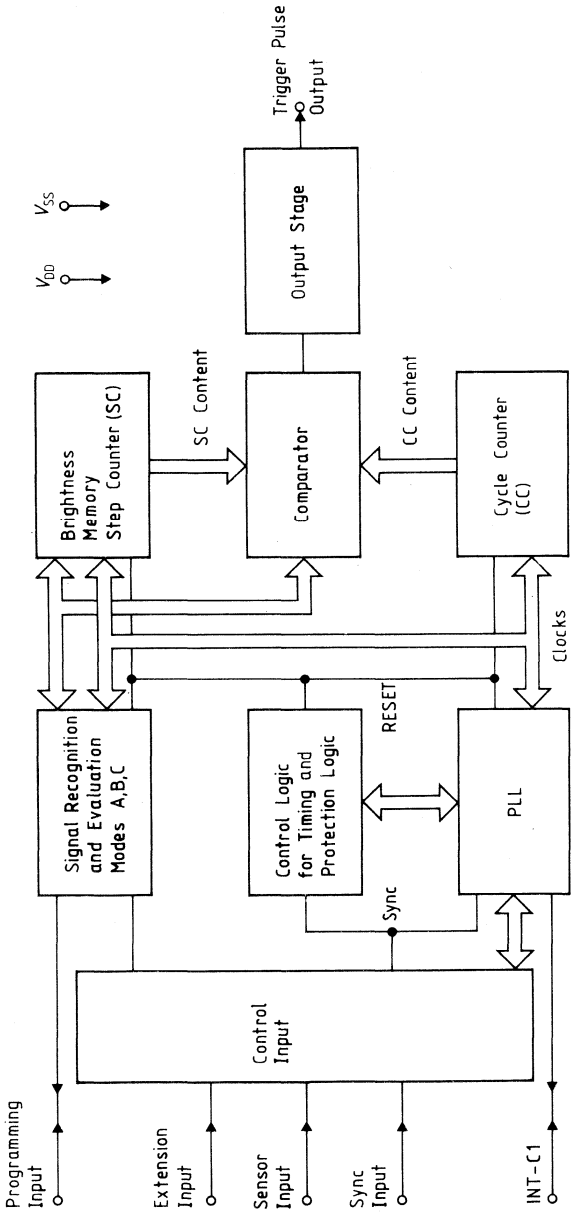
P-DSO-8



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{DD}	Ground
2	I PROG	Programming input
3	C_1	C_1 integrator
4	I SYNC	Sync input
5	I SEN	Sensor input
6	IN	Extension input
7	V_{SS}	Supply voltage
8	QZ	Trigger pulse output

Block Diagram



Functional Description

The SLB 0586A permits the design of fully electronic dimmers for light bulbs (resistive loads) which are operated via a single sensor.

The integrated circuit replaces mechanical wall switches in conventional light circuit installations. All functions can be selected from several switching points (extensions).

The brightness is set by phase control. Its digital logic is synchronized with the line frequency **(see block diagram)**.

It is possible to supply the IC via a two-wire connection, as the angle of current flow is limited to a maximum of 152 °C of the half wave.

Operation

The integrated circuit can distinguish the instruction "ON/OFF" and "Dimming" by the duration for which control input is operated i.e. the sensor is touched **(refer to figure 1)**.

Turning ON/OFF

Short touching (50 to 400 ms) of the sensor area turns the lamp on or off, depending on its preceding state. The switching process is activated as soon as the sensor is released.

Setting of the Brightness (Dimming)

If the sensor is touched for a longer period (> 400 ms), the angle of current flow will be varied continuously. It runs across its control loop in approximately 7.6 s (e.g. bright-dark-bright) and continues this sequence until the sensor is released.

Easy operation, even in the lower brightness range, is enabled by the following procedure: the phase control angle is controlled such that the lamp brightness varies physiologically-linear with the operating time and pauses for a short period when the minimum brightness is reached.

Using R_2 and C_4 in the application circuit the angle of current flow can be controlled between 40° and 148°.

Control Behavior

The three operating MODES A, B, C, differ in their control behavior. The required MODE is set with the programming input.

MODE A With turn-on, the maximum brightness level is set; with dimming, control starts from the minimum brightness level. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

MODE B With turn-off, the selected brightness is stored and set again when the switch is turned on. Dimming starts at this stored value and the control direction is reversed with repeated dimming.

MODE C With turn-on, the maximum brightness is set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Programming of the MODES

MODE A: $V_{I2} = V_{SS}$ (L)

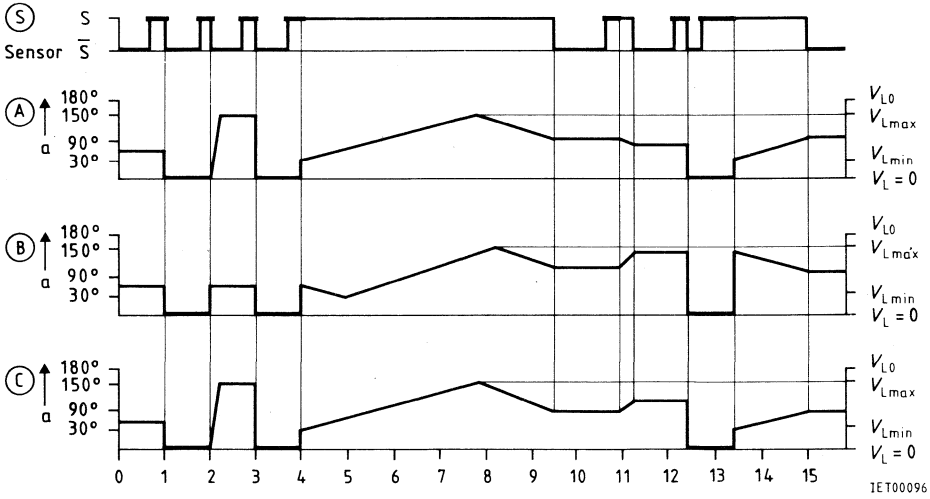
MODE B: V_{I2} = open (tristate)

MODE C: $V_{I2} = V_{DD}$ (H)

V_{I2} = Level at pin 2

Figure 1

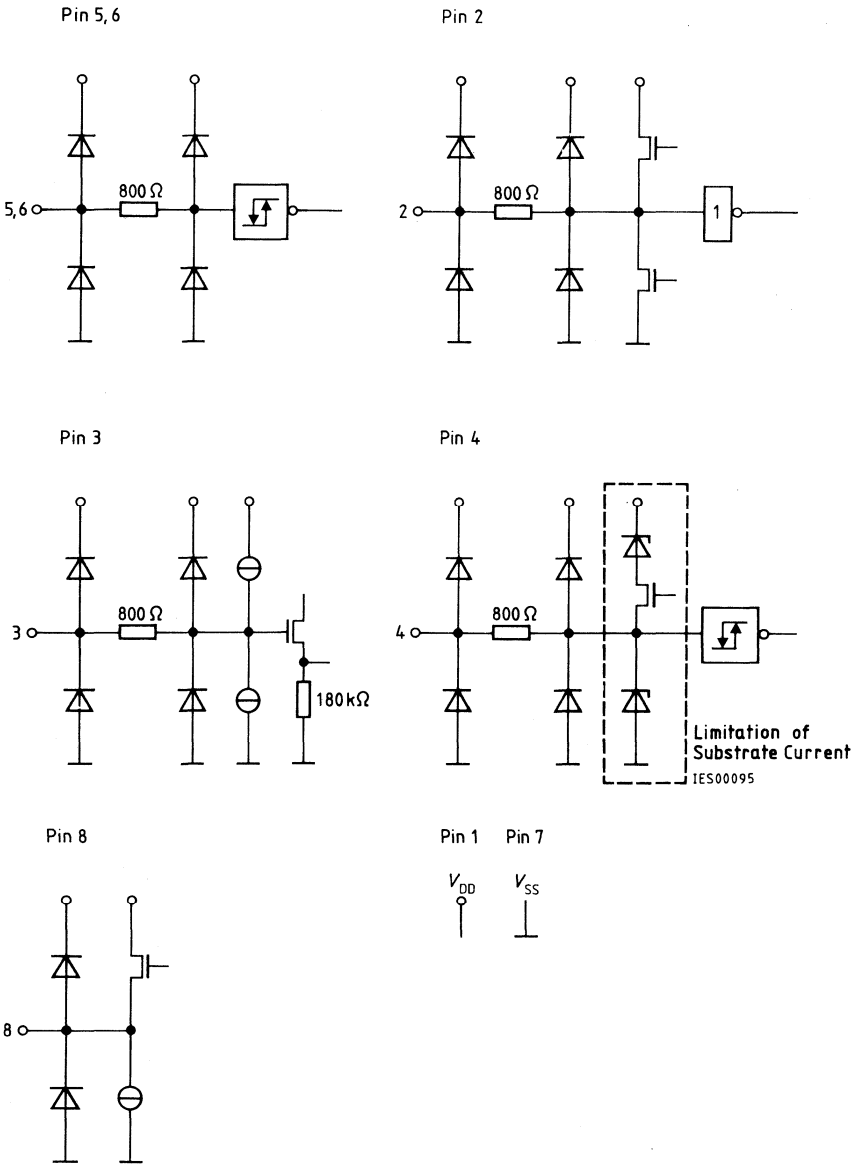
Control Behavior of Operating MODES
(schematic)



α Angle of current flow
V_L Lamp voltage
S Control signal: S Sensor touched (=< 0.4 s, -> 0.4 s)
S̄ Sensor not touched

MODES A and C permit "soft" turn-on; i.e. brightness is increased from 0 to maximum within 380 ms.

Figure 2
Schematic Circuit Diagram



Absolute Maximum Ratings

$V_{DD} = 0$ V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SS}	−7.5	0.3	V
Input voltage	V_I	V_{SS} −0.3	0.3	V
Input current	I_I	−0.5	0.5	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Total power dissipation ($T_A = 25$ °C)			10	mW

Thermal Resistance

System-air P-DIP-8	$R_{th\ SA}$		135	K/W
System-air P-DSO-8	$R_{th\ SA}$		231	K/W

Operating Range

Supply voltage	V_{SS}	−4.5	−5.6	V
Line frequency	f	47.5	63	Hz
Ambient temperature	T_A	0	80	°C

Characteristics

$T_A = 25$ °C; $V_{SS} = -5$ V ($V_{DD} = 0$ V)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current with missing sync signal	I_{DD}			0.45	mA	$f_{sync} = 0$
Input capacitance	C_I		5		pF	$V_I = 0$ V $f = 1$ MHz

Sensor Input (pin 5)

H-input voltage	V_{IH}	1/2 V_{SS} +1.1			V	
L-input voltage	V_{IL}			1/2 V_{SS} −1.1	V	
Input current	I_{IH}		33	37	µA	220 V at sensor input and series resistor
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		line sine wave			
Frequency with active signal	f		50/60		Hz	synchronized with 50/60 Hz clock at sync input

Characteristics

$T_A = 25\,°C$; $V_{SS} = -5\,V$ ($V_{DD} = 0\,V$)

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Extensions (pin 6)						
H-input voltage	V_{IH}	$1/2\,V_{SS}+1.1$			V	
L-input voltage	V_{IL}			$1/2\,V_{SS}-1.1$	V	
Input current	I_{IH} I_{IL}	-1 0		0 1	µA µA	$V_I = 0\,V$ $V_I = V_{SS}$
Sync Input (pin 4)						
H-input voltage L-input voltage Input current	V_{IH} V_{IL} I_{IH}	$1/2\,V_{SS}+1.8$	 207	 $1/2\,V_{SS}-1.8$	V V µA	with series resistor 1.5 MΩ from 220 V line*)
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		supply sine wave			
Frequency	f		50/60		Hz	
Programming Input (pin 2)						
Load capacitance through board with tristate	C_L			7	pF	
Programming of Operating MODES						
Integrator (pin 3)						
Application circuit	C_5 R_{10}	68 22	100 100	330 680	nF kΩ	
Output (pin 8)						
L-output current	I_Q	25			mA	$V_{QL} = -3\,V$
L-pulse width	t_{QL}			39.0 32.6	µs µs	50 Hz supply 60 Hz supply
HL transition time	t_{HLQ}			5	µs	
LH transition time	t_{LHQ}			5	µs	

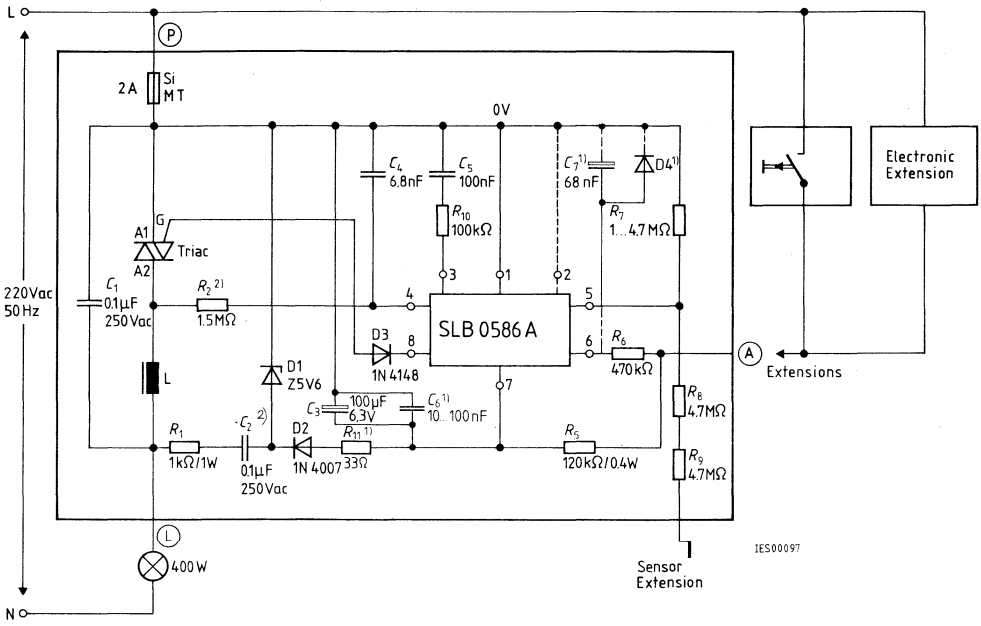
*) see application circuit

Application Circuit

The suggested circuit design of the SLB 0586 A performs the following functions:

- Current supply for the circuit (R_1, C_2, D1, D2, C_3).
- Filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4). For specific applications C_4 can be increased up to 33 nF, however, only at the expense of the lamp brightness so that the lamp gets darker (control range shifts to the left).
- Integration unit for internal PLL circuit (C_5, R_{10})
- Protection of the user (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in the case of reverse polarity of the extension (R_5, R_6).
  Both resistors can be omitted, if no extension is connected. In this case pin 6 must be interconnected with V_{SS} (pin 7).
- D3: Reduction of positive voltages which may arise during the triggered state at the gate of some triacs to values below V_{DD} +0.3 V **(refer to maximum ratings)**. If suitable triacs are used, diode D3 can be omitted. (This feature of the triac depends on the anode current and on the internal resistance between G and A1, and can be measured and specified by the manufacturer).
- Dr: The choke and the capacitor C_1 are used for EMI suppression.
  Depending on the application, the EMI suppression is to be dimensioned in acc. with
  VDE 0875/part 1 (general)
  VDE 0550/part 6 (chokes)
  or corresponding to national regulations
  e.g. 1.4...2 mH, Q = 11...24

Application Circuit



1) The components C_6 10...100 nF ceramic
C_7 33...68 nF
D_4 Ge or Schottky diode
R_{11} 33...68 Ω
serve to improve interference immunity under special conditions like for example:
- high-frequency mains interferences
- long extension lines exlubiting high earth capacitances
- supply line resistances in the load circuit
and can therefore be dropped for normal operating conditions.

2) At 110 V/60 Hz line:
C_2: 150 nF/160 Vac
R_2: 680 kΩ

Application Notes

1. **Synchronization**

   Interference of the synchronization can be suppressed by setting the C_4 filter capacitor at the sync input between 3.3 and 33 nF. By increasing the C_4 value the range of the controllable conduction angle goes to less minimum brightness. At the same time, the immunity against superimposed interference from the line improves, so that, for example, with C_4 = 33 nF an interference amplitude of 30 V does not cause any synchronization errors in the range of 150 to 1500 Hz.

C_4 (nF)	Conduction angle (°)	Interference amplitude (V)
3.3	151 to 43	20
6.8	148 to 40	↓
10.0	147 to 39	
15.0	144 to 36	
33.0	136 to 28	30

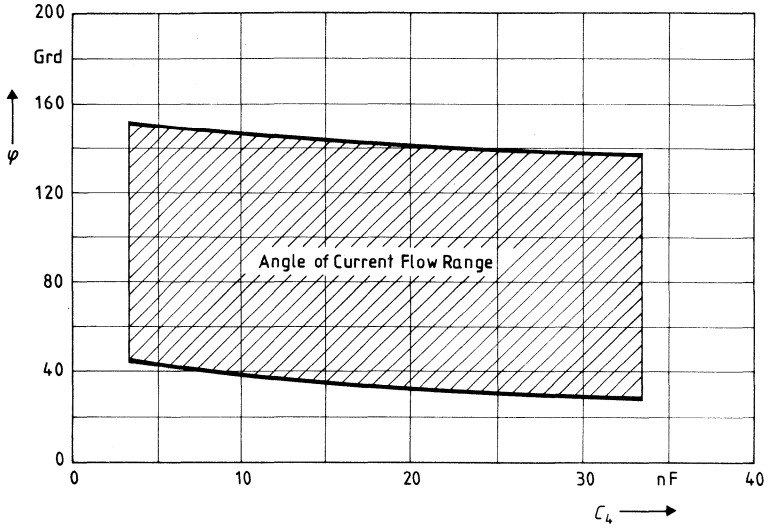
2. **PLL Circuit**

   The PLL circuit at pin 3 can be varied to reach a minimum of flickering and a maximum of noise immunity. The PLL circuit is adjusted to a capacitor value of 100 nF.

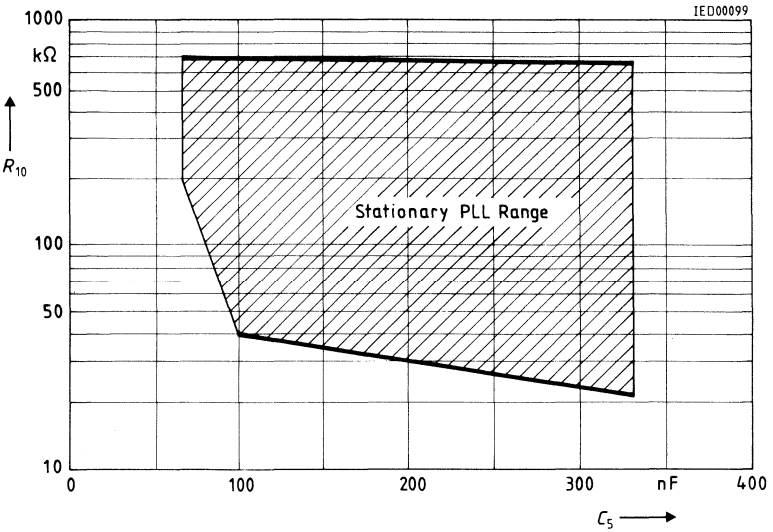
   R_{10} can be varied in the range of 22 kΩ to 680 kΩ **(figure 6)**. Here higher resistances speed up the response of the PLL circuit.

   Hence it is possible to reduce the jitter of the trigger pulse to below 0.5 ms by a low-resistance R_{10} at low interference frequencies (≤ 400 Hz) and a high-resistance R_{10} at high interference frequencies. This will greatly reduce brightness modulations through interferences.

3. Dependence of C_4 and Angle of Current Flow (Figure 3)



4. Range of Value of the RC-Component at Pin 3 for Stationary PLL-Operation (Figure 4)



Extensions

All switching and control functions can also be performed from extensions which are connected to the extension input. The main sensor input and the extension inputs have equal priority. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation "H" potential must be applied to the extension input for both half cycles.

An electronic circuit suitable for this purpose is shown in the application example **(figure 7)**. The circuit operates as return delay and takes over the triggering of the switching transistors during the negative half cycle.

- Response time approx. 2 ms
- Return delay time approx. 30 ms
- Protection against incorrect polarization (R_1, D1, Si)

Note

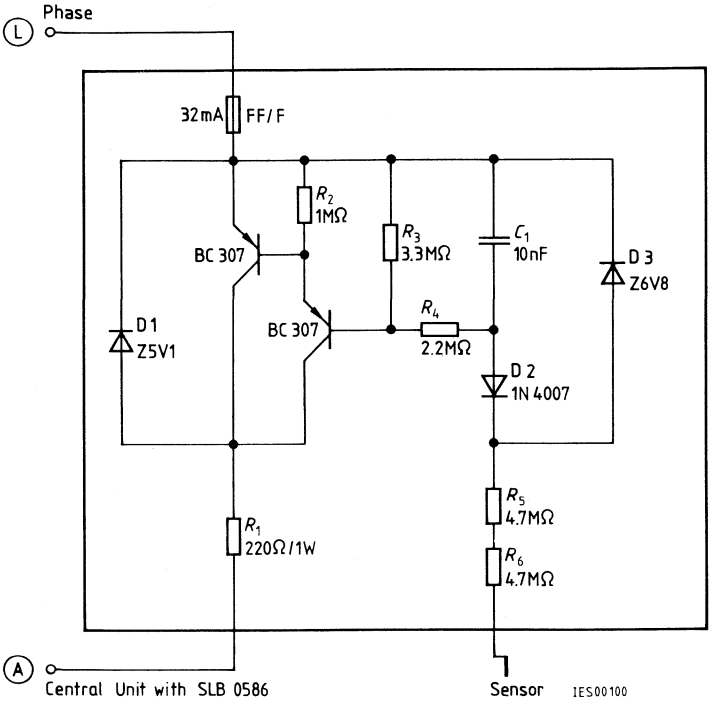
The extension input must be connected to V_{SS}, if this input is not required.

Operation of the Control Inputs

Input potential during both half ways of the line phase:

Function	Line Half Wave	Sensor Input	Extension Input		
operated	positive	L	H		
	negative	0	H		
not operated	positive	H	L	or	0
	negative	0	0		L

Figure 5
Application Circuit – Electronic Extension



Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0586 A can be performed with the aid of a single transmission channel.

Interference Immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs and additionally allows almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In case of power failure the set switching state with the recommended external circuitry remains stored. After prolonged power failure ($V_{SS} > -3.6$ V) the circuit turns into off-state.

The control characteristic of the synchronous oscillator (PLL circuit) is designed such that interference due to ripple control signals may cause slight variations in brightness. However, they will not lead to malfunction of the dimmer.

General Information

All time specifications refer to a line frequency of 50 Hz. In case of a line frequency of 60 Hz, the times are reduced accordingly.

Functional description of evaluation logic for sensor and extension inputs

The logic status at the sensor and extension inputs are sampled by latches L1 and L2 using the time slot pattern shown in the timing diagram (Fig. 7).

For operation (ON/OFF or DIMMING) "1" must be present at the D input of FF1 for two consecutive rising edges of the 50 Hz clock pulse of the internal PLL. The flipflops FF1 and FF2, are reset by two logic zeros occurring at the same time at latch outputs L1 and L2.

For operation via the extension input five consecutive sampling values must be "1". The minimum immunity time is therefore approx. 24 ms. Due to the different sampling rates, two sampling values of "1" must follow at the sensor input for an operation to be recognized. In this case the minimum immunity time is approx. 39 ms.

Figure 6
Schematic circuit diagram of evaluation logic for sensor and extension inputs

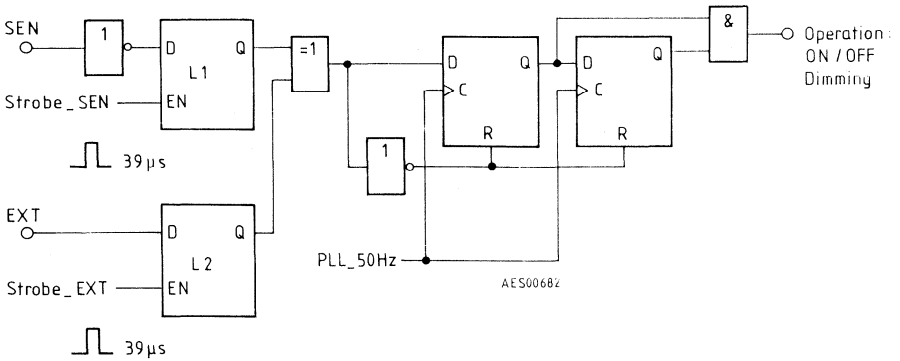


Figure 7
Timing diagram of evaluation logic for sensor and extension inputs

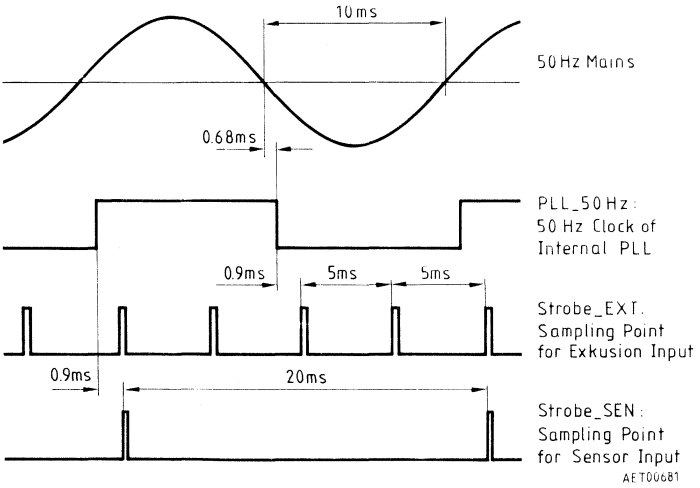
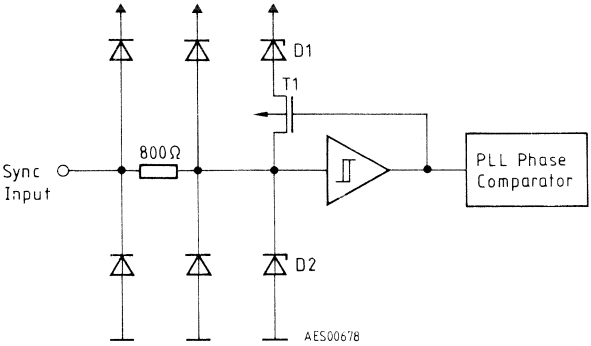


Figure 8
Schematic circuit diagram at synchronous input



Functional Description

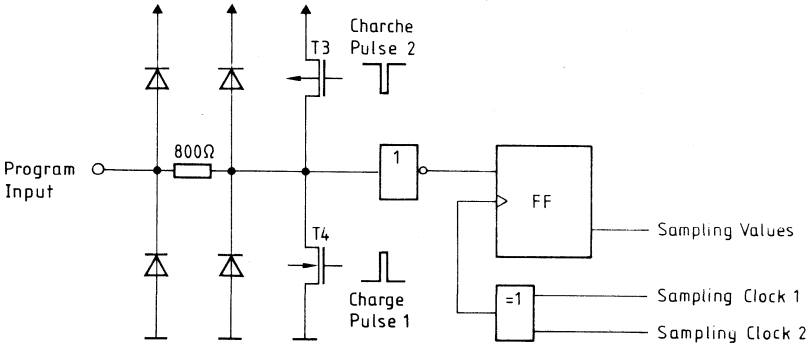
Diodes D1 and D2 have characteristics similar to Z-diodes and start conducting at about 2.5 V.

In spite of the mains voltage at the triac it is ensured – by using R2 **(Fig. 3)** – that the voltages present at the synchronous input of SLB 0586A remain within the supply voltage level.

To obtain a highly stable trigger point for the phase comparator, T1 becomes conductive only after recognizing the synchronisation edge.

Figure 9

Schematic circuit diagram at programming input (pin 2)



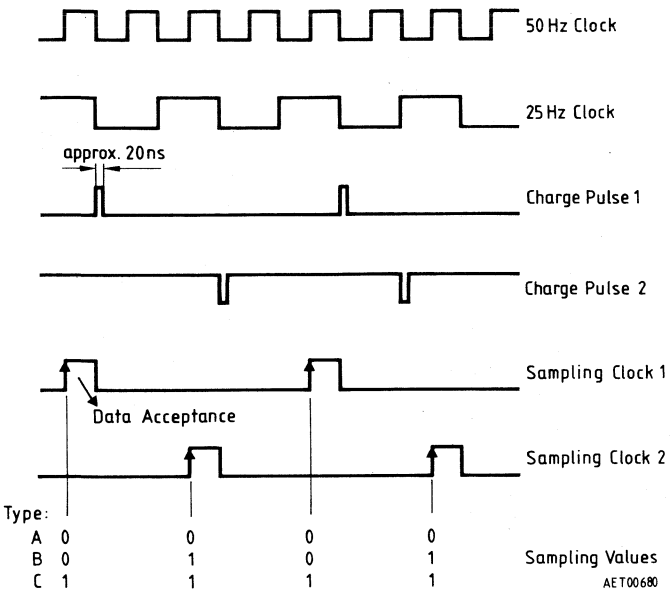
Functional description of pin 2 (programming input)

The SLB 0586A provides the possibility of differentiating between types A, B, and C by appropriate connection of pin 2.

Depending on the charge pulses shown in fig. 10 transistors T3 and T4 alternate in becoming conductive. The currents flowing during the conductive phase of the transistors are sufficient for a charge reversal of the load capacitance of 7 pF max. present at pin 2.

It is important that no major discharge of the capacitance present at pin 2 occurs from the time of charge reversal until the sampling of the voltage level by the two sampling clocks.

Figure 10
Internal timing for differentiating between the three possible modes A, B, and C



A/D Umsetzer,
Schnelle Datenakquisition

A/D Converters,
High-Speed Data Acquisition

Selector Guide

Type	Package	Resolution Bit	Conversion time[3]	Strobe frequency max MHz	Supply voltage V	Analog Multiplex	TUV[4] LSB max.	Page
Ultra-Fast ADC								
SDA 6020	C-DIP-16	6	20 ns	50	+5, −5.2		±1/2[5]	359
SDA 5200N; S	C-DIP-16	6	10 ns	100	+5, −5.2		±1/2[5]	368
SDA 8200	C-DIP-40	6	4 ns	300	+5, −4.5		±1/4[5]	375
SDA 8010	C-DIP-24	8	10 ns	100	+5, −4.5		±1/2[5]	392
High-Speed Data Acquisition								
SDA 8020 N	PL-CC-68	100 MHz/4 x 25 MHz shift register						405
Microprocessor-Compatible ADC								
SDA 0808 B	P-DIP-28	8	13 µs	1.5[1]	5	8 x	±1/2	424
SDA 0808 N	PL-CC-28	8	13 µs	1.5[1]	5	8 x	±1/2	424
SDA 1808 N	PL-CC-28	8	15 µs	2.5[1]	5	8 x	±1	424
SDA 0810 B	P-DIP-28	10	15 µs	1.5[1]	5	8 x	±1/2	437
SDA 0810 N	PL-CC-28	10	15 µs	1[1]	5	8 x	±1/2	437
SDA 1810 N	PL-CC-28	10	15 µs	2[1]	5	8 x	±1	437
SDA 1810 D	P-DIP-28	10	15 µs	2[1]/66 kHz[2]	5	8 x	±1.25	437
SDA 1810 DN	PL-CC-28	10	15 µs	2[1]/66 kHz[2]	5	8 x	±1.25	437
SDA 0812 A	P-DIP-28	12	8.5 µs	2[1]	5	4 x	±1/2	452
SDA 0812 AN	PL-CC-28	12	8.5 µs	2[1]	5	4 x	±1/2	452
SDA 1812 D	P-DIP-28	12	8.5 µs	2[1]/100 kHz[2]	5	4 x	±0.75	452
SDA 1812 DN	PL-CC-28	12	8.5 µs	2[1]/100 kHz[2]	5	4 x	±0.75	452

= SMD

[1] Clock frequency
[2] Sampling rate
[3] Including sample time
[4] Total Unadjusted Error
[5] Linearity Error

SIEMENS

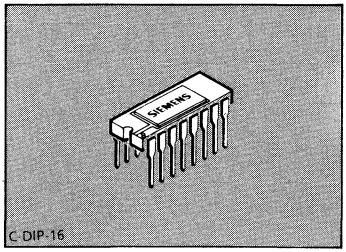
6-Bit A/D Converter, 50 MHz

SDA 6020

Bipolar IC

Features

- Conversion up to Nyquist frequency (25 MHz)
- 6-bit resolution (1.6%), simple extension to 8 bits
- 50 MHz strobe frequency
- ±1/2 LSB max. linearity error
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL-compatible (ECL → TTL matching possible, e.g. with SH 100.255
- Low power dissipation of 450 mW
- Logic-compatible supply voltage +5 V; −5.2 V



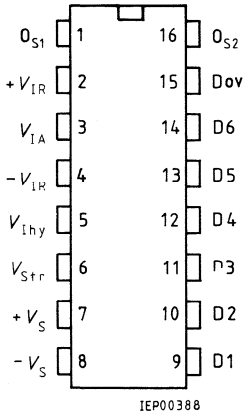
6

Type	Ordering Code	Package
■ SDA 6020	Q67000-Y584	C-DIP-16

■ Not for new design

Pin Configuration

top view



Pin Definitions and Functions

Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< 2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	V_{Str}	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	D ov	Overflow
16	0_{S2}	Digital ground of output stages

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$ $-V_{IR}$	−3.0	3.0	V
Strobe	V_{Str}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System – air	$R_{th\ SA}$		70	K/W

Characteristics

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Power Supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog Section $T_A = 25\,°C$; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal Input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert(+V_{IR\,max}) - (-V_{IR\,min})\rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference Input					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	$64\,R$	96	128	256	Ω
Digital Section					
Strobe Input					
H-input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L-input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H-input voltage	I_{IH}	5	30	100	µA
L-input voltage	I_{IL}	5	30	100	µA
Data Outputs 100 Ω to −2 V					
H-output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L-output voltage	V_{QL}	−2.0	−1.7	−1.5	V

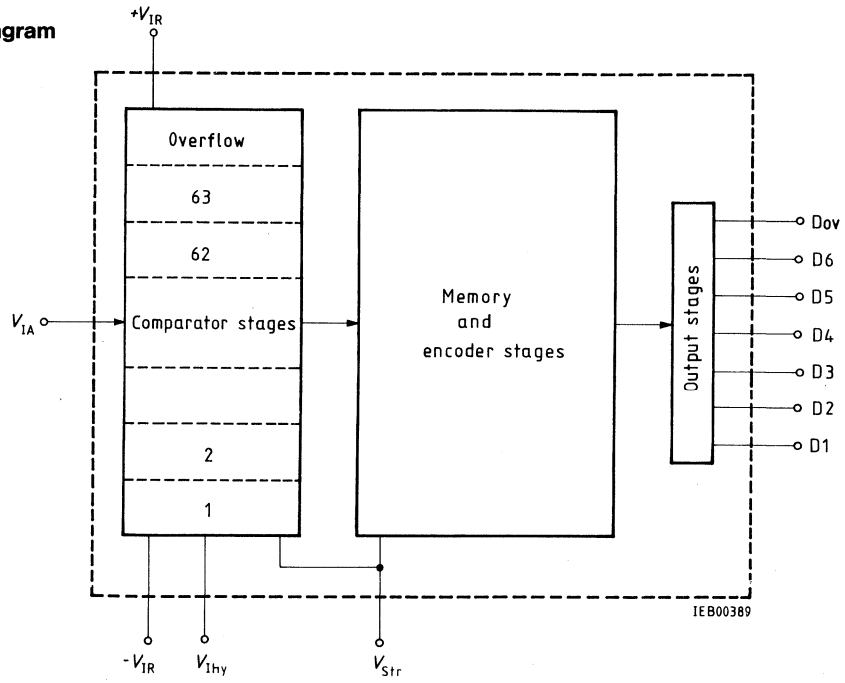
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		8	10[1])	ns
Signal transition time[2])	$t_{TLH\ Qmax}$		9		ns
Signal transition time[2])	$t_{THL\ Qmin}$		11		ns
Strobe frequency	f_{strobe}	50			MHz

1) Exceeding this value at strobe frequencies of less than 50 MHz is quite permissible as long as the remaining hold time is adequate for reliable data transfer.

2) The data transfer into the following circuit should occur with a delay t_D referred to the rising strobe edge in the range:

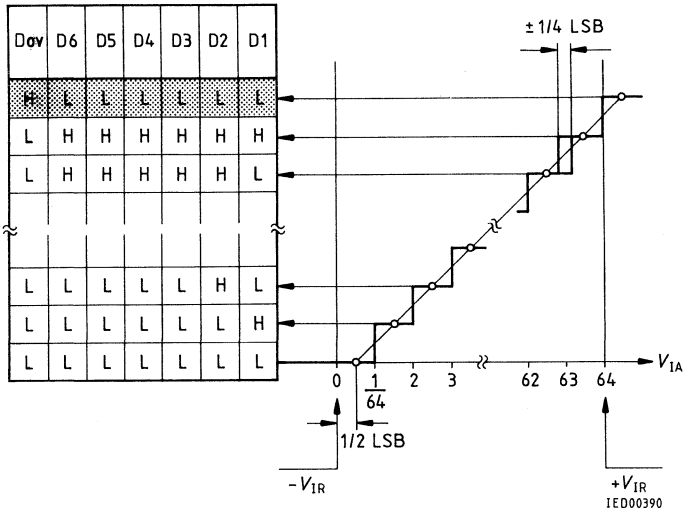
$$t_{TLH\ Qmax} + t_{hold/2} < t_D < t_{hold} + t_{THL\ Qmin}$$

Block Diagram

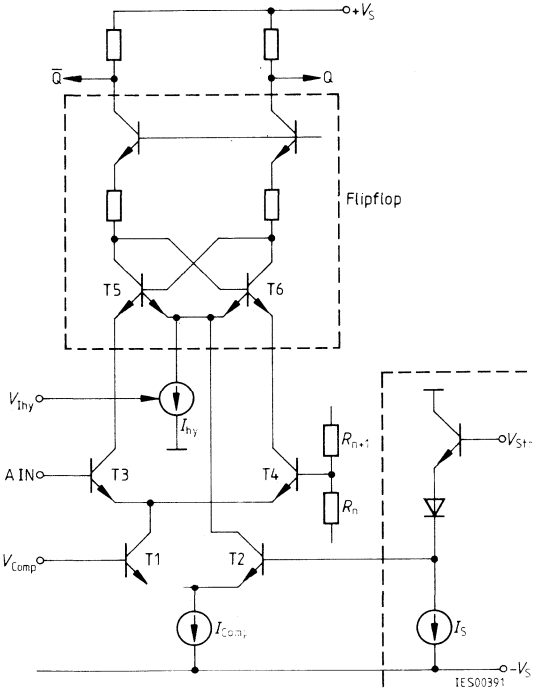


Transfer Characteristic and Truth Table

Dov	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L

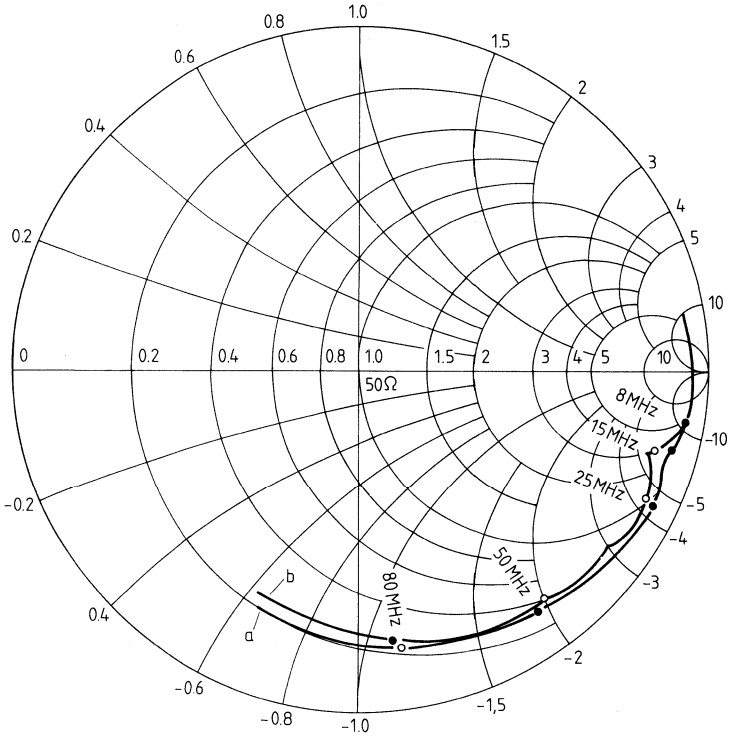


Input Stage

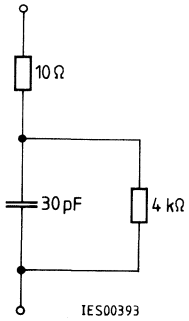


Smith Diagram

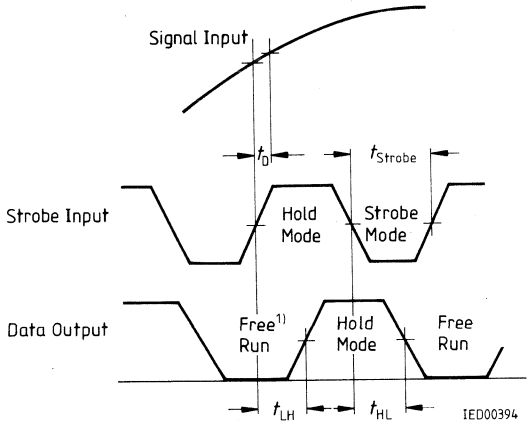
a) Nyquist plot of input impedance
b) Nyquist plot of equivalent circuit



Equivalent Circuit

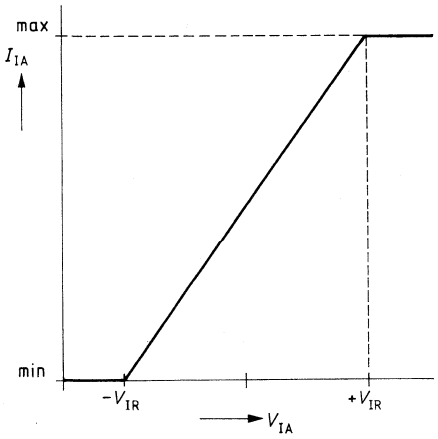


Pulse Diagram of Strobe Input and Data Outputs

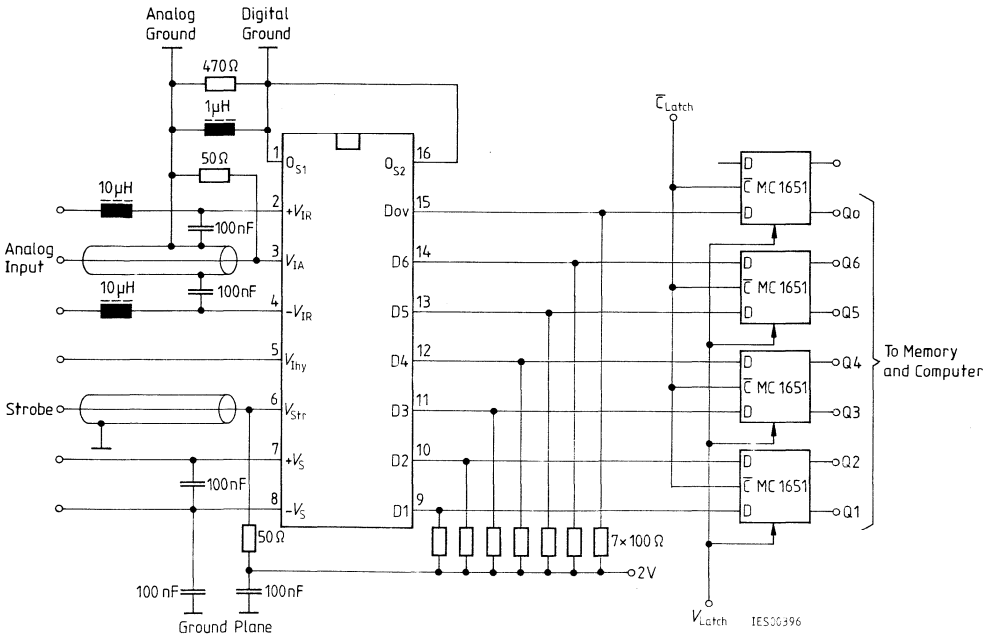


[1] undefined Output Levels

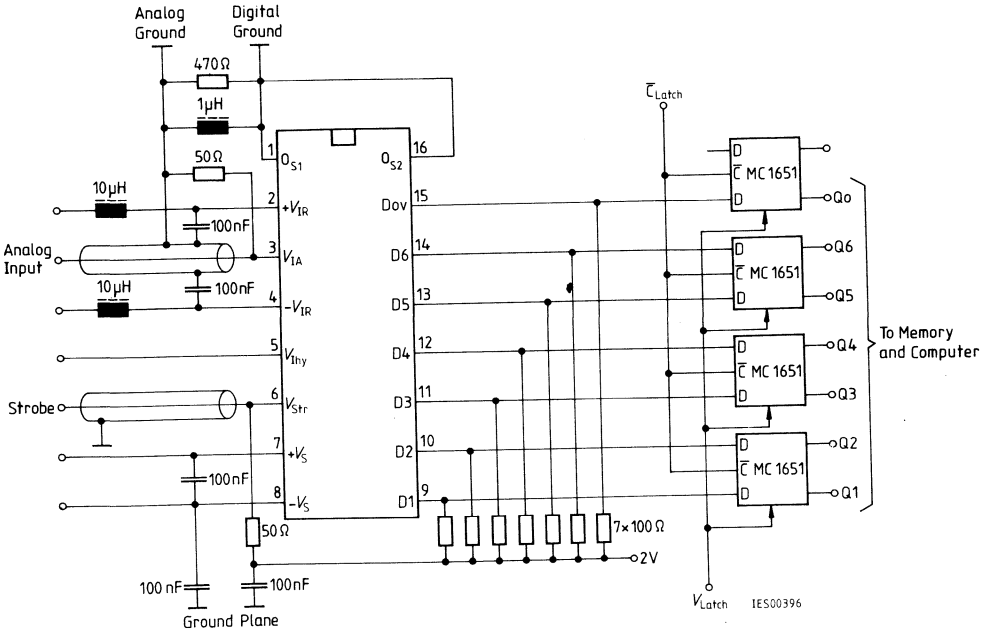
Input Current versus Input Voltage



Test Circuit



Test Circuit



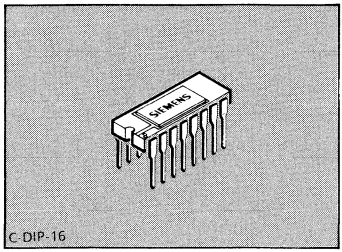
6-Bit A/D Converter, 100 MHz

SDA 5200

Bipolar IC

Features

- Strobe frequency 100 MHz
- 6-bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs (SDA 5200 N), thus simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to Nyquist limit
- ± 1/2 LSB max. linearity error
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V



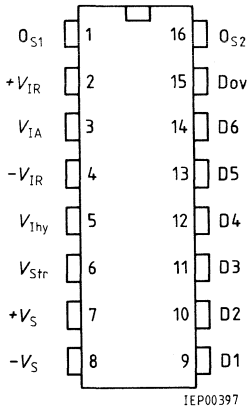
Type	Ordering Code	Package
SDA 5200 N	Q67000-A2242	C-DIP-16
SDA 5200 S	Q67000-A2243	C-DIP-16

The SDA 5200 is an ultrafast A/D converter with 6-bit resolution and overflow output. After cascading, it enables straightforward implementing of 7 or 8 bit A/D converters, respectively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and excellent linearity, the SDA 5200 is outstanding for a broad analog bandwidth which – from the analog side – permits application up to the limit of the Nyquist theorem.

The SDA 5200 is pin-compatible with the SDA 6020.

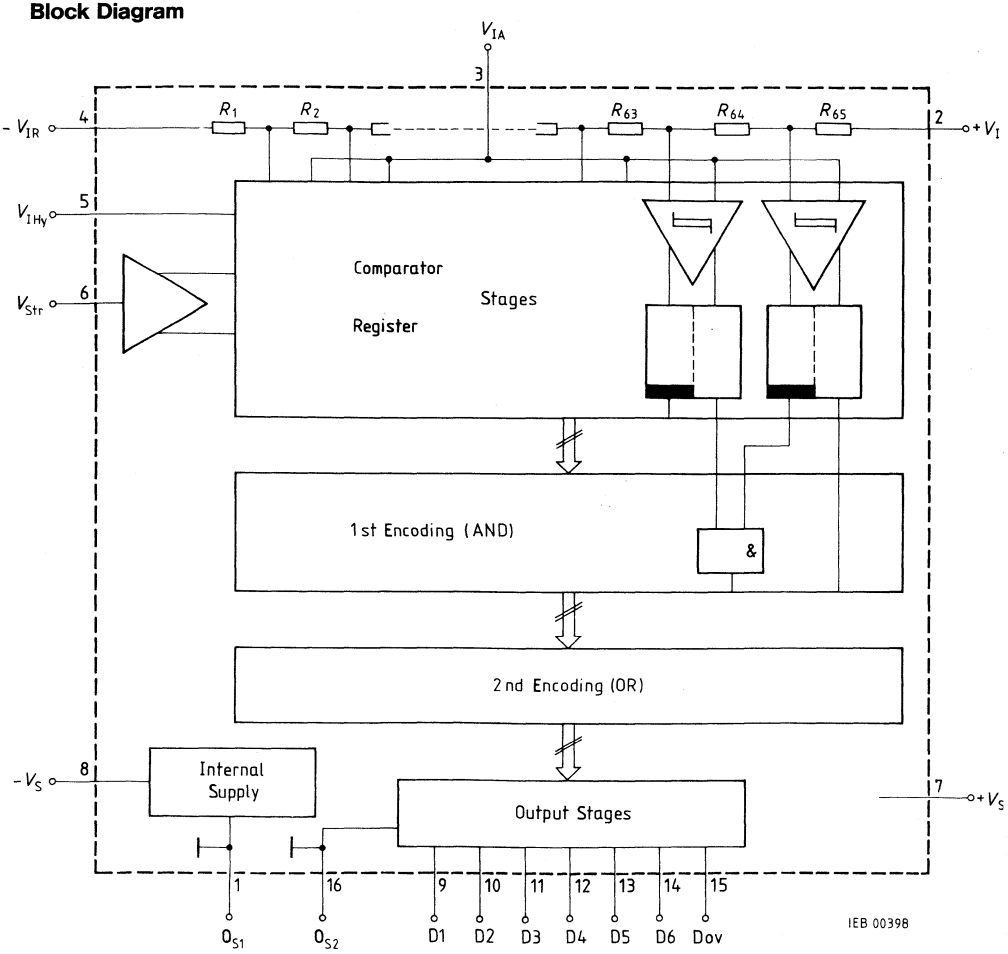
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	D_{OV}	Overflow output
16	0_{S2}	Digital ground 2

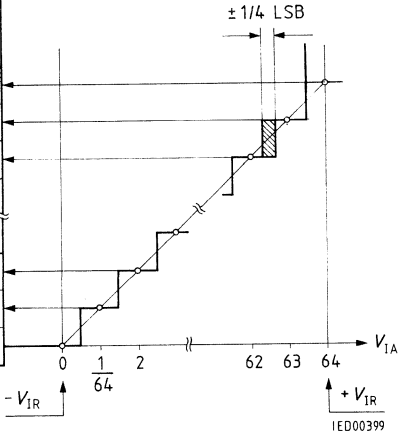
Block Diagram



Transfer Characteristic and Truth Table

SDA 5200 N

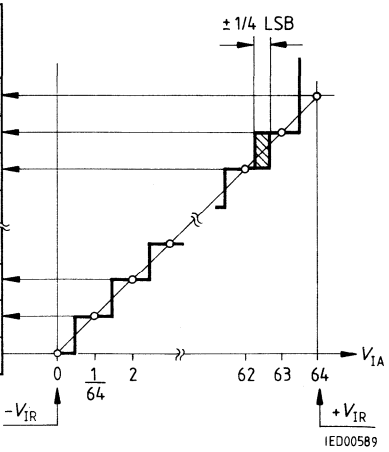
Dov	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Transfer Characteristic and Truth Table

SDA 5200 S

Do	D6	D5	D4	D3	D2	D1
H	H	H	H	H	H	H
L	H	H	H	H	H	H
L	H	H	H	H	H	L
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{I\,A}+V_{I\,R}, -V_{I\,R}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1}-0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
System – air	$R_{th\,SA}$		70	K/W
Junction	$R_{th\,J}$		16	K/W

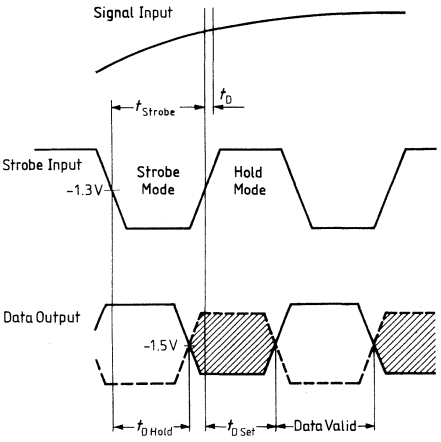
Characteristics

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Power Supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{I\,A} \leq -V_{I\,R}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{I\,A} \leq -V_{I\,R}$	I_{S-}		55	80	mA
Analog Section					
Signal Input					
Max. input voltage	$V_{I\,Amax}$	$-V_{I\,Rmin}$		$+V_{I\,Rmax}$	V
$V_{I\,Amax} = \lvert(+V_{I\,Rmax}) - (-V_{I\,Rmin})\rvert$				5	V
$V_{I\,A}$ for 6 bit resolution			0.3		V
$V_{I\,A}$ for 1/2 LSB linearity		1.2	0.6		V
$V_{I\,A}$ for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{I\,A} = +V_{I\,R}$	$I_{I\,A}$		150	500	µA
at $V_{I\,A} < -V_{I\,R}$	$I_{I\,A}$	−500		500	nA
Input capacitance					
at $V_{I\,A} < -V_{I\,R}$	$C_{I\,A}$		25		pF
Reference Input					
Pos. reference voltage	$+V_{I\,R}$	−2,5		2	V
Neg. reference voltage	$-V_{I\,R}$	−3.0		1.5	V
Reference resistance	R_{REF}	96	128	195	Ω

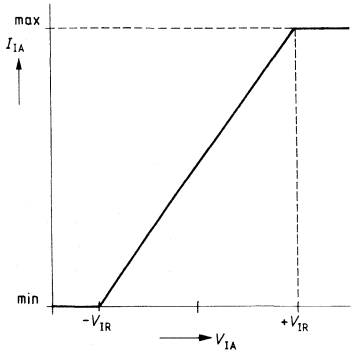
Characteristics (cont'd)

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Digital Section					
Strobe Input					
H-input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L-input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H-input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA
Data Outputs 100 Ω to −2 V					
H-output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L-output voltage	V_{QL}	−2.0	−1.7	−1.5	V
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time SDA 5200 N; S	$t_{D\,Hold}$		12	17	ns
Signal transition time SDA 5200 N; S	$t_{D\,Set}$		12	17	ns
Max. strobe frequency SDA 5200 N; S	f_{strobe}	100			MHz
Max. slew rate	SR		0.5		V/ns
Bandwidth (−3 dB)	B		140		MHz

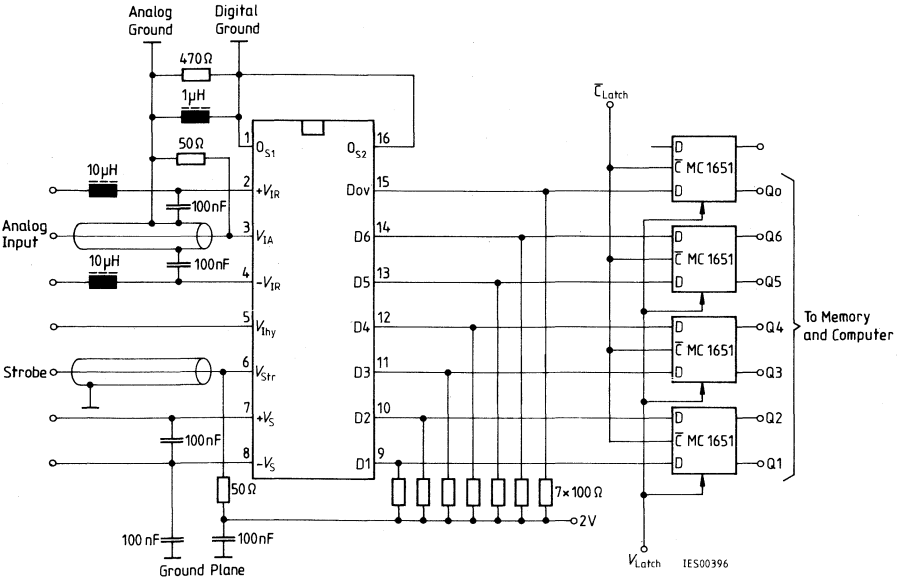
Pulse diagram of strobe input and data outputs



Input current versus input voltage

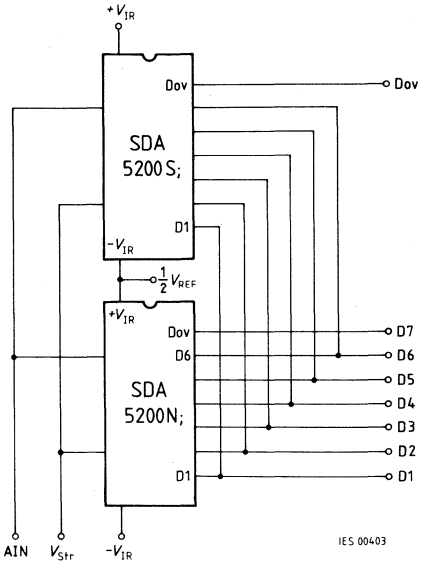


Test Circuit



Application Circuit

7-bit A/D converter with SDA 5200 S, N



SIEMENS

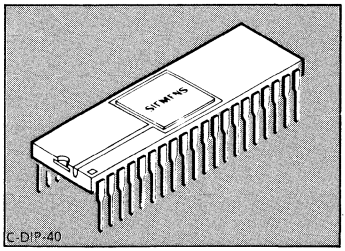
6-Bit A/D Converter, 300 MHz

SDA 8200

Bipolar IC

Features

- 300 MHz strobe frequency
- 5.4 effective bits ($f_{analog} = 100$ MHz)
- ± 0.25 LSB max. linearity error
- ± 1 V input voltage range
- 12 pF input capacitance
- Optionally 2:1 demultiplexed output data
- No pipelining in "Transparent Mode"
- Data ready clock output
- Overflow output

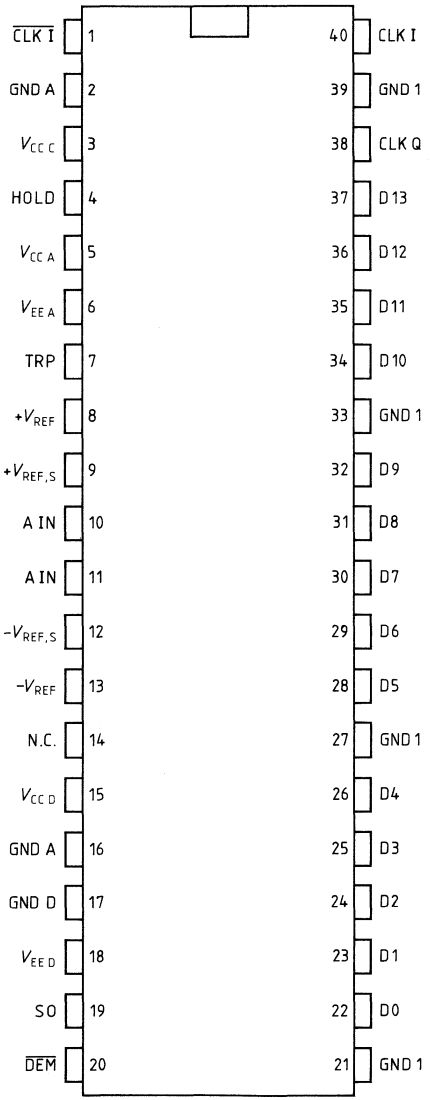


6

Type	Ordering Code	Package
SDA 8200	Q67000-A8164	C-DIP-40

The SDA 8200 is an ultrafast A/D converter operating according to the parallel principle with a resolution of 6 bits, a guaranteed clock frequency of 300 MHz and high performance up to 150 MHz full-scale input.

Figure 1
Pin Configuration
(top view)



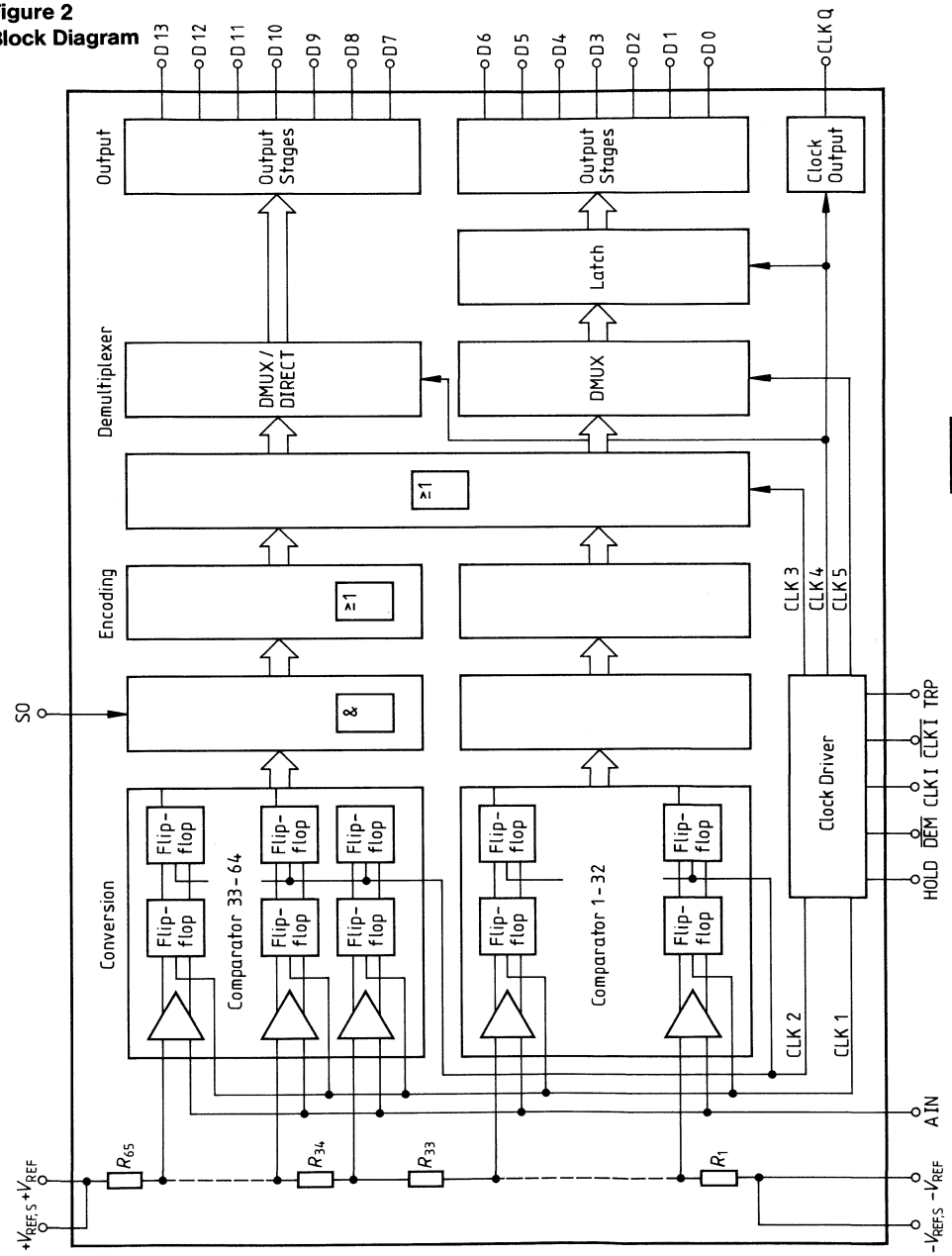
Pin Definitions and Functions

Pin	Name	Symbol	Function
10, 11	Analog input	A IN	Input for the signal to be digitalized. To lower parasitic inductance two pins are used for this input.
13, 12 8, 9	Reference inputs	$-V_{REF}$ $-V_{REF,S}$ $+V_{REF}$ $+V_{REF,S}$	Bottom and top of the reference-resistor string. The inputs may either be used as sense and force for a Kelvin connection or connected in parallel to minimize parasitic resistance.
40, 1	Conversion clock	CLK I, $\overline{\text{CLK I}}$	Every rising edge of a signal applied to CLK I initiates sampling of the analog signal. Either ECL (differential or single-ended) or sinewave clock inputs may be used.
38	Clock output	CLK Q	Provides an ECL signal which can be used to control the transfer of the digital outputs into subsequent circuits (not available in the transparent mode). In the demultiplexing mode the frequency of CLK Q is half the sampling frequency (see "Modes of Operation").
22, 23 24, 25 26, 28 29	Output word 1	D0...D6	ECL outputs including overflow bit (D6) valid only in the demultiplexing mode. In this mode every first digital word of a pair of subsequent samples is delivered with a clock rate of half the sampling frequency. In the direct modes these outputs are undefined.
30, 31 32, 34 35, 36 37	Output word 2	D7...D13	ECL outputs (D13 overflow) delivering the second word of a pair in the demultiplexing mode. In the direct modes the digital data at these outputs appear with a clock rate equal to the sampling rate.

Pin Definitions and Functions (cont'd)

Pin	Name	Symbol	Function
19	Set Overflow	SO	A logic H at this ECL input or strapping the pin to GND D causes the overflow bit to be H and the data bits to be L when the analog signal exceeds the uppermost comparator threshold. If the pin is not connected or L is applied the data bits remain H in case of overflow.
20	Demultiplexing	$\overline{\text{DEM}}$	Setting this pin to H or strapping it to GND D sets the device in the direct mode.
7	Set transparent	TRP	A logic H (or GND D) at this input sets the device in the transparent mode (no pipelining). In this mode both DEM and HOLD inputs become ineffective. Besides, no clock output is provided.
4	Hold	HOLD	H active ECL input that immediately stops data transfer to the outputs (D0...D13) and inhibits the clock output. The last data word remains at the output and CLK Q is forced Low. In the direct mode the first valid output data together with the output clock appear one clock cycle after HOLD is released. In the demultiplexing mode clock and valid data appear after two conversion clock cycles with the first data word (corresponding to the first sampled value after HOLD is set to L) always present on D0...D6. HOLD is inactive in the transparent mode.
5, 6, 2, 16,	Analog supply	$V_{CC\,A}$, $V_{EE\,A}$, GND A	} Supply voltages
15, 18, 17,	Digital supply	$V_{CC\,D}$, $V_{EE\,D}$, GND D	
3	Clock supply	$V_{CC\,C}$	
21, 27 33, 39	Output ground	GND 1	Return path for the emitter-follower current in the ECL output stages.

Figure 2
Block Diagram



6

Circuit Description

The A/D conversion is carried out in an array of 64 comparators connected in parallel to the analog input A IN. The signal is compared simultaneously with 64 equally spaced reference voltages provided by the resistor string $R_1 \ldots R_{65}$. With the rising edge of the conversion clock CLK I the result of the comparison is stored in the first comparator latch and afterwards passed to the second latch in a pipelining operation. Then the digital result of the comparison is pending at the comparators' output in a so-called thermometer code. Three subsequent encoding stages form the binary representation of the sampled value and a demultiplexer optionally divides the 300-MHz output data stream into two 150-MHz channels which are converted to ECL levels by two parallel output driver blocks. All clock signals for the pipelining and demultiplexing stages are formed internally by a clock driver circuit connected to the external conversion clock via CLK I. A clock signal for transferring the output data into subsequent circuitry is provided at CLK Q. If, however, the pipelined operation is disadvantageous (e.g. in subranging converter applications), all internal latches following the comparators may be set transparent via the programming input TRP. So any encode command directly causes the appearance of the respective output data after a short delay.

Clock Input (CLK I)

The clock inputs are designed to be driven differentially with ECL levels **(figure 3a).** Since CLK I is internally biased to −1.32 V, it is also possible to use CLK I single-ended. With this configuration a bypass capacitor from CLK I to GND A is recommended.

In this case the clock has to be stable with regard to the internal reference voltage to ensure the specified timing ($t_{WH,\ CLK\ I}$, $t_{WL,\ CLK\ I}$) over the operating range. For a continuously applied input clock the configuration shown in **figure 3b** is recommended. A capacitively coupled sinewave clock input (300 m V_{pp} typ.) can then be employed without degradation in performance **(figure 3c)**.

Analog and Reference Inputs

The input voltage range is determined by the voltages applied to the top ($+V_{REF}$) and bottom ($-V_{REF}$) of the resistor string. Two pins for each voltage allow a Kelvin connection (sense, force) if very high precision is required. Otherwise the parallel connection of these pins ensures low parasitic resistances. The analog input can be driven from a customary 50 Ω source since the input capacitance is a very low 12 pF, independent of input voltage, and the input voltage range may be set symmetric to ground.

Supply System

The supply system breaks down into three parts. The analog supply $V_{CC\ A}$, $V_{EE\ A}$ is connected to the first comparator stages, the digital supply $V_{CC\ D}$, $V_{EE\ D}$ serves for encoding, demultiplexer and output stages, and a special clock supply $V_{CC\ C}$ is provided to separate the high and noisy driver currents from the other supply systems. Additionally, a separate return path for the currents of the output emitter followers is established via GND 1.

Modes of Operation

The analog signal is sampled with every rising edge of the clock signal CLK I. By programming the TRP and DEM inputs three different output modes can be chosen:

a) Direct modes (figure 4):

The output data appear at the outputs D7...D13 with a word rate equal to the sampling rate. The logic state of the outputs D0...D6 is not defined.

One of two submodes can be chosen:

(I) Normal Mode (TRP low, DEM high)
Due to internal pipelining the output data appear one clock cycle after the rising edge of CLK I (sampling moment). CLK Q delivers a clock signal with the same frequency as CLK I.

(II) Transparent Mode (TRP high)
After a sampling command the associated output data appear directly with a delay of less than 7 ns. No output clock is available.

b) Demultiplexing mode (TRP low, DEM low; figure 5)

The output words corresponding to two subsequent samples appear simultaneously at the outputs D0...D6 and D7...D13, respectively, with half the clock rate of the conversion clock CLK I. After a HOLD pulse the word belonging to the first sample is always shown at D0...D6 and the delay between the first sample and output is two cycles of the conversion clock CLK I. At CLK Q a clock signal with half the frequency of the conversion clock, synchronous to the output data, is provided.

In all modes the output format in the overflow status can be programmed via the SO input. Setting SO to H causes the overflow bits (D6 and D13, respectively) to remain H and the data bits (D0...D5 and D7...D12, respectively) to go to L when the analog signal exceeds the threshold of comparator 64. If SO is set to L or not connected all data and overflow bits remain H in case of overflow **(figure 6).**

The HOLD input allows the output digital data stream to be stopped and restarted with defined output conditions. It is disabled in the transparent mode.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Pos. supply voltages	$V_{CC\,A}$ $V_{CC\,D}$ $V_{CC\,C}$	−0.3	6.0	V
Neg. supply voltages	$V_{EE\,A}$ $V_{EE\,D}$	−6.0	0.3	V
Analog input voltages	$+V_{REF}$ $-V_{REF}$ V_{AIN}	−2.5[1])	1.5	V
Digital input voltages	V_{CLKI} $V_{\overline{CKLI}}$ V_{DEM} V_{SO} V_{TRP}	−3.0	0.3	V
Output current	$I_{D0} \dots I_{D13}$		20	mA
Junction temperature	T_j		150	°C
Ambient temperature (without heat sink)	T_A	−25	50	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance Junction – ambient (without heat sink)	$R_{th\,JA}$		45	K/W

[1]) $+V_{REF}$ has to be more positive than $-V_{REF}$.

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$,
$T_j = 25\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Supply					
Pos. supply currents	$I_{VCC\,A}$		50		mA
	$I_{VCC\,D}$		65		mA
	$I_{VCC\,C}$		35		mA
Total pos. supply current	I_{CC}			170	mA
Neg. supply currents	$I_{VEE\,A}$		45		mA
	$I_{VEE\,D}$		125		mA
Total neg. supply current	I_{EE}			180	mA
Power dissipation	P_D		1.5	1.8	W
Permissible supply voltage difference	ΔV_{CC}, ΔV_{EE}			100	mV

Characteristics

$V_{CC\,A}$, $V_{CC,\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$,
$T_j = 25\ °C$ to $125\ °C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Analog Section					
Signal input					
Voltage range	V_{AIN}	−2		1	V
Max. input current $V_{AIN} = +V_{REF}$	I_{AIN}		500	700	µA
Input capacitance	C_I		12		pF
Reference Inputs					
Reference voltages[4])	$+V_{REF}$, $-V_{REF}$	−2		1	V
Reference resistance	R_{REF}		200		Ω
Temperature coefficient of reference resistor	TC		1.7		10^{-3}/K
Digital Section					
Logic Levels					
H-input voltage[1])	V_{IH}	−1.165			V
L-input voltage[1])	V_{IL}			−1.475	V
H-output voltage[2]) $R_L = 100\ \Omega$	V_{QH}	−1.025		−0.88	V
L-output voltage[2]) $R_L = 100\ \Omega$	V_{QL}	−1.810		−1.620	V
Clock Inputs[3])					
Input current	I_{CLKI}			20	µA
Max. clock frequency	$f_{c,\,max}$	300	350		MHz
Aperture delay	t_A		1		ns
Hold time	$t_{WH,\,CLKI}$	1.2			ns
Strobe time	$t_{WL,\,CLKI}$	1.2			ns
Programming Inputs[3])					
H-input current	I_{IH}		80		µA
L-input current	I_{IL}		60		µA
Hold Input					
Setup time	$t_{S,\,HOLD}$	0.5			ns
Release time	$t_{R,\,HOLD}$	2			ns
High pulse width	$t_{W,\,HOLD}$	1			ns

[1]) applies to DEM, SO, HOLD, TRP
[2]) applies to DEM, SO, HOLD, TRP
[3]) applies to CLKQ, D0...D13
[4]) see "Circuit Description"

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,D} = -4.5\ V \pm 5\%$, $25\,°C < T_j < 125\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Data Outputs[1])						
Data valid range						
normal mode	$t_{V,\,N}$	3	3.5		ns	$f_c = 250$ MHz
transparent mode	$t_{V,\,T}$	2.5			ns	$f_c = 250$ MHz
demultiplexing mode	$t_{V,\,D}$	5	5.8		ns	$f_c = 300$ MHz
Output timing						
normal mode	$t_{d,\,N}$	0.5[2])			ns	$f_c = 250$ MHz
transparent mode	$t_{d,\,T}$			9	ns	
demultiplexing mode	$t_{d,\,D}$	0[2])			ns	$f_c = 300$ MHz
Clock Output						
Max. frequency[3])	$f_{Q\,max}$		250		MHz	
Clock delay LH	t_{dLH}		6		ns	
Clock delay HL	t_{dHL}		5.5		ns	
Static Nonlinearity						
Integral nonlinearity	*INL*			0.25	LSB	
Differential nonlinearity	*DNL*			0.25	LSB	
Dynamic Performance[4])						
Large signal bandwidth	f_{3dB}		250		MHz	
Effective resolution[5])						
$f_c = 300$ MHz, $V_{AIN} = 2\ V_{pp}$						
$f_{AIN} = 10$ MHz			5.9		bit	
$f_{AIN} = 50$ MHz		5.6	5.8		bit	
$f_{AIN} = 100$ MHz		5.3	5.4		bit	
$f_{AIN} = 150$ MHz			5.0		bit	
Signal-to-noise ratio[6])	*SNR*					
$f_c = 300$ MHz, $V_{AIN} = 2\ V_{pp}$						
$f_{AIN} = 50$ MHz		36	37.5		dB	
$f_{AIN} = 100$ MHz		35	36.5		dB	
$f_c = 300$ MHz, $V_{AIN} = 1\ V_{pp}$						
$f_{AIN} = 50$ MHz			37		dB	
$f_{AIN} = 100$ MHz			36		dB	
Total harmonic distortion	*THD*					
$f_{AIN} = 50$ MHz, $V_{AIN} = 2\ V_{pp}$			−44		dB	
$f_{AIN} = 100$ MHz, $V_{AIN} = 2\ V_{pp}$			−39		dB	

1) Values refer to sinewave clock inputs (duty cycle 50%)
2) Increases with sampling period
3) Has been chosen lower than the max. sampling frequency because at very high input clock rates the device should preferably be operated in the demultiplexing mode.
4) Measured in a 50 Ω analog system at 300 MHz sampling rate (300 mV_{pp} sinewave clock)
5) Includes both noise and harmonic distortions
6) Without the effect of harmonics: thus b_{eff}, *SNR* [dB] and *THD* [dB] are related by
$b_{eff} = \{-10 \log -(10^{-SNR/10} + 10^{THD/10}) - 1.8\}/6$

Clock input
Figure 3a

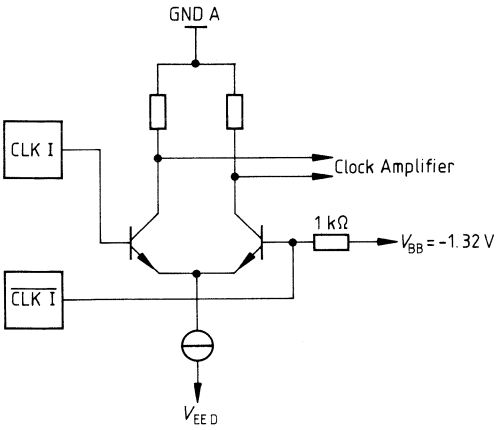


Figure 3b

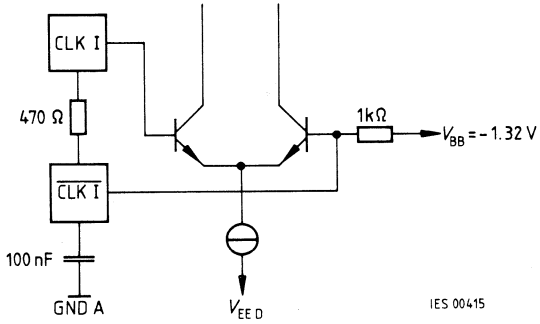


Figure 3c

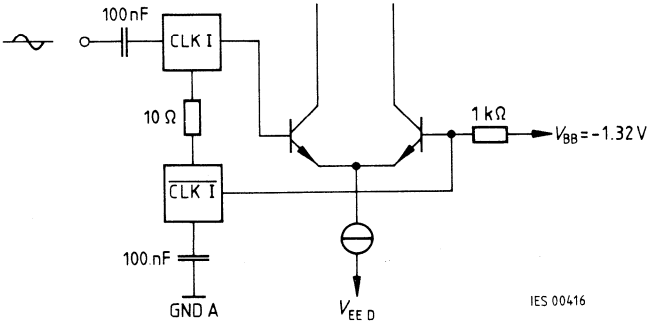


Figure 4
Timing Diagram
Direct Modes

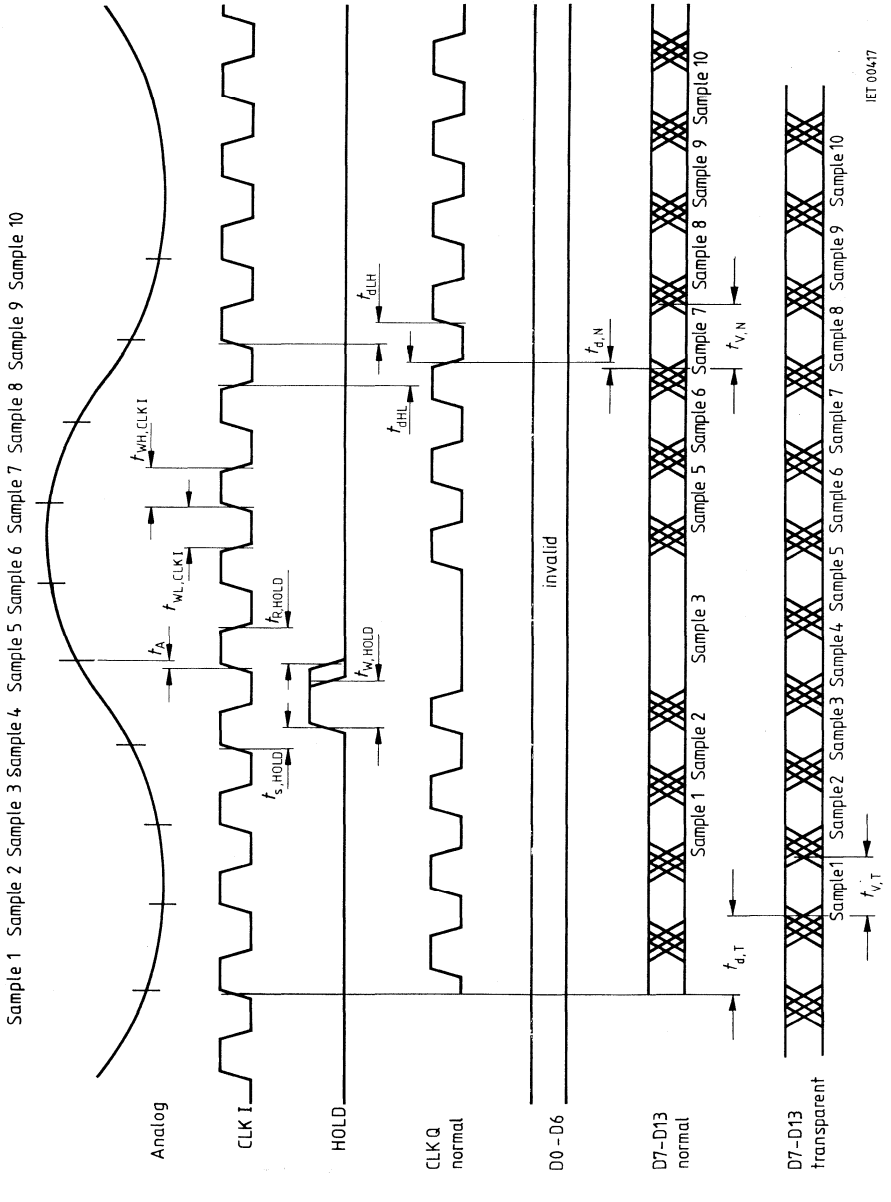


Figure 5
Demultiplexing Mode

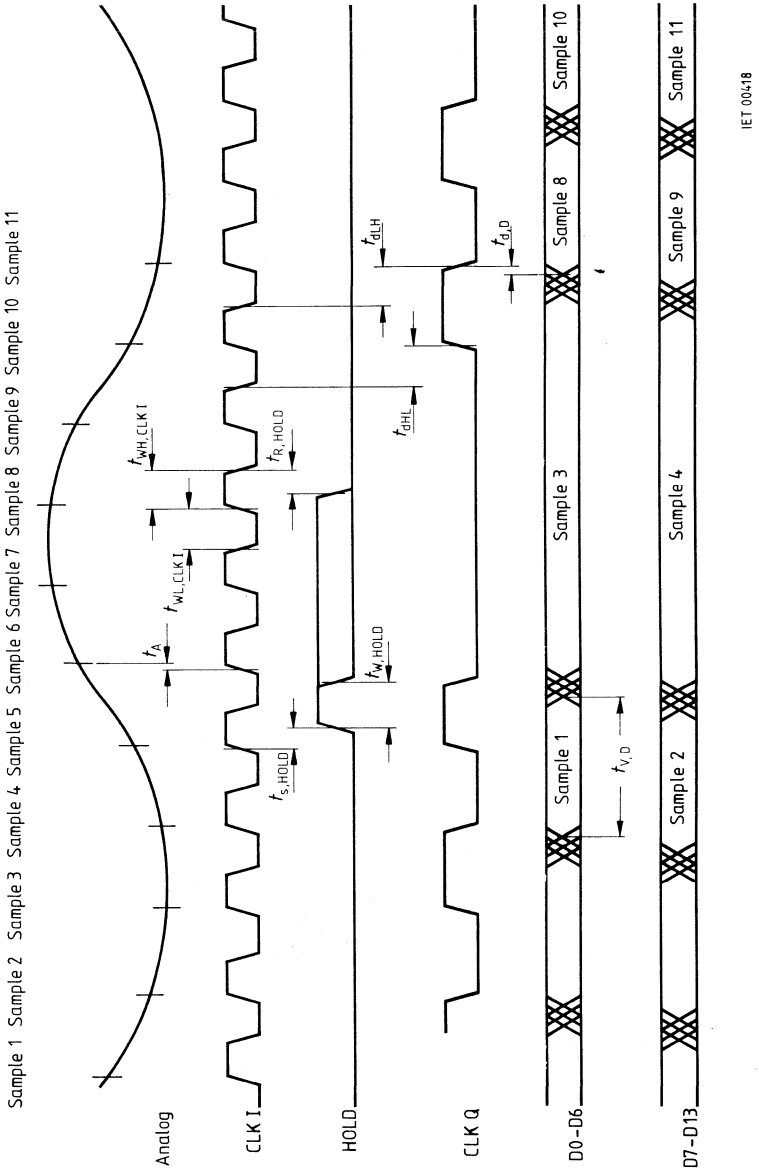
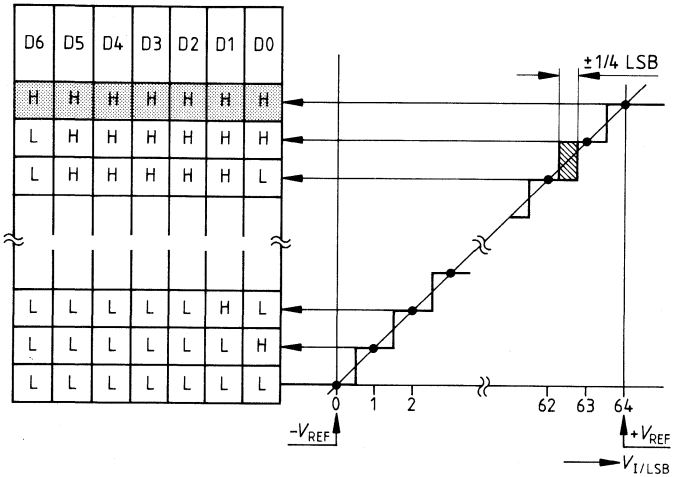
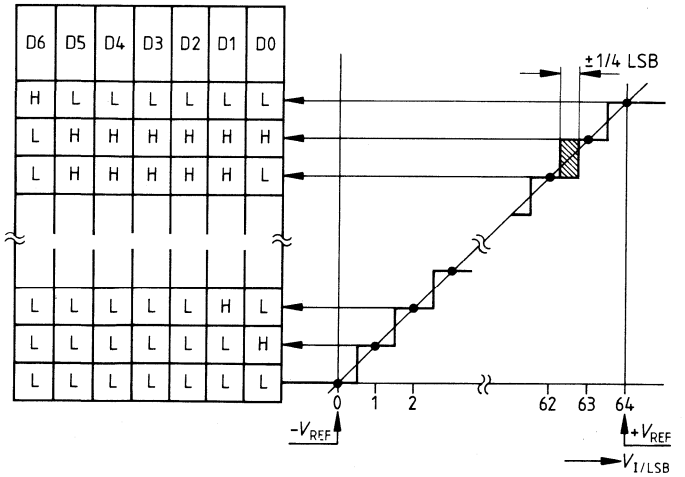


Figure 6
Transfer Characteristic and Truth Table

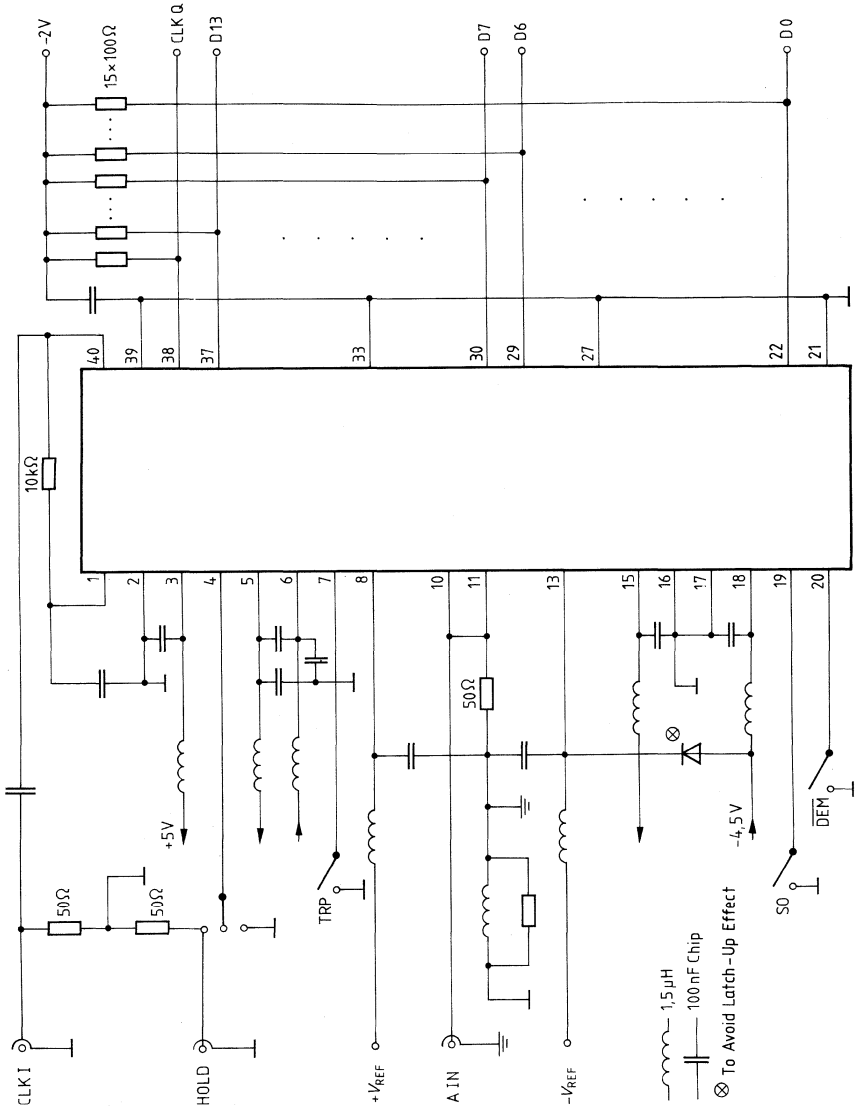


a) SO set to "L" or not connected

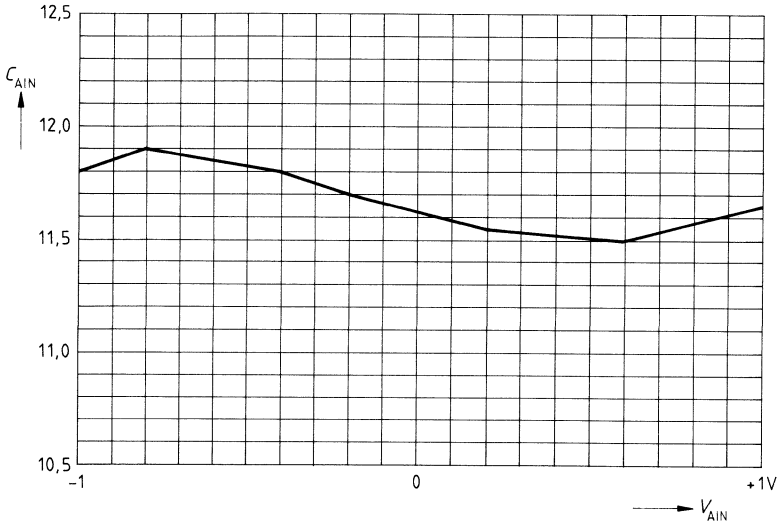


b) SO set to "H" or strapped to ground

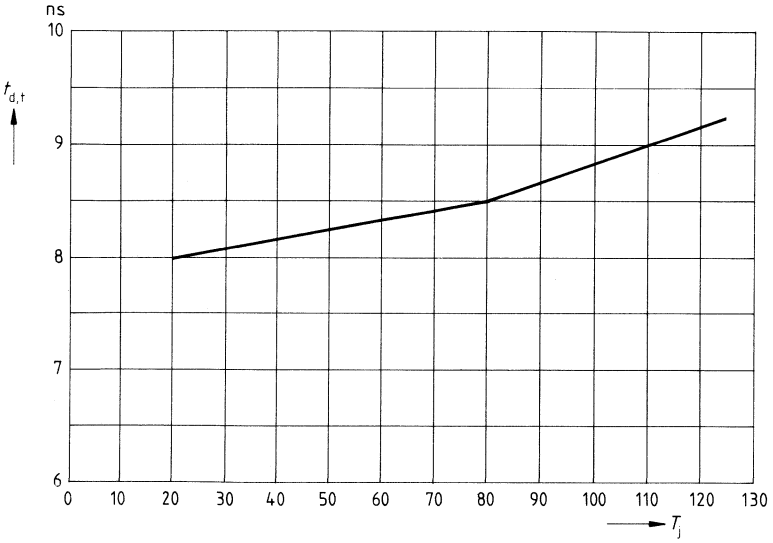
Figure 7
Test Circuit



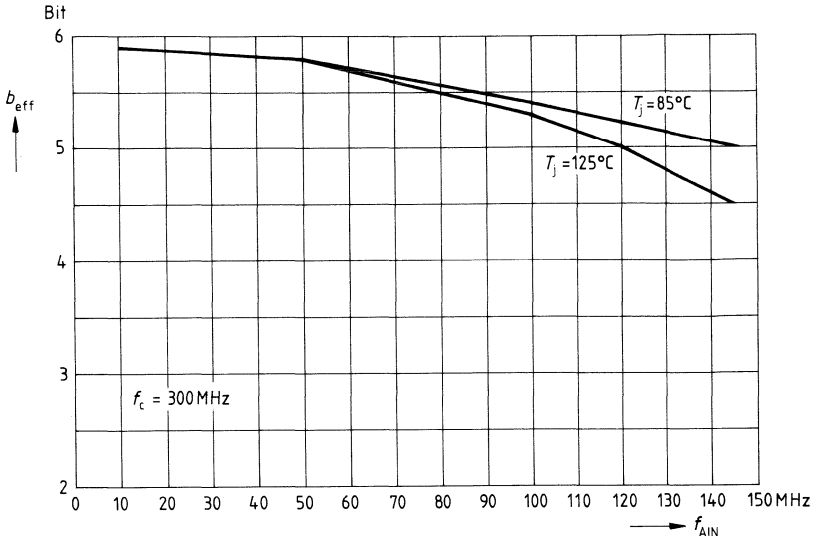
Analog Input Capacitance C_{AIN} versus Input Bias Voltage



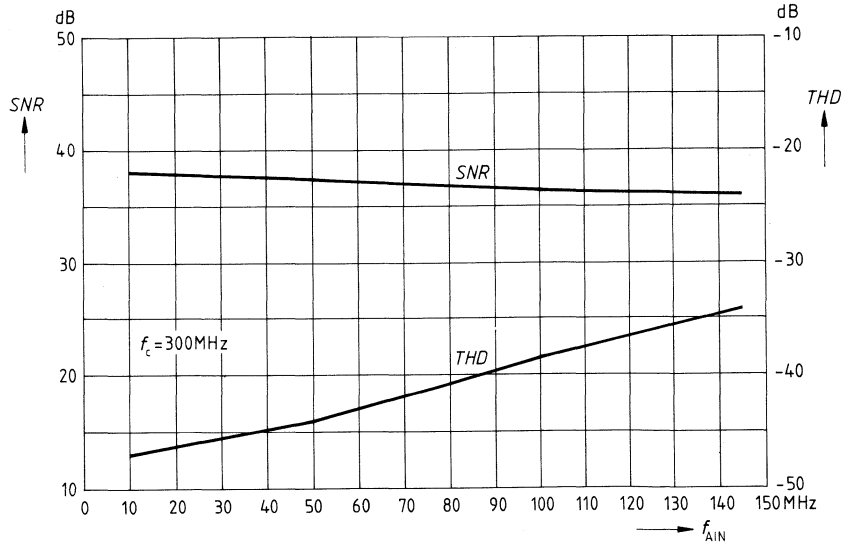
Output Delay (Transparent Mode) $t_{d,T}$ versus Junction Temperature



Effective Resolution b_{eff} versus Analog Frequency



Signal-to-Noise-Ratio *SNR* and Total Harmonic Distortion *THD* versus Analog Frequency



SIEMENS

8-Bit A/D Converter, 100 MHz

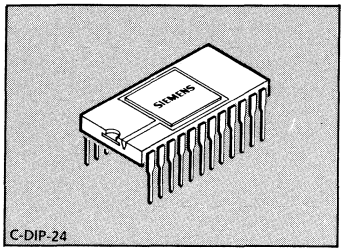
SDA 8010

Preliminary Data

Bipolar IC

Features

- 100 MHz min. strobe frequency
- 6.3 effective bits at 30-MHz input frequency
- Excellent large-signal bandwidth
- ±1/2 LSB max. linearity error
- Balanced input voltage range
- ECL-100-K compatible output data
- Lower power dissipation



Type	Ordering Code	Package
SDA 8010	Q67000-A2566	C-DIP-24

The SDA 8010 is an ultrafast A/D converter operating according to the parallel principle, with a resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. The device is capable of digitizing full scale (±1 V) analog signals with frequency components up to 50 MHz at a power consumption of 1.3 W. Due to the symmetric input voltage range it can be driven directly by a customary 50-Ω source.

Functional Description

The SDA 8010 is an ultrafast A/D converter operating according to the "flash" or parallel principle: a field of 255 comparators simultaneously compares the analog signal with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, delivered in the so-called thermometer code, is converted into binary representation by three encoding stages and is then available as a digital signal with ECL levels at the outputs **(see block diagram)**.

An individual comparator consists of a differential amplifier and a master/slave register stage. They are activated alternately by means of two strobe signals STR1 and STR2, thereby sampling the analog signal and holding the corresponding logical state. The sequence of the conversion process is given in the pulse diagram.

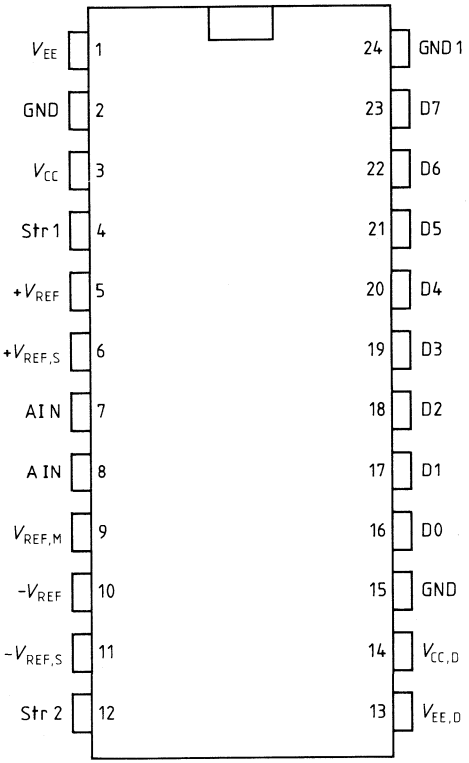
During the L phase of STR1, the analog signal is compared with the reference voltages. With the rising edge of STR1 the result of the comparison is passed into the first register stage and held there until the falling edge of STR 1. Towards the end of this hold period the signal is accepted into the second flipflop with the L phase of the second strobe STR2 and stored with the rising edge. After a delay $t_{d,\,Q}$ this data appears at the output and remains valid for the period $t_{v,\,Q}$.

Driving the converter's analog input is an easy task. Due to the ground-symmetrical input voltage range and the low input capacitance, the converter can be operated in a customary 50-Ω system without any preamplifiers or level shifters. Nevertheless, lower impedance driving would be a means for further improving the device's specified dynamic parameters. Two input pins AIN ensure low lead inductance. The internal reference voltages are generated by an on-chip resistor string. The potential at its end points, $+V_{REF}$ and $-V_{REF}$, respectively, determine the input voltage range which is resolved with an accuracy of 8 bits. Additional sense pins $+V_{REF,\,S}$ and $-V_{REF,\,S}$ allow compensation of voltage drops across parasitic resistances at the top and bottom of the string. The assignment of the digital output code to the input voltage is shown in the transfer characteristic. As no overflow function is provided, the output will remain at a value of 255 when the reference voltage range is exceeded.

Connection $V_{REF,\,M}$ only serves for RF decoupling; no additional adjustment is required for maintaining the specified accuracy of ±0.5 LSB.

The use of two supply systems, V_{CC} V_{EE} and $V_{CC,\,D}$, $V_{EE,\,D}$ and an additional ground line GND 1 for the output stages reduces the mutual influence of analog and digital signals. Additionally, the separate return of the analog signal ground line is recommended **(see test circuit).**

Figure 1
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{EE}	Neg. supply voltage, analog section
2	GND	Ground
3	V_{CC}	Pos. supply voltage, analog section
4	Str 1	Strobe signal 1
5 6	$+V_{REF}$ $+V_{REF, s}$	Pos. reference voltage Pos. reference voltage sense
7 8	A IN A IN	Analog input Analog input
9	$V_{REF, M}$	Center tap of voltage divider
10 11	$-V_{REF}$ $-V_{REF, s}$	Neg. reference voltage Neg. reference voltage sense
12	Str 2	Strobe signal 2
13 14	$V_{EE, D}$ $V_{CC, D}$	Neg. supply voltage, digital section Pos. supply voltage, digital section
15	GND	Ground
16 to 23	D0 to D7	Digital output signals
24	GND 1	Ground connection for output emitter follower

Figure 2
Block Diagram

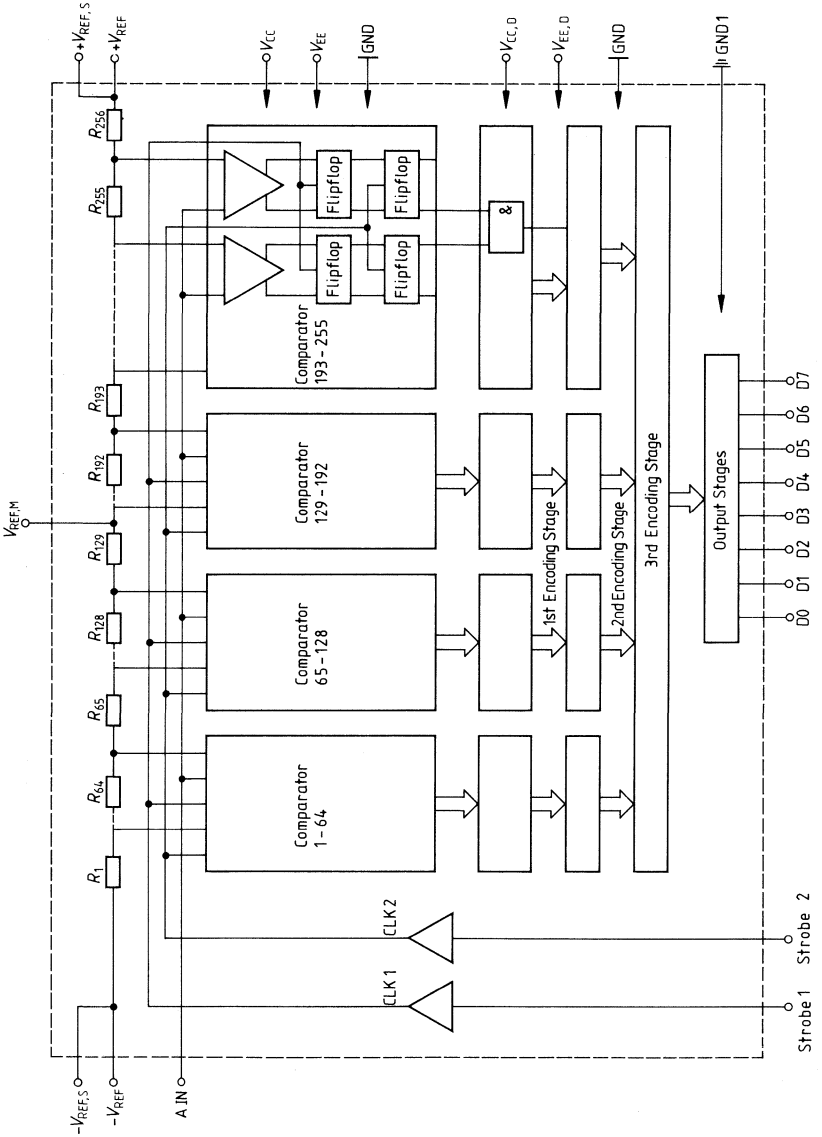
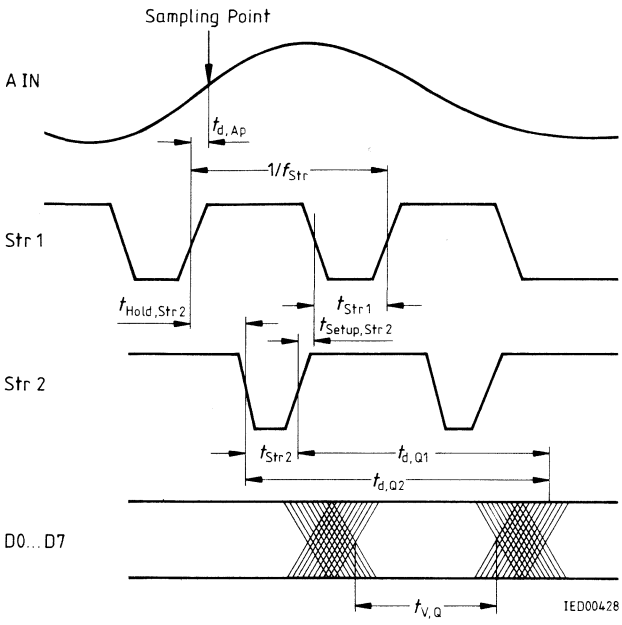


Figure 3
Pulse Diagram



Strobe Timing[1)]

	min.	typ.	Unit
$t_{Str\ 1}$	4	5	ns
$t_{Str\ 2}$	3	3.5	ns
$t_{Set\ up,\ Str\ 2}$	−2.0[2)]	−1.5[2)]	ns
$t_{Hold,\ Str\ 2}$	2	3	ns

1) This is recommended strobe setting for operation at 100 MHz. At lower strobe frequencies the timing becomes more and more uncritical. Below 75 MHz complementary strobe signals with a duty cycle of 50% may be used.

2) Negative values of $t_{Setup,\ Str\ 2}$ indicate that the rising edge of Str 2 should appear after the falling edge of Str 1.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Pos. supply voltage	V_{CC}, $V_{CC,\,D}$	−0.3	6.0	V
Neg. supply voltage	V_{EE}, $V_{EE\,D}$	−6.0	0.3	V
Reference voltage[1])	$+V_{REF}$, V_{REF}	−2.5	1.5	V
Analog input voltage	$V_{A\,IN}$	−2.5	1.5	V
Digital input voltage	$V_{Str\,1}$, $V_{Str\,2}$	−3.5	0	V
Output current	$I_{D0} \ldots I_{D7}$		20	mA
Junction temperature	T_j		150	°C
Ambient temperature (with heat sink)	T_A	−25	50	°C
Storage temperature	T_{stg}	−25	125	°C
Thermal resistance Junction – ambient (without heat sink)	$R_{th\,JA}$		50	K/W

Characteristics

V_{CC}, $V_{CC,\,D} = 5\ V \pm 5\%$, V_{EE}, V_{EE}, $V_{EE,\,D} = -4.5\ V \pm 5\%$, $T_j = 25\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Current Consumption					
Pos. supply current, analog	I_{CC}		95		mA
Pos. supply current, digital	$I_{CC,\,D}$		85		mA
Total pos. supply current	$I_{CC} + I_{CC,\,D}$		180	200	mA
Neg. supply current, analog	I_{EE}		70		mA
Neg. supply current, digital	$I_{EE,\,D}$		20		mA
Total neg. supply current	$I_{EE} + I_{EE,\,D}$		90	100	mA
Power dissipation	P_D		1.3	1.5	W
Permissible supply voltage difference	ΔV_{CC}, ΔV_{EE}			100	mV
Reference Inputs					
Reference voltages[1])	$+V_{REF}$, $-V_{REF}$	−2		1	V
Total reference resistance	R_{REF}	105	150	190	Ω
Temperature coefficient of reference resistor	TC		3×10^{-3}		1/K
Analog Input					
Voltage range	V	−2		1	V
Input current[2]) $V_{AIN} \geq +V_{REF}$	I_I	150		700	µA
$V_{AIN} \leq -V_{REF}$	I_I			1	µA
Input capacitance $V_{AIN} \geq +V_{REF}$	C_{AIN}		45		pF
$V_{AIN} \leq -V_{REF}$	C_{AIN}		55		pF

For comments see two pages hereafter.

Characteristics (cont'd)

V_{CC}, $V_{CC,\,D}$ = 5 V ± 5%, V_{EE}, $V_{EE,\,D}$ = −4.5 V ± 5%; T_j = 25 °C to 125 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Strobe Inputs					
H-input voltage	V_{IH}	−1.165			V
L-input voltage	V_{IL}			−1.475	V
Max. strobe frequency	f_{Str}	100	125		MHz
H-input current $V_{Str} = V_{IH}$	I_{IH}	2		30	µA
L-input current $V_{Str} = V_{IL}$	I_{IL}			40	nA
Aperture delay	$t_{d,\,ap}$		1		ns
Aperture jitter	t_{jit}		15		ps
Data Outputs					
H-output voltage (100-Ω resistor to −2 V)	V_{QH}	−1.025		−0.880	V
L-output voltage (100-Ω resistor to −2 V)	V_{QL}	−1.810		−1.620	V
Signal transition time[3]	$t_{d,\,Q1}$			10.5	ns
	$t_{d,\,Q2}$			14	ns
Time of valid output data[4] f_{Str} = 100 MHz	$t_{V,\,Q}$	4	6		ns
Conversion Characteristics					
Static Nonlinearity[5]					
Integral nonlinearity ΔV_{REF} = 1.8 V	*I NL*			0.5	LSB
Differential nonlinearity ΔV_{REF} = 1.8 V	*D NL*		0.5	0.6	LSB
Dynamic Performance[6]					
Large signal bandwidth	$f_{3\,dB}$	80			MHz
Signal-to-noise ratio					
f_{an} = 30 MHz	*SNR*	40	43		dB
f_{an} = 45 MHz	*SNR*		35		dB
Total harmonic distortion					
f_{an} = 30 MHz	*THD*		−43		dB
f_{an} = 45 MHz	*THD*		−30		dB
Effective bits					
f_{an} = 1 MHz	N_{eff}		7.4		bit
f_{an} = 30 MHz	N_{eff}	6.0	6.3		bit
f_{an} = 45 MHz	N_{eff}		4.5		bit

For comments see next page.

Comments

1) $+V_{REF}$ must always be more positive than $-V_{REF}$.
2) The input current is linearly dependent on the input voltage.
3) Delay from the rising edge ($t_{d, Q1}$) or falling edge ($t_{d, Q2}$) of Str2 to the beginning of validity of the associated output data.
4) Time interval, during which the conversion of a 30 MHz/2 V_{pp} signal at 100 MHz sampling rate yields an *SNR* of more than 40 dB.
5) The actual transfer characteristic is measured by means of the servo loop principle at both low sampling rates (100 kHz) and slow strobe edges (> 500 ns).
6) Dynamic measurements are performed at 100 MHz sampling rate using the typical strobe timing. All specified parameters are derived from the FET of the converter's response to a full scale (2 V_{pp}) sine wave input. The analog source impedance is 25 Ω (50-Ω line with 50-Ω termination). The test circuit is shown in **figure 5.**

Figure 4
Transfer Characteristic and Truth Table

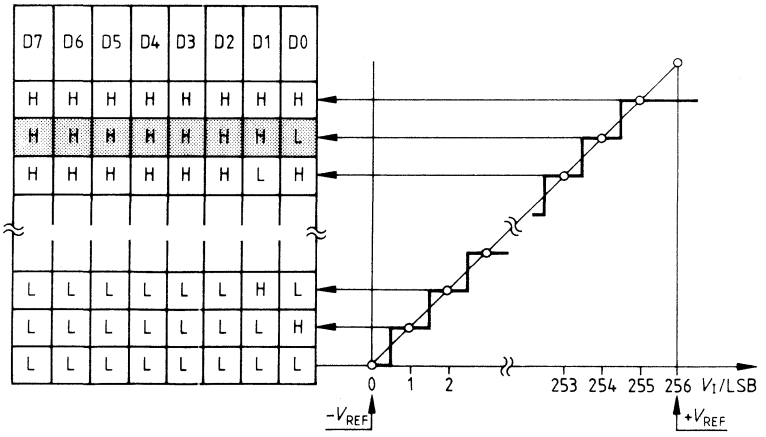


Figure 5
Test Circuit

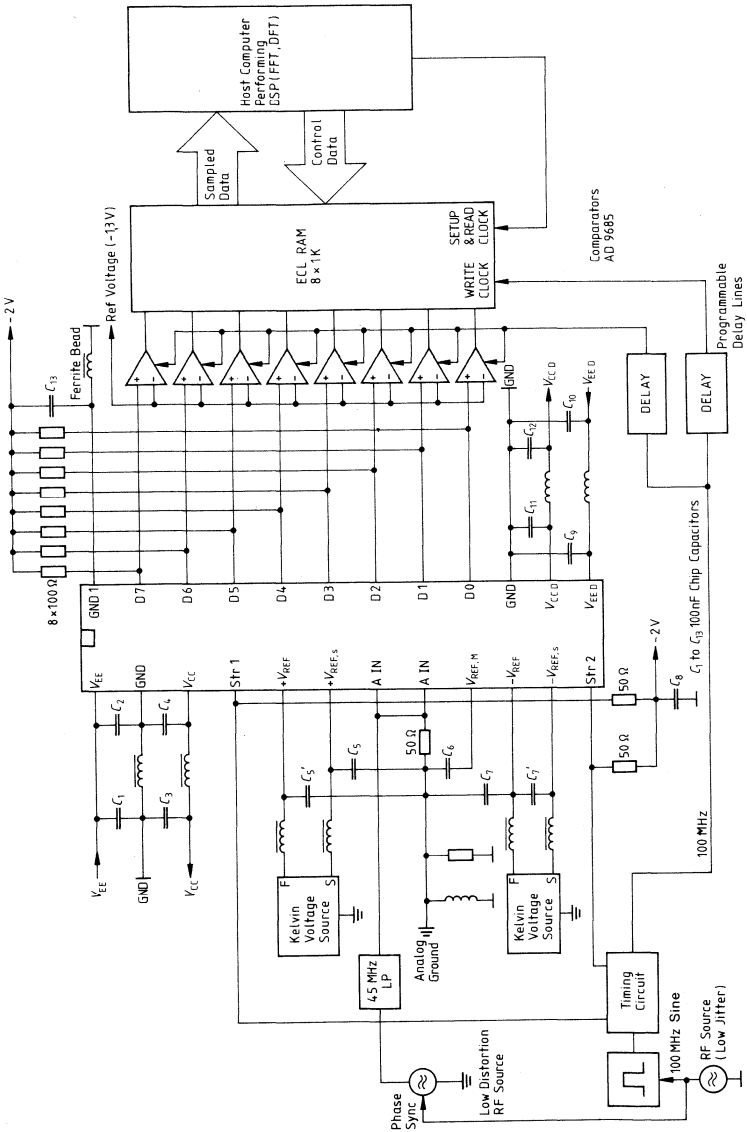


Figure 6
Analog Input Capacitance versus Input Bias Voltage
($+V_{REF} = 1$ V; $-V_{REF} = -1$ V)

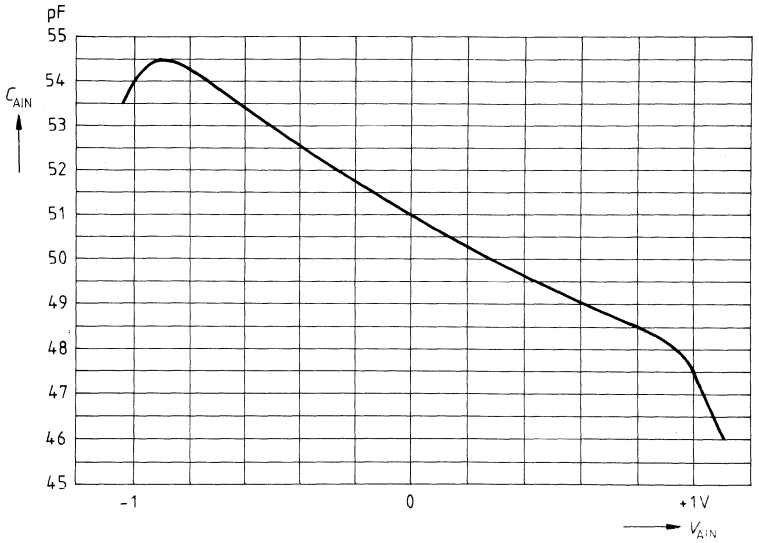


Figure 7
Signal Transition Time $t_{d,Q1}$ and Valid Data Range $t_{V,Q}$ versus Junction Temperature

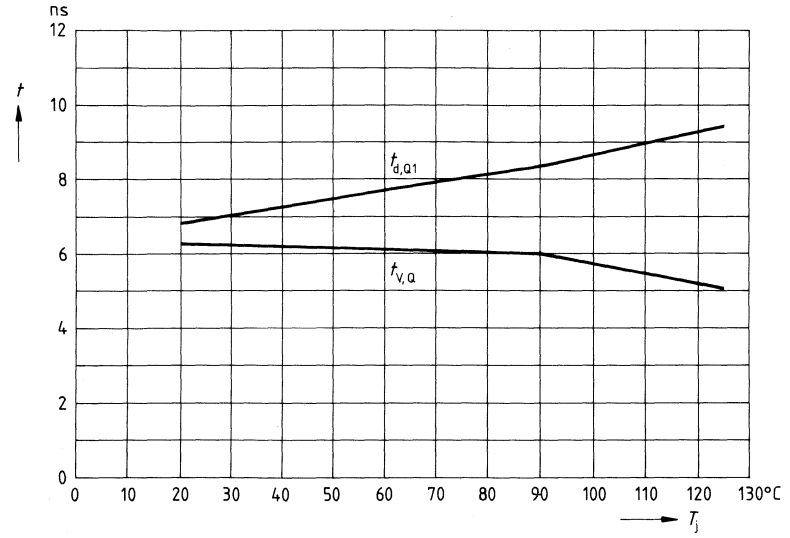


Figure 8
Amplitude Response versus Analog Frequency
a) including voltage drop across source impedance (25 Ω)
b) without voltage drop across source impedance (25 Ω)

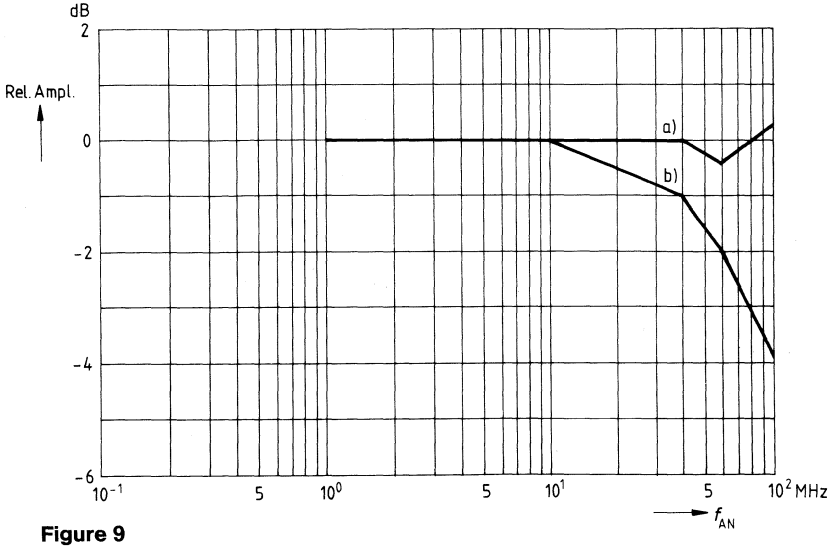


Figure 9
Signal-to-Noise-Ratio *SNR* and Harmonic Distortion *THD* versus Analog Frequency

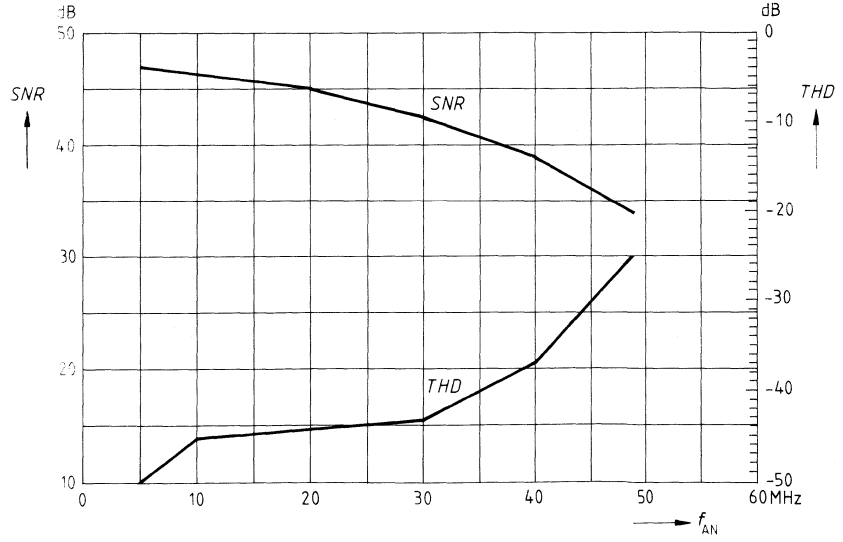
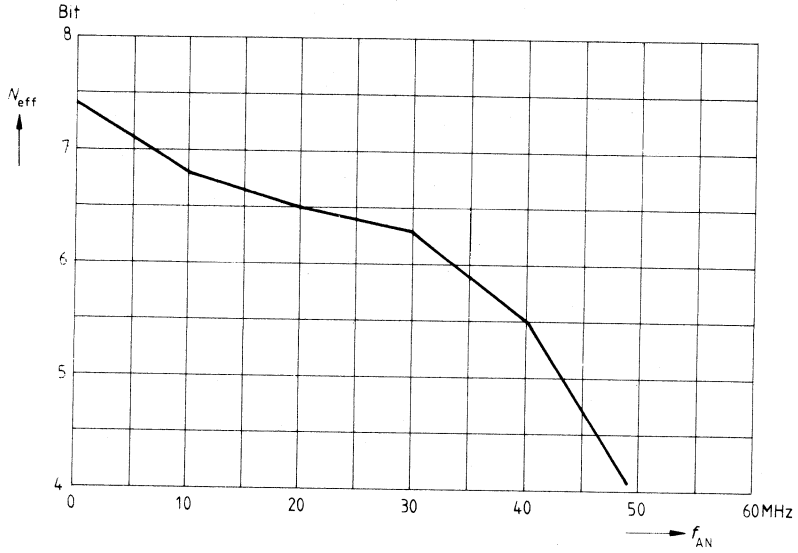


Figure 10
Effective Resolution N_{eff} versus Analog Frequency



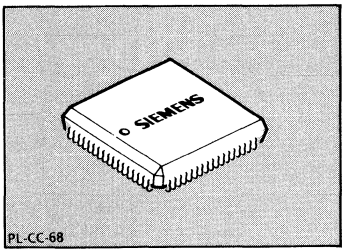
SIEMENS

DASR – Data Acquisition Shift Register for HSDA Systems

SDA 8020 N

Preliminary Data

Bipolar IC



Features

- 4 x 8-bit shift register
- ECL-serial or TTL-parallel loading
- 125 MHz shift clock frequency typically
- Latches for parallel TTL input/output data
- TTL-compatible control pins
- Cascadable, thereby automatically decreasing the TTL clock frequency
- Two clock outputs, TTL CLK and $\overline{W}$, for easy handling
- Interface between high speed ECL and customary TTL circuits
- Power consumption typically 1.5 W

6

Type	Ordering Code	Package
SDA 8020 N	Q67000-A8127	PL-CC-68 (SMD)

The DASR SDA 8020 N with ECL signal compatible inputs is capable of **DEMULTIPLEXING** an 8-bit wide data stream with a clock rate of up to 100 MHz into four parallel 8-bit TTL data channels with a clock rate one quarter of the serial clock. In a second operating mode a **MULTIPLEX** function combining four 8-bit wide TTL data channels into one 8-bit ECL compatible channel with up to 100 MHz clock rate is provided.

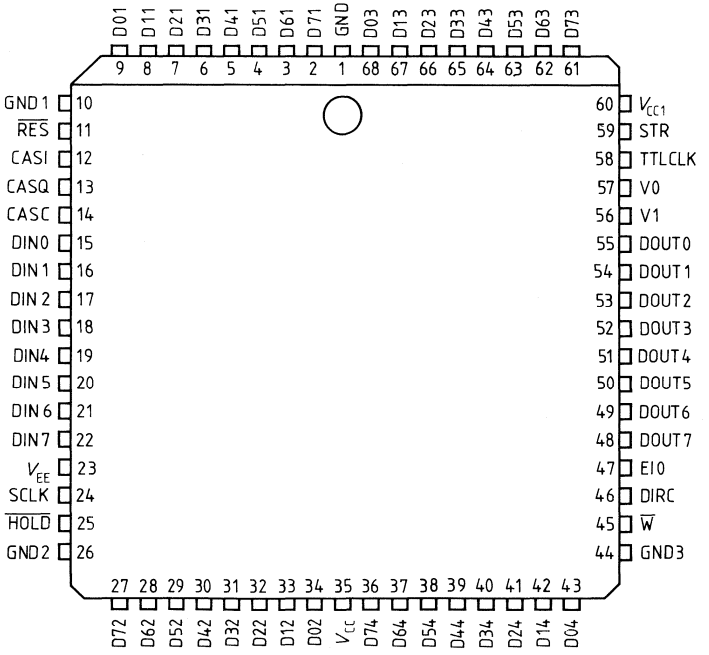
Circuit Description

The DASR contains eight parallel 4-bit shift registers, each of them with two internally cascaded level-operated input/output latches. The device has 8 ECL-compatible serial inputs and outputs and 32 parallel TTL-compatible common inputs/outputs. Beside the data inputs and outputs the device has 7 mode control inputs and provides 2 clock signals which especially support the use of the DASR together with fast static MOS RAMs in a data acquisition system. All these inputs and outputs are TTL-compatible.

The clock section comprises a 1-bit x 4 shift register whose output (CASO) is fed back to its input (CASI) via the external clock loop. If the cascade control input (CASC) is set to H, a single pulse is written into the first shift register cell. When $\overline{\text{HOLD}}$ is released this single clock pulse is moved around the clock loop and all timing signals are derived from this pulse.

The DASR is intended primarily as an interface between a high-speed A/D or D/A converter and the memories in a data acquisition or waveform-generating system. Further applications are high-speed logic analyzers and digital word generators.

Figure 1
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Type	Symbol	I/O	Function
1		GND		TTL data ground
9-2 34-27 43-36 68-61	TTL TTL TTL TTL	D01..D71 D02..D72 D04..D74 D03..D73	I/O I/O I/O I/O	These are the 32 parallel TTL inputs or outputs (dependent on the DIRC input) of the single shift register cells. The fanout of these outputs is 2 TTL loads.
10		GND1		ECL ground
11	TTL	$\overline{RES}$	I	By activating this input (active low) all 32 shift register cells are cleared and the clock generator is reset (DOUT 0..7 = low, TTLCLK = low, $\overline{W}$ = high)
12, 13	–	CASI, CASO	I/O	Cascading in, Cascading out **(see figure 4)** These two pins control in connection with the cascading control input the TTL clock rate and internal strobe timing. Used only to establish the clock loop. They don't provide ECL compatibility.
14	TTL	CASC	I	Cascading control The required logic level at this input depends on the cascading configuration **(see chapter "cascading" and figure 4).** A single chip configuration requires a High level.
15-22	ECL	DIN 0...7	I	ECL data input byte
23		V_{EE}		Negative supply voltage; ECL section
24	ECL	SCLK	I	The single shift register cells are clocked by this signal. Data pending at DIN 0...7 are transferred with the falling clock edge.
25	TTL	$\overline{HOLD}$	I	A logic low at the $\overline{HOLD}$ input inhibits the shift clock and sets the 32 parallel I/Os into the high-impedance state. The register is inactive.
26		GND2		TTL ground; clock and control section
35		V_{CC}		Positive supply voltage; TTL data section
44		GND 3		Ground for ECL output emitter followers
58	TTL	TTLCLK	O	The frequency of the TTL clock in single chip operation is 1/4 of the shift clock frequency. In a cascaded configuration the TTL clock frequency is automatically decreased.

Pin Definitions and Functions

Pin	Type	Symbol	I/O	Function
46	TTL	DIRC	I	A logic high on the DIRC configurates the DASR for parallel in/serial out (multiplexing, parallel loading), and a logic low for serial in/parallel out (demultiplexing, serial loading) operation.
47	ECL	EIO	I/O	Enables the internal data transfer from the latches to the shift registers in multiplexing mode. In this mode the EIOs provide internal timing information to all cascaded DASRs. This pin must be connected to −2 V via 1 kΩ resistor **(see figure 4).** In demultiplexing mode the EIO pin has no influence on internal timing and may be left open.
55-48	ECL	DOUT 0...7	O	ECL data output byte. Data are transferred to the output on the falling SCLK edge.
56, 57	TTL	V1, V0	I	With V0, V1 one of four possible delay times of the $\overline{W}$ signal is selected.
45	TTL	$\overline{W}$	O	The $\overline{W}$ output has the same frequency as the TTLCLK but a different duty cycle (1/4 in single-chip operation). It may be used as the write or chip select signal for high speed MOS SRAMs which are placed at the parallel inputs/outputs. It can be delayed in multiples of shift clock periods programmable by V0, V1 (see programming table for V0, V1 below).
59	TTL	STR	I	The four 8-bit data words are latched in the first input/second output latch by the Strobe. A high strobe level makes these latches transparent.
60		V_{CC1}		Positive supply voltage; TTL clocks and control signal section.

Programming table for V0, V1

V0	V1	Delay of $\overline{W}$
0	0	0 SCLK period
0	1	1 SCLK period
1	0	2 SCLK periods
1	1	3 SCLK periods

Figure 2
Functional Block Diagram

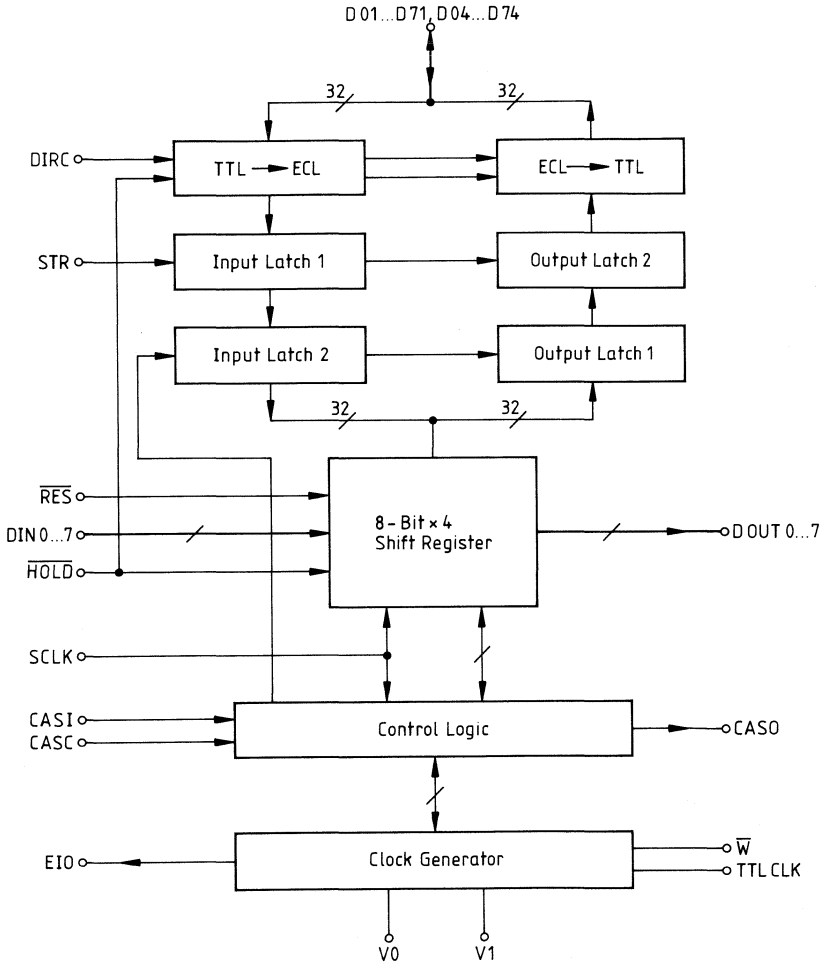
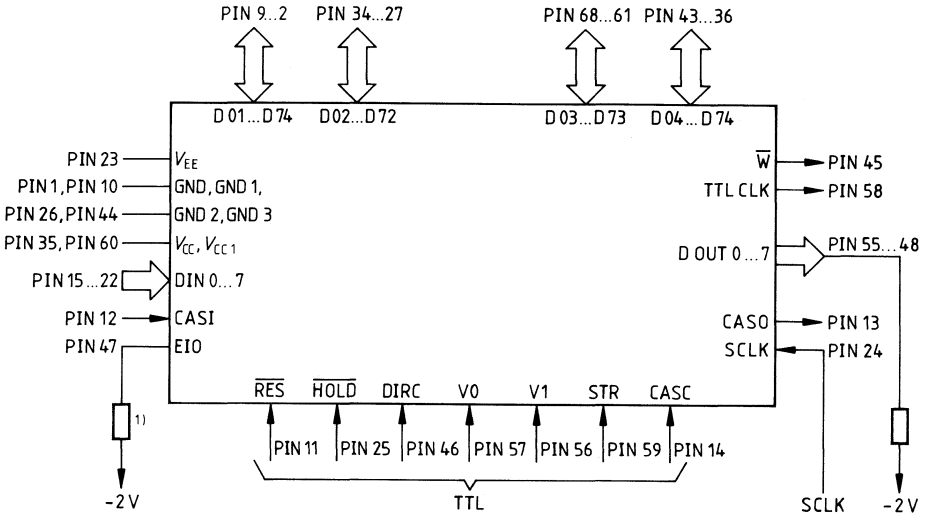


Figure 3
Basic Configuration



1) Only in multiplexing mode

Mode of Operation

The DASR has two distinct modes of operation, selected by the DIRC. To avoid excessive power dissipation those circuit parts which are unused in one mode are switched off.

1 **Serial IN/Parallel OUT (Figure 8)**

After activating the DASR by asynchronous $\overline{RES}$ and $\overline{HOLD}$ **(see figure 5** for recommended $\overline{HOLD}$, $\overline{RES}$ timing), the 8-bit wide ECL data words (present at DIN0...DIN7) are loaded synchronously into the register by the falling SCLK edge. Shortly after every fourth trailing SCLK edge, the contents of the single shift register cells are strobed into the first output latch by an internally created clock. These four data bytes appear at the outputs (D01...D71,...D04...D74) after they are passed to the second output latch by the external STR signal. This latch can also be made transparent by setting STR to H or leaving it unconnected. The first acquired data byte appears at D04...D74, the second at D03...D73, the third at D02...D72 and the fourth at D01...D71. Due to the inherent skew of the latches, a falling edge of the external STR must not appear during a short interval ($t_{H,\ STR,\ D}$) after every fourth SCLK period (because output latch 1 has only just been made transparent; **see figure 8**).

An acquisition cycle is completed by a negative $\overline{HOLD}$ level, which is internally synchronized first with the leading TTLCLK edge and secondly with the leading $\overline{W}$ edge. This double synchronization simplifies stopping the acquisition on a well-defined sample **(see Application Circuit, figure 12)**.

There are a few TTLCLK waveforms possible at the end of an operation cycle depending on the delay of $\overline{W}$ **(see figure 5).** $\overline{W}$ remains high after stopping the DASR. When inhibitting SCLK by $\overline{HOLD}$ the TTL data outputs change to the high-impedance state.

2 **Parallel IN/Serial OUT (Figure 9)**

Synchronous parallel loading is accomplished by applying four 8-bit TTL data words at D01...D74 and taking the STR high.

Every fourth SCLK period, beginning with the 6th falling edge of SCLK after starting operation with a high $\overline{HOLD}$, the second input latch is transparent for one SCLK cycle. With the next falling edge of SCLK the data are written into the shift register cells. The first valid data at DOUT do not appear before the 8th falling edge of SCLK from the beginning onwards. Those data pending at D04...D74 are shifted out first and those at D01...D71 last within a TTLCLK cycle. To obtain defined starting conditions at DOUT, DIN should be set to logic low. The setup and hold times $t_{S,\ D,\ SCLK}$, $t_{H,\ D,\ SCLK}$ apply only if the first input latch is made transparent by setting STR to H.

In either operating mode the first rising edge of the TTLCLK appears two falling edges of shift clock after activating the DASR. The first $\overline{W}$ pulse with a duration of one SCLK cycle and a delay programmed by V0 and V1 is provided after the third falling edge of SCLK.

6

Cascading

The ability to cascade the DASR enables lower TTL data rates combined with the advantage of a 100 MHz shift clock. By cascading the DASR the CASO of one device must be connected with the CASI of the next. This clock loop is closed by connecting the CASO of the last DASR with the CASI of the first one. Furthermore, the cascading control input (CASC) of one DASR only is set high **(see figure 4)**. The position of the DASR with a high CASC input determines the moment for the internal strobes to transfer data to the second input latch and to the single shift register cells in parallel in/serial out mode **(see figure 7).** The first internal strobes appear at the same time as in single chip operation and their period depends on the length of the shift register cascade. In a system with cascaded DASRs, the first edge of $\overline{W}$ or TTLCLK is to transfer at that DASR with CASC = H. The $\overline{W}$ and TTLCLK signals of the other SDA 8020s are provided in the same succession as if they were interconnected via CASI, CASO.

The time delay between the rising edges of the TTLCLK signals is four SCLK periods. In parallel in/serial out mode all EIOs must be tied together and connected to −2 V via a 1 kΩ-resistor. In serial in/parallel out mode the position of the DASR with a high CASC is unimportant for internal timing. In this mode the period of the internal strobe (for output latch 1) is non increased. So the data of the shift registers are strobed to the output latch 1 every fourth SCLK period. To obtain valid TTL output data over the whole TTLCLK period an STR pulse with a duration of a maximum of 4 SCLK periods must be used, e.g.: $\overline{W}$ **(see figure 6).** The signals at the EIOs are for internal use only **(see figure 4).**

The TTL clock high phase of the DASRs with a low CASC is doubled. When cascading the DASR the $\overline{W}$ signal can be delayed not only in four steps as in the single-chip configuration but over the whole TTL clock period by using the $\overline{W}$ output of the appropriate chip.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Positive supply voltage	V_{CC}	−0.3	6.0	V
Negative supply voltage	V_{EE}	−6.0	0.3	V
ECL input voltage		−3.5	0	V
ECL output voltage			1	V
TTL input and output voltage		−0.6	5.5	V
Tristate current into D01...D74			1	mA
Output current at $\overline{W}$		−40[1]	40[2]	mA
Output current at D01...D74		−10[1]	10[2]	mA
Output current at TTLCLK		−20[1]	20[2]	mA
Output current at DOUT 0...7		−20	0	mA
Output current at EIO		−10	0	mA
Junction temperature	T_j		150	°C
Ambient temperature	T_A	−25	70	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance				
system – ambient	$R_{th\ SA}$		30	K/W
system – package	$R_{th\ SP}$		15	K/W

[1]) High-State
[2]) Low-State

Electrical Characteristics

$T_A = -25\,°C$ to $70\,°C$, $V_{CC} = 5\ V \pm 5\%$, $V_{EE} = -4.5\ V \pm 5\%$, $|V_{CC} - V_{CC\,1}| < 0.5\ V$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions	Test Circuit
Power Supply							
Positive supply current	I_{CC}		65	80	mA		
Negative supply current	I_{EE}		240	265	mA		
TTL Pins							
H-input voltage	V_{IHT}	2			V		
L-input voltage	V_{ILT}			0.8	V		
H-input current	I_{IHT}			30	µA	V_{CC} = max; V_I = 2.4 V	
L-input current	I_{ILT}			−1.6	mA	V_{CC} = max; V_I = 0.5 V	
H-output voltage	V_{QHT}	2.4			V	V_{CC} = min; I_{IQH} = −800 µA	a
L-output voltage	V_{QLT}			0.5	V	V_{CC} = min; I_{QL} = 3.2 mA	a
Off-state output current	I_{QZLT}			−50	µA	V_{CC} = max; V_Q = 0.5 V	
	I_{QZHT}			50	µA	V_{CC} = max; V_Q = 2.4 V	
ECL Pins							
H-input voltage	V_{IHE}	−1.165		−0.88	V		
L-input voltage	V_{ILE}	−1.81		−1.475	V		
H-output voltage	V_{QHE}	−1.025		−0.88	V		c
L-output voltage	V_{QLE}	−1.81		−1.62	V		c

Electrical Characteristics

$T_A = -25\,°C$ to $70\,°C$, $V_{CC} = 5\ V \pm 5\%$, $V_{EE} = -4.5\ V \pm 5\%$, $| V_{CC} - V_{CC\,1} | < 0.5\ V$

Parameter	Symbol	Limit Values			Unit	Test Conditions	Test Circuit
		min.	typ.	max.			
CASI, CASO							
H-input voltage	V_{IHC}	−1.0		−0.65	V		
L-input voltage	V_{ILC}	−1.6		−1.35	V		
H-output voltage	V_{QHC}		−0.9		V		
L-output voltage	V_{QLC}		−1.55		V		
Maximum load capacity at CASO	C_{CASO}	5			pF		

Timing Characteristics

$T_A = -25\,°C$ to $70\,°C$, $V_{CC} = 5\ V \pm 5\%$, $V_{EE} = -4.5\ V \pm 5\%$, $| V_{CC} - V_{CC\,1} | < 0.5\ V$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Setup time DIN 0...7 to SLCK	$t_{S,\,DIN}$	0.5			ns
Hold time DIN 0...7 to SCLK	$t_{H,\,DIN}$	2.0			ns
Setup time D01...D74 to STR	$t_{S,\,D}$ [1]	8.0			ns
Hold time D01...D74 to STR	$t_{H,\,D}$ [1]	0			ns
Setup time Control to $\overline{HOLD}$	$t_{S,\,CONT}$ [2]	30	7		ns
Hold time Control to $\overline{HOLD}$	$t_{H,\,CONT}$ [2] [6]	20	0		ns
min. Setup time STR to SCLK	$t_{S,\,STR,\,D}$ [1] [3]		−4.5		ns
min. Hold time STR to SCLK	$t_{H,\,STR,\,D}$ [1] [3]		6.5		ns
min. Setup time $\overline{HOLD}$ to SCLK	$t_{S,\,\overline{HOLD},\,S}$		14	20	ns
Setup time $\overline{HOLD}$ to TTL CLK	$t_{S,\,\overline{HOLD},\,T}$	20			ns
Setup time $\overline{RES}$ to $\overline{HOLD}$	$t_{S,\,\overline{RES}}$	20			ns
min. Setup time STR to SCLK	$t_{S,\,STR,\,SLCK}$ [4] [7]		3		ns
min. Hold time STR to SCLK	$t_{H,\,STR,\,SCLK}$ [4] [7]		0		ns
min. Setup time D01...D74 to SCLK	$t_{S,\,D,\,SCLK}$ [5]		5		ns
min. Hold time D01...D74 to SCLK	$t_{H,\,D,\,SCLK}$ [5]		1		ns

For notes see next page.

Timing Characteristics (cont'd)

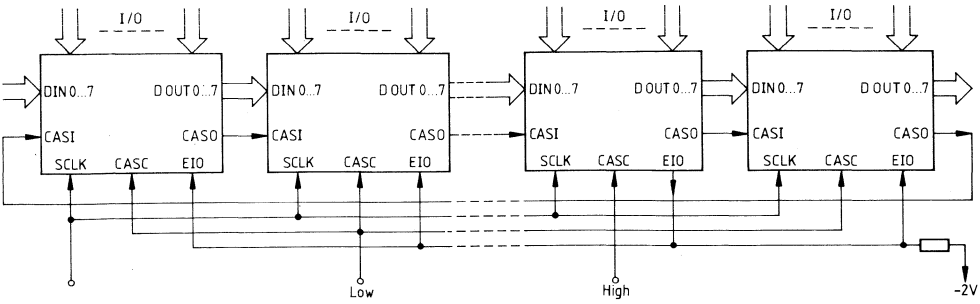
Parameter	Symbol	Limit Values			Unit	Test Conditions	Test Circuit
		min.	typ.	max.			
Delay SCLK – D01...D74	$t_{D,\ SCLK,\ D}$		24	27	ns	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a
Delay STR – D01...D74	$t_{d,\ D}$	16.5	21	23	ns	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a
Delay DIRC, $\overline{\text{HOLD}}$- D01...D74	t_{ZL} t_{ZH}		40	100	ns	$R_{L1} = 1200\ \Omega$, $C_L = 15$ pF	b
Delay DIRC, $\overline{\text{HOLD}}$- D01...D74	t_{HZ}[6], t_{LZ}[6]		25	100	ns	$R_{L1} = 1200\ \Omega$, $C_L = 15$ pF	b
Delay SCLK – $\overline{W}$	$t_{d\ HL\overline{W}}$		9.5	13	ns	$R_L = 1200\ \Omega$, $C_L = 40$ pF	a
Delay SCLK – $\overline{W}$	$t_{d\ LH\overline{W}}$		9	11	ns	$R_L = 1200\ \Omega$, $C_L = 40$ pF	a
Delay SCLK – TTLCLK	$t_{d\ LH,\ TTLCLK}$		11	13	ns	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a
Delay SCLK – TTLCLK	$t_{d\ HL,\ TTLCLK}$		12.5	15	ns	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a
Delay SCLK – DOUT 0...7	$t_{d,\ DOUT}$		5	7.5	ns		c
Delay $\overline{\text{RES}}$ – DOUT 0...7	t_d		15		ns		c
Pulse width of SCLK	t_W	4			ns		
Pulse width of $\overline{\text{RES}}$	$t_{W,\ \overline{\text{RES}}}$	30			ns		
Min. pulse width of STR	t_{STR}		6		ns		
Max. SCLK frequency	f_{SCLK}	100	125		MHz		

Notes

1) Only every 4th SCLK period from the 4th trailing edge onwards
2) Control: Signals DIRC, V0, V1, CASC
3) Doesn't apply if output latch 2 is transparent
4) Doesn't apply if input latch 1 is transparent
5) Only every 4th SCLK period and if input latch 1 is transparent
6) Refers to $\overline{\text{HOLD}}$ after internal synchronization
7) Only every 4th SCLK period from the 7th trailing edge onwards

Figure 4
Cascading Block Diagram

a) Parallel in / serial out



b) Serial in / parallel out

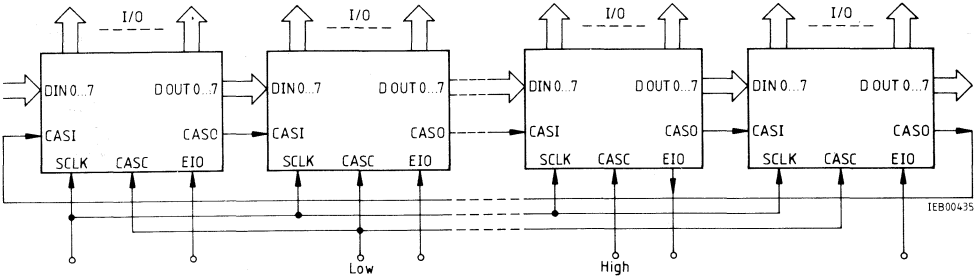


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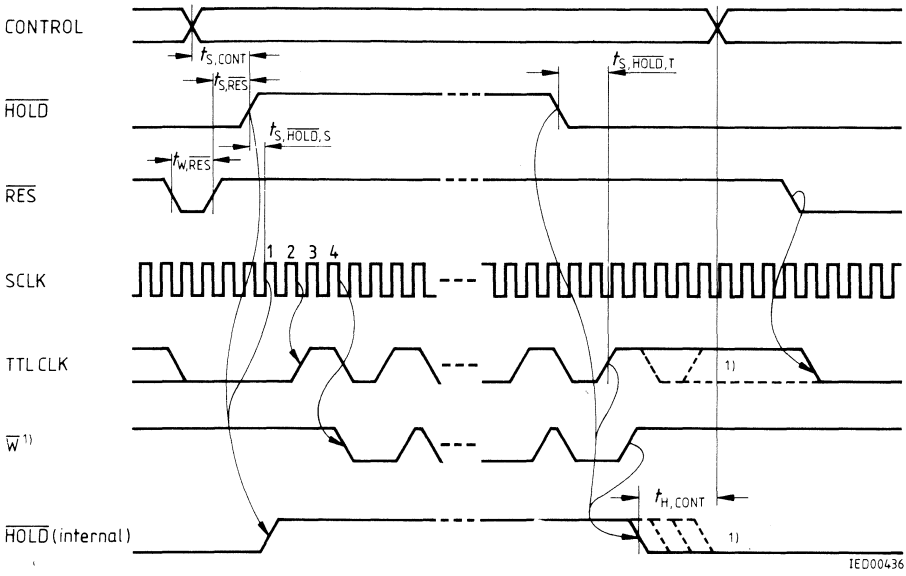
Figure 5
$\overline{\text{HOLD}}/\overline{\text{RES}}$ Timing



1) Dependent on the Programmed Delay of $\overline{W}$; Solid Line Shows Conditions for V0 = 0, V1 = 0

Figure 6a
Cascading of Two DASRs – Serial IN/Parallel OUT

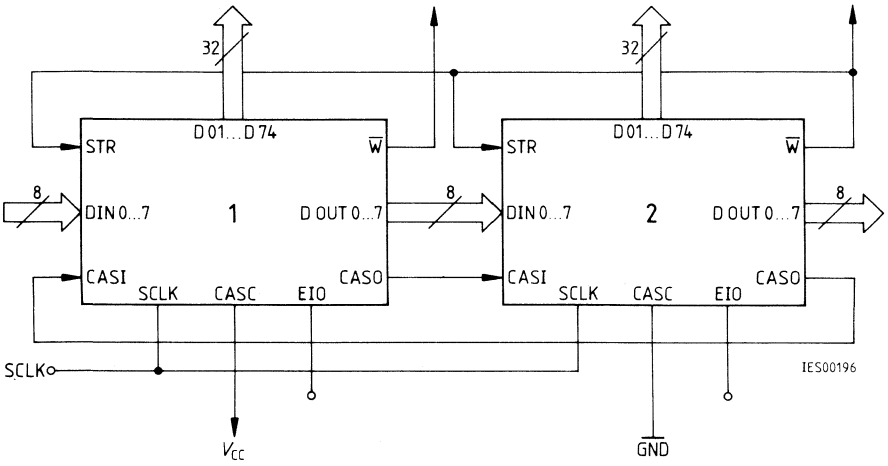
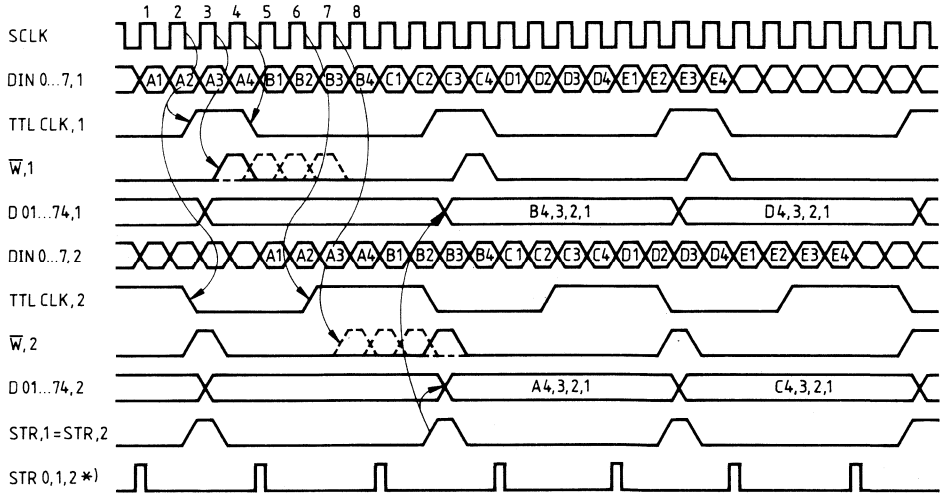


Figure 6b
Cascading of Two DASRs – Serial IN/Parallel OUT



*) Controls output latch 1 of either DASR

Figure 7a
Cascading of Two DASRs – Parallel IN/Serial OUT

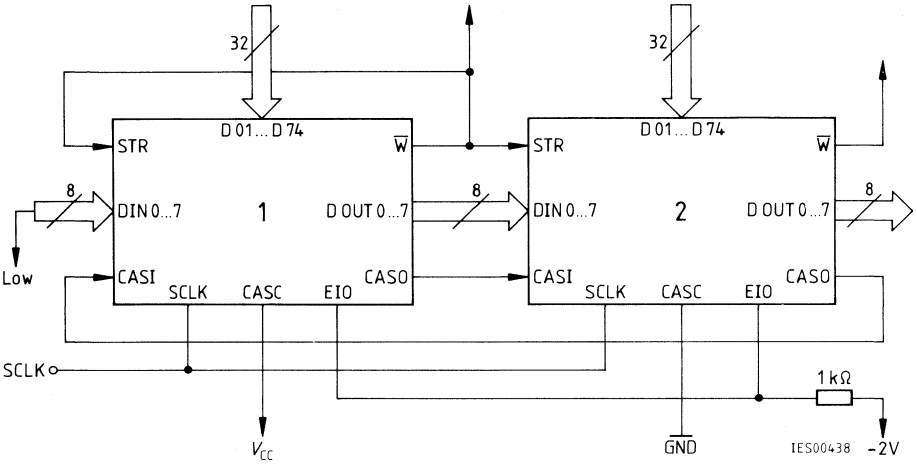
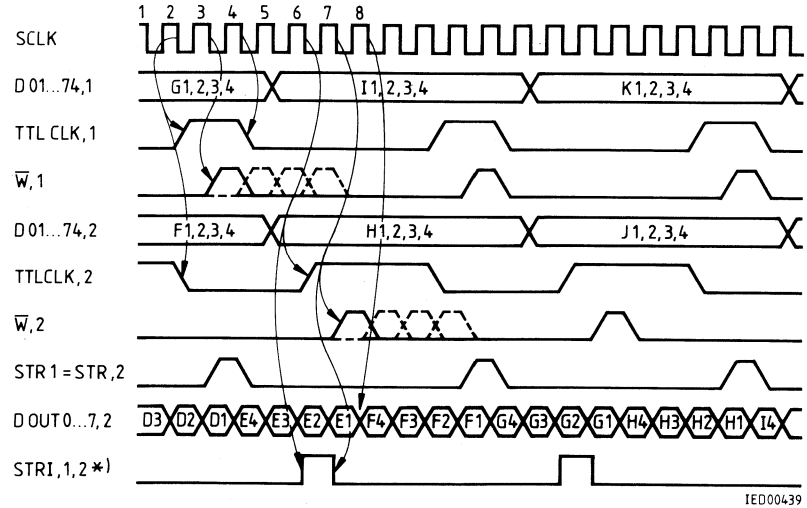


Figure 7b
Cascading of Two DASRs – Parallel IN/Serial OUT



*) Controls input latch 2 of either DASR

Figure 8
Timing Relations for Serial IN/Parallel OUT Operation

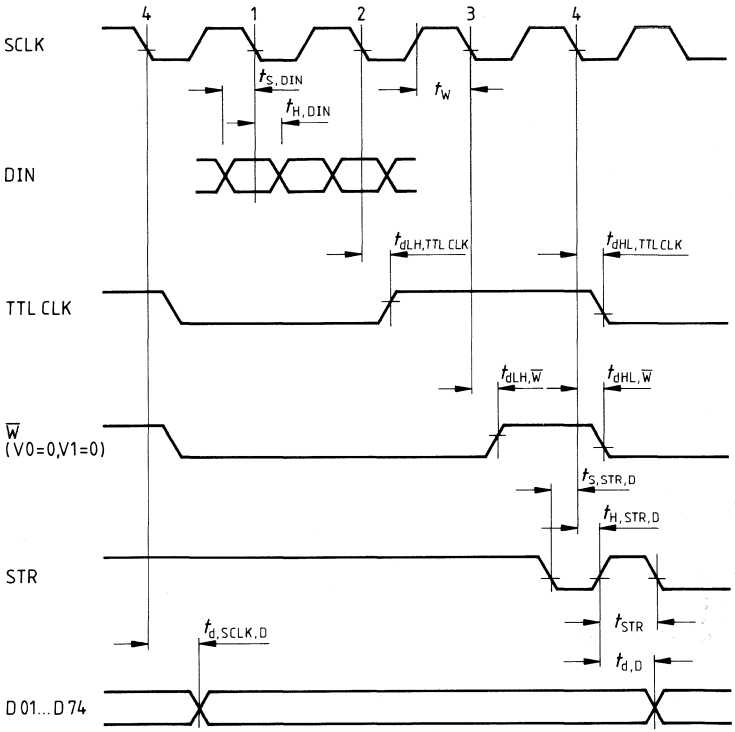


Figure 9
Timing Relations for Parallel IN/Serial OUT Operation

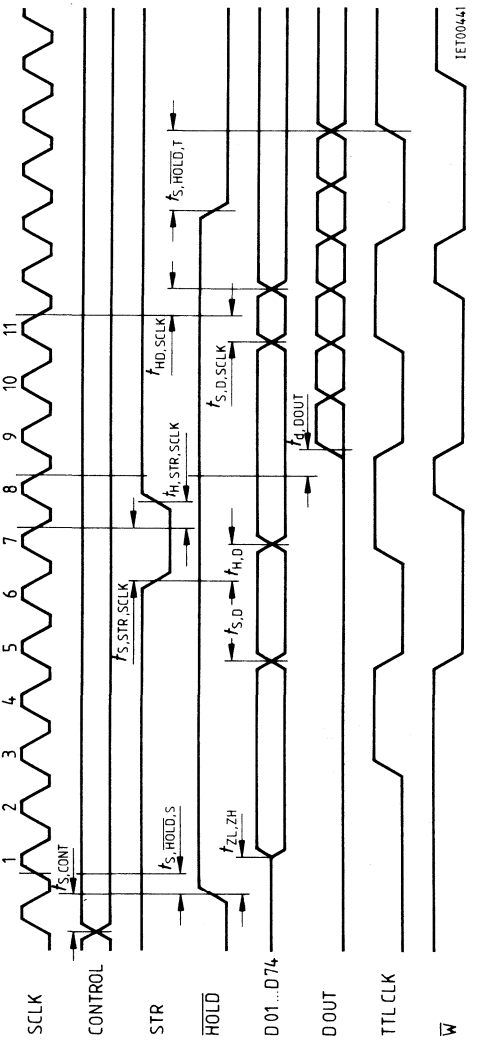


Figure 10
Test Circuits

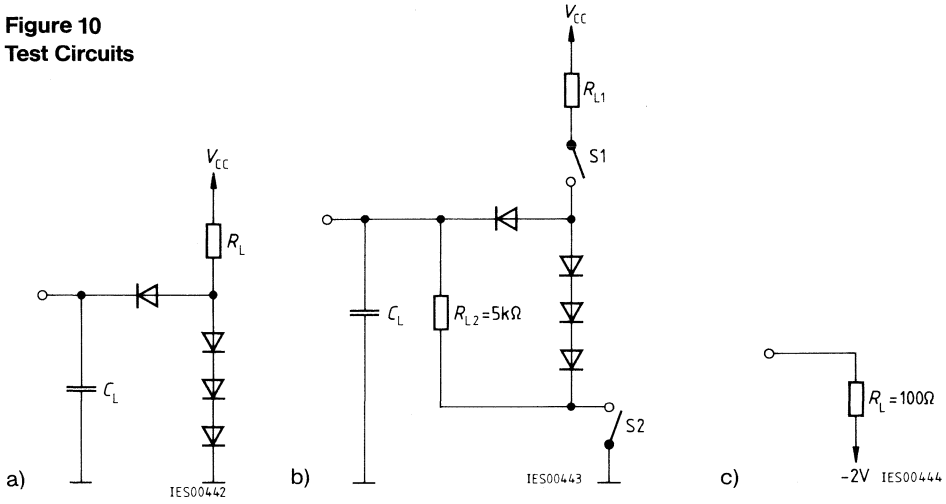
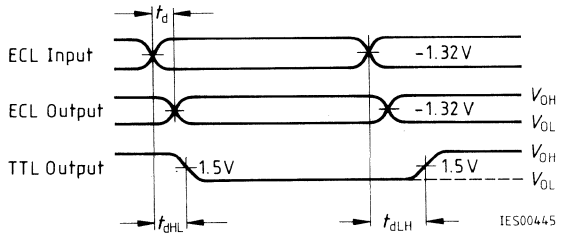
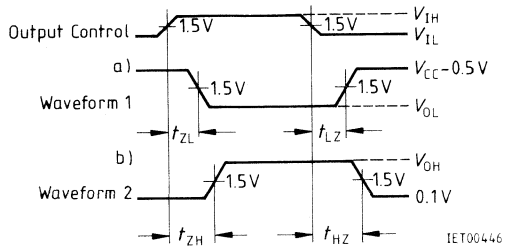


Figure 11
Testing Points



Enable and disable times (Tristate outputs)



a) for an output with internal conditions such that the output is low except when disabled by the output control

b) for an output with internal conditions such that the output is high except when disabled by the output control

6

Figure 12
Application Circuit
Data Acquisition System

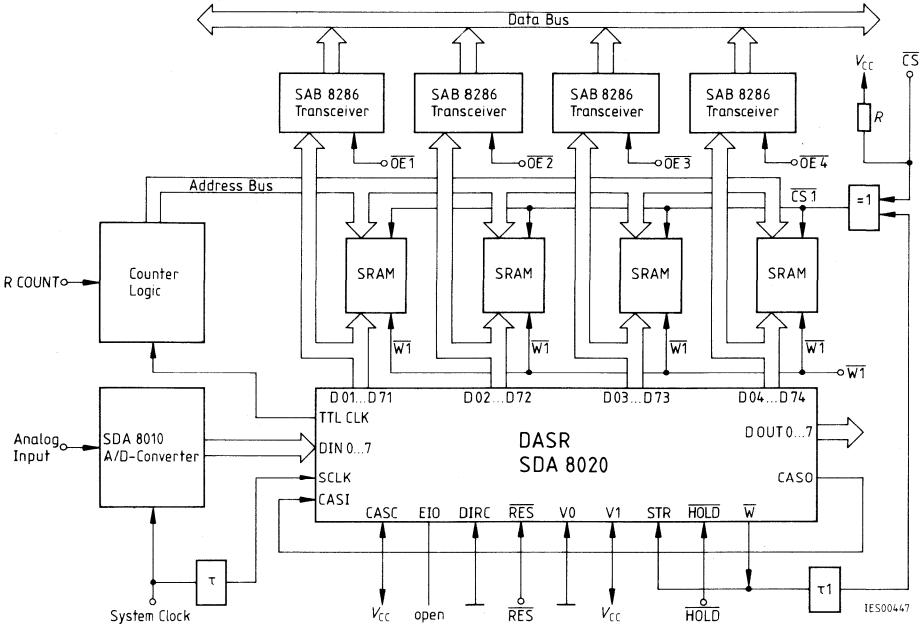
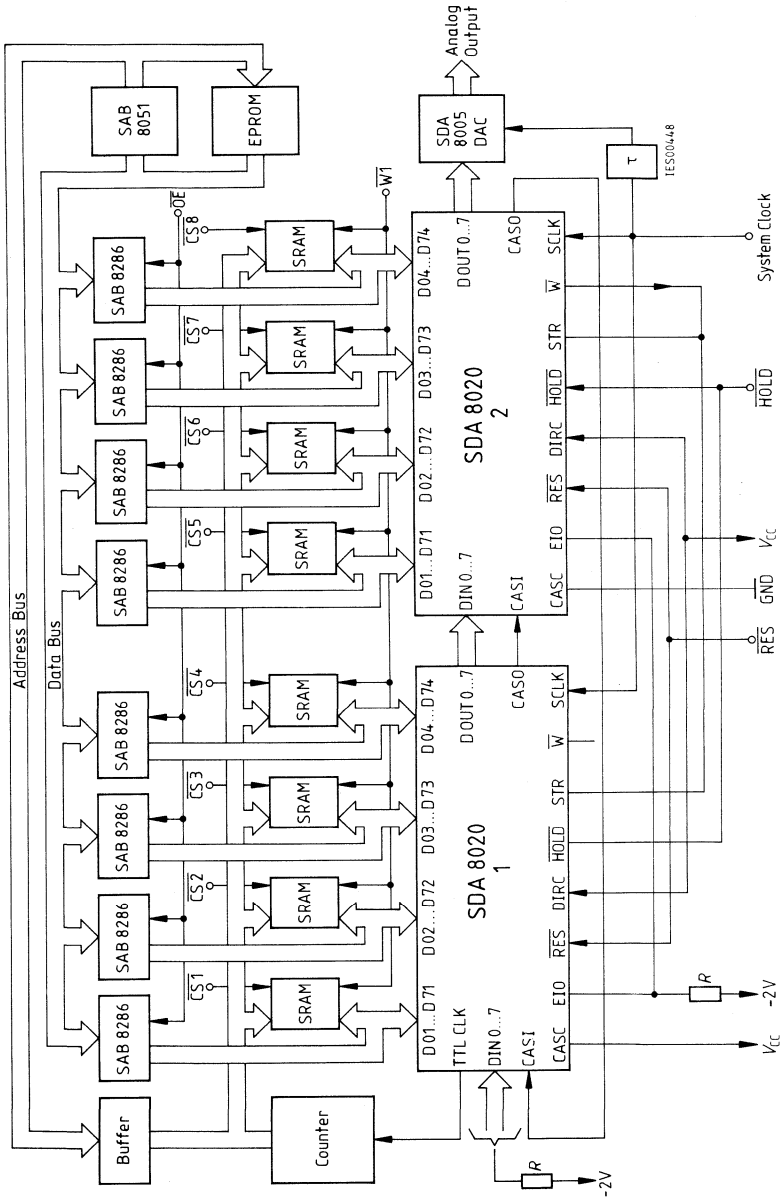


Figure 13
Application Circuit
Waveform Generation System



SIEMENS

Microprocessor-Compatible 8-Bit A/D Converters with 8-Channel Multiplexer

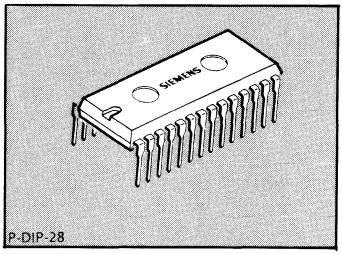
SDA 0808
SDA 1808

Preliminary Data

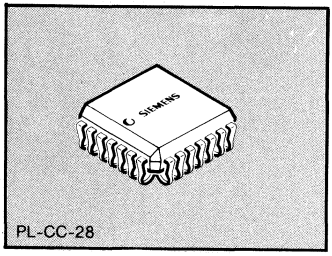
CMOS IC

Features

- **A**dvanced **CMOS** (ACMOS) technology
- 8-bit resolution
- Total unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (13 µs) (SDA 0808)
- Fast conversion time (15 µs) (SDA 1808)
- Single 5 V DC supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustment required
- Latched tristate outputs
- TTL-compatible output voltage
- Low power consumption (15 mW)



P-DIP-28



PL-CC-28

Type	Ordering Code	Package	Temp. Range
S SDA 0808 B	Q67100-A8129	P-DIP-28	−40 to 125 °C
SDA 0808 N	Q67100-A8206	PL-CC-28 (SMD)	−40 to 85 °C
SDA 1808 N	Q67100-A8254	PL-CC-28 (SMD)	−40 to 85 °C

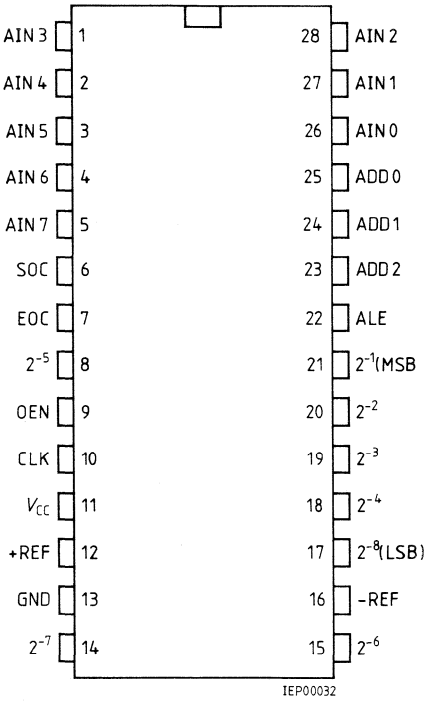
SDA 0808 and SDA 1808 are monolithic 8-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V DC supply. The IC contains a microprocessor-compatible control logic and an 8-bit data bus. They are pin-compatible with the data-acquisition component ADC 0808/0809.

SDA 0808 and SDA 1808 use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

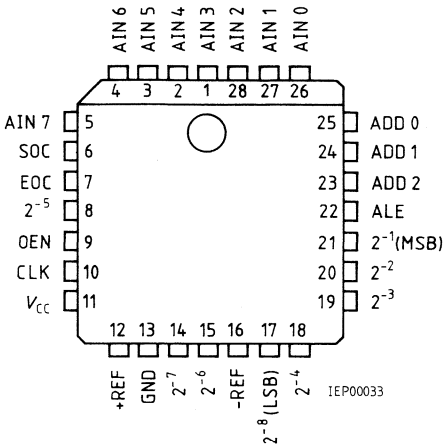
The temperature range of the SDA 0808 N, SDA 1808 N is −40 °C to 85 °C and that of the SDA 0808 B −40 °C to 125 °C. The SDA 0808 operates at a clock frequency of 1.5 MHz, the SDA 1808 at 2.5 MHz max.

Pin Configurations
(top view)

SDA 0808 B



SDA 0808 N,
SDA 1808 N



6

Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^{-5}	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11 12	V_{CC} + REF	Positive supply voltage Positive reference voltage
13	GND	Ground
14, 15	2^{-7}, 2^{-6}	Digital output signals
16	– REF	Negative reference voltage
17 to 21	2^{-8} (LSB) to 2^{-1} (MSB)	} Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 50 pF) as a sample and hold circuit, a successive-approximation register and a comparator.

The A/D converter's successive-approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output (end of conversion) passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is automatically set to zero, has a high resolution and a low drift. Thus the A/D converter is extremely insensitive to temperature errors.

A/D Converter Timing

The values stated apply to the SDA 0808, those in parentheses to the SDA 1808.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 10 (20) external clock cycles which will be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 10 (20) clock cycles.

Conversion of the sampled analog voltage takes place between the 11th (22nd) and 19th (38th) clock cycle after sampling has been completed. In the 19th (38th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 20th (40th) clock cycle.

Multiplexer

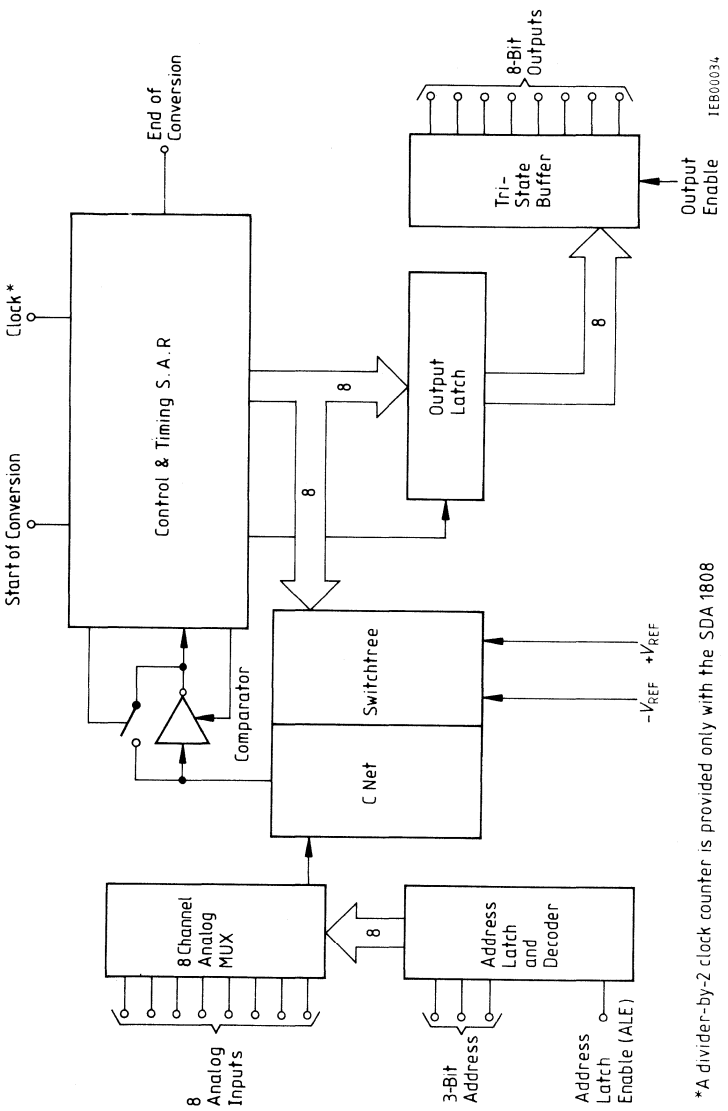
The converters provide eight multiplexed analog input channels. The input channels are selected by three address lines (AD2, AD1, AD0).

Table 1 shows the input states for the address lines that select a channel. The address is latched on the rising slope of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage[1])		V_{CC}		6.5	V
Input voltage range, any input		V_I	−0.3	V_{CC} +0.3	V
Junction temperature		T_j		150	°C
Storage temperature		T_{stg}	−65	125	°C
Thermal resistance system – ambient	P-DIP-28	$R_{th\ SA}$		50	K/W
	PL-CC-28	$R_{th\ SA}$		70	K/W

Operating Range

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage[2])	$+V_{REF}$		V_{CC}	V_{CC}+0.1	V
Negative reference voltage	$-V_{REF}$	−0.1	0		V
Differential reference voltage[10])	$\Delta V_{REF} = +V_{REF}-(-V_{REF})$		5		V
Analog input range	V_{AIN}	$-V_{REF}$		$+V_{REF}$	V
Slew rate[11]) at f_{CLK} = 1 MHz/2 MHz	SR			60	mV/µs
Start pulse duration	$t_{w\ (S)}$	200			ns
Address load control pulse width	$t_{w\ (ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0808	f_{CLK}	10	640	1500	kHz
SDA 1808	f_{CLK}	20	1280	2500	kHz
Ambient temperature					
SDA 0808 N; SDA 1808 N	T_A	−40		85	°C
SDA 0808 B	T_A	−40		125	°C

Characteristics

V_{CC} = 4.75 V to 5.25 V (unless otherwise specified)

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
High-level input voltage, control inputs	V_{IH}	V_{CC}−1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC}−0.4			V	I_Q = −360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA

For notes see 2 pages hereafter.

Characteristics

V_{CC} = 4.75 V to 5.25 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
OFF-state output current (high impedance-state)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			−3	µA	V_Q = 0
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			−1	µA	V_I = 0
Supply current	I_{CC}		0.3	3	mA	$f_{CLK} = f_{CLK}$ (typ.)
Input capacitance, control input	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance between pins 12 and 16	R	1		1000	kΩ	T_A = 25 °C

Analog Multiplexer

V_{CC} = 5 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Channel ON-state current[3]	I_{ON}			2	µA	V_I = 5 V, $f_{CLK} = f_{CLK}$ (typ.)
				−2	µA	V_I = 0 V, $f_{CLK} = f_{CLK}$ (typ.)
Channel OFF-state current	I_{OFF}		10	200	nA	V_{CC} = 5 V, T_A = 25 °C, V_I = 5 V
			−10	−200	nA	V_{CC} = 5 V, T_A = 25 °C, V_I = 0 V
				1	µA	V_{CC} = 5 V, V_I = 5 V
				−1	µA	V_{CC} = 5 V, V_I = 0 V

Characteristics

T_A = 25 °C, $V_{CC} = +V_{REF}$ = 5 V, $-V_{REF}$ = 0 V, $f_{CLK} = f_{CLK}$ (typ), unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply voltage sensitivity	k_{SVS}		±0.05		%/V	$V_{CC} = V_{REF+}$ = 4.75 V to 5.25 V, T_A = −40 °C to 85 °C[4]
Linearity error[5]				±0.5	LSB	
Zero error[6]				±0.5	LSB	

For notes see next page.

Characteristics

$T_A = 25\,°C$, $V_{CC} = +V_{REF} = 5$ V, $-V_{REF} = 0$ V, $f_{CLK} = f_{CLK}$ (typ.), unless otherwise specified

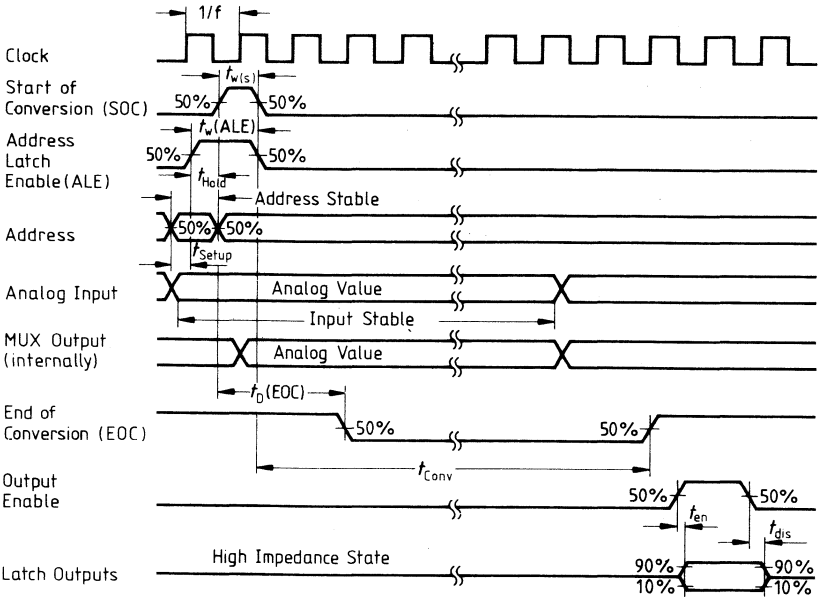
		Limit Values				
Total unadjusted error[7])			±0.25		LSB	$T_A = 25\,°C$
SDA 0808 N				±0.5	LSB	$T_A = -40\,°C$ to $85\,°C$
SDA 0808 B				±0.5	LSB	$T_A = -40\,°C$ to $125\,°C$
SDA 1808 N			±0.5	±1	LSB	$T_A = -40\,°C$ to $85\,°C$, $f_{CLK} = 2.5$ MHz
Output enable time **(Figure 1)**	t_{en}		80	150	ns	$C_L = 50$ pF, $R_L = 10$ kΩ
Output disable time **(Figure 1)**	t_{dis}		40	95	ns	$C_L = 10$ pF, $R_L = 10$ kΩ
Output turn-off time **(Figure 1)**	t_{OFF}		20	60	ns	$C_L = 10$ pF, $R_L = 10$ kΩ
Conversion time[12])	t_{Conv}	13	31	2000	µs	$f_{CLK} = 1.5$ MHz/640 kHz/10 kHz[8])
SDA 1808 N	t_{Conv}	15	31	2000	µs	$f_{CLK} = 2.5$ MHz/1280 kHz/20 kHz[8])
Delay time, EOC output	$t_{D\,(EOC)}$	0		200	ns	[9])

6

Notes

1) All voltage values refer to the network's ground terminal.
2) Care must be taken that this rating is observed, even during power-up.
3) The channel on-state current is primarily generated by the current of the Schmitt trigger and varies directly with the clock frequency.
4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and $+V_{REF}$ are changing together and the change in accuracy is measured with respect to full-scale deflection.
5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.
6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.
7) The total unadjusted error is the total-of-linearity error, zero and full-scale error.
8) SDA 0808: $t_{Conv\,max} = 20 \cdot 1/f_{CLK}$ $t_{Conv\,min} = 19 \cdot 1/f_{CLK}$;
   SDA 1808: $t_{Conv\,max} = 40 \cdot 1/f_{CLK}$ $t_{Conv\,min} = 38 \cdot 1/f_{CLK}$;
9) Refer to the operating pulse diagram.
10) For typical error versus reference voltage span refer to the respective diagram.
11) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full-scale errors. Filtering by a low pass ($R = 500\ \Omega$, $C = 100$ nF) or use of an external sample-and-hold is then required.
12) Including sample time.

Operating Pulse Diagram



Typical Error versus Reference Voltage Span

$V_{CC} = 5.0$ V; $f_{CLK} = f_{CLK}$ typ.; $\Delta V_{REF} = +V_{REF} - (-V_{REF})$

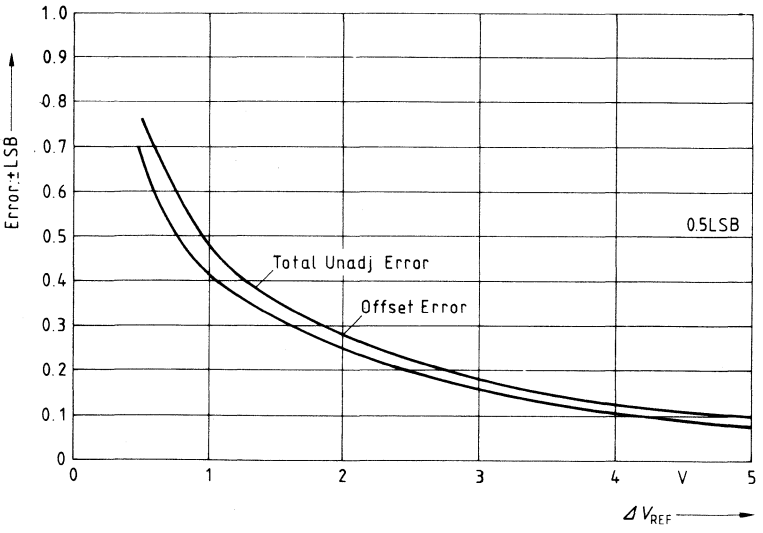
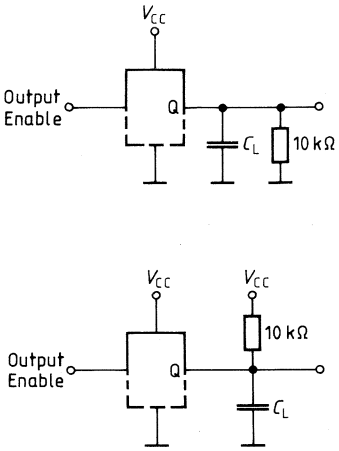
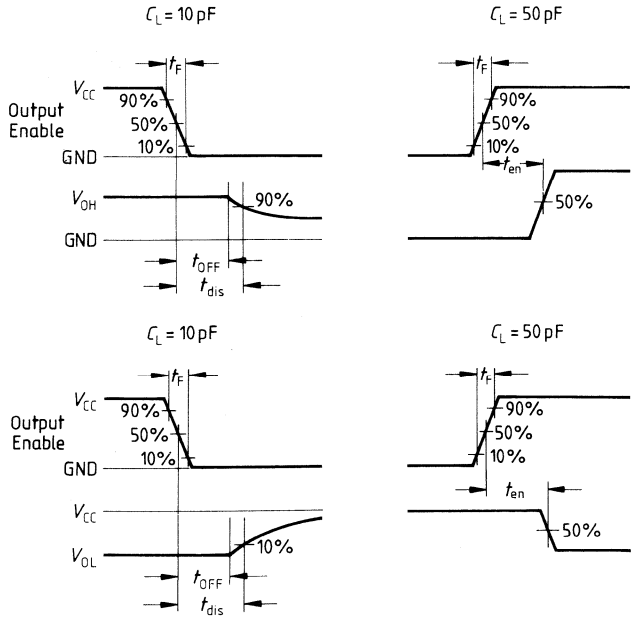


Figure 1
Tristate Measurement Circuits and Pulse Diagrams





Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates.

INTEL Microprocessors

A typical interface is shown in **Figure 2.**

Start of Conversion

A write instruction selects one of the analog input channels and starts the conversion.

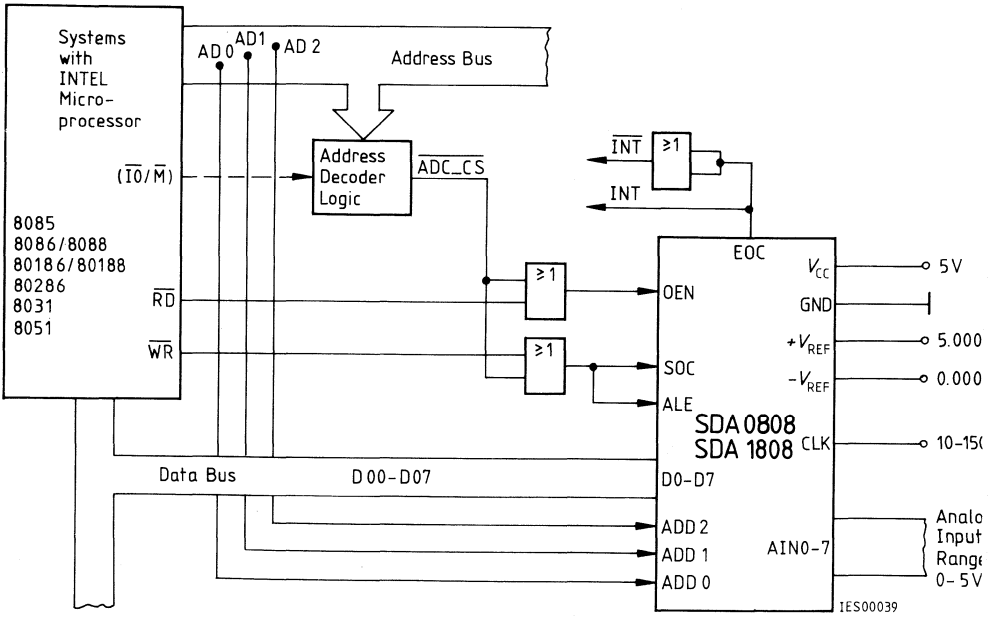
Write address: $\overline{\text{ADC\_CS}}$

The end of conversion signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the Conversion Result

With a read instruction the conversion result is read from the $\overline{\text{ADC\_CS}}$ address.

Figure 2



Motorola Microprocessors

A typical interface is shown in **figure 3.**

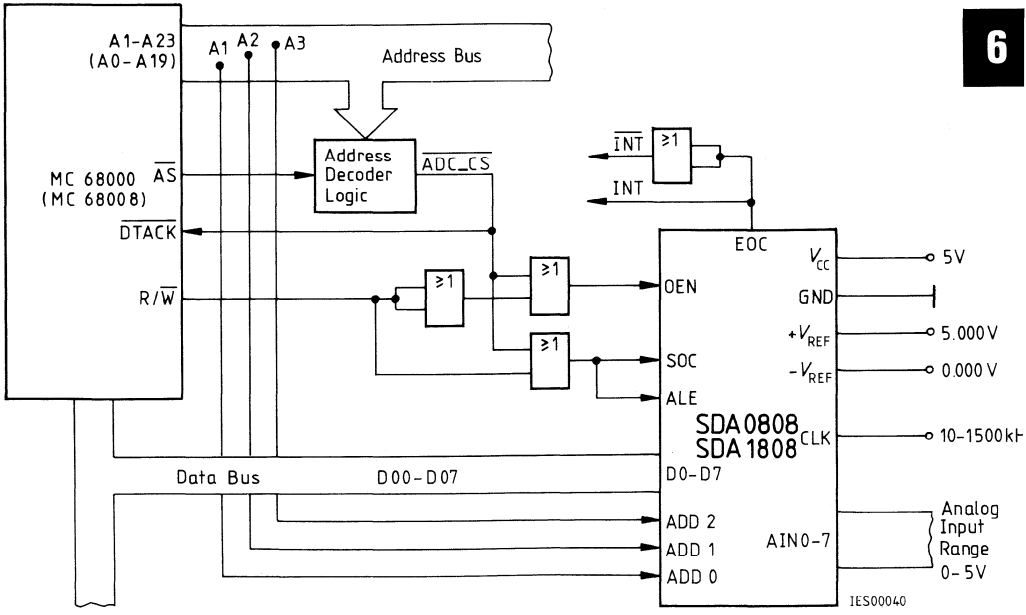
Start of Conversion

A write instruction to an address that has been decoded by the address decoder logic will start a conversion. The lower 3 bits of the address bus select the input channel.

Reading of the Conversion Result

A read instruction from the ADC-address puts the conversion result to the data bus: MOVE.B ADC-ADDRESS, D0 places the conversion data in the D0 register of the microprocessor.

Figure 3



Application Hints

Power Supply Decoupling

The power supply should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

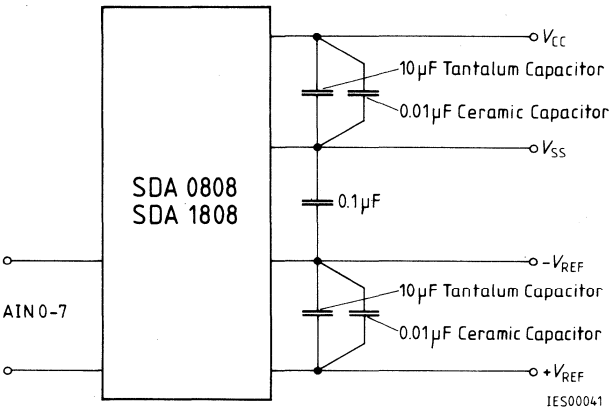
Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog Input

The high input impedance of the analog channels AIN0 to AIN7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq AIN \leq +V_{REF}$) can directly be connected to the analog input channels, that is, without additional buffering if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 10 (20 for SDA 1808) clock cycles.

Figure 4
Capacitors



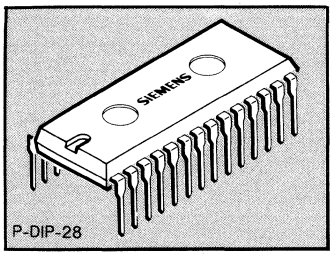
SIEMENS

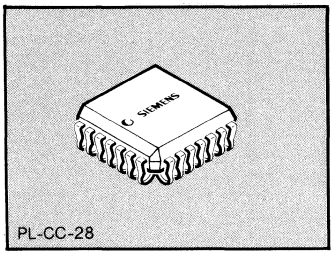
Microprocessor-Compatible 10-Bit A/D Converters with 8-Channel Multiplexer

SDA 0810
SDA 1810

Preliminary Data

ACMOS IC





Features

- **A**dvanced **CMOS** (ACMOS) technology
- 10 bit resolution
- Total unadjusted error ±1/2 LSB
- No missing codes
- Fast conversion time (15 µs)
- SDA 1810 D with 66 kHz sampling frequency
- Single 5 V dc supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustments required
- Latched tristate outputs
- TTL-compatible output voltages
- Low power consumption (15 mW)

Type	Ordering Code	Package	Temp. Range
SDA 0810 B	Q67100-A8144	P-DIP-28	−40 to 125 °C
SDA 0810 N	Q67100-A8207	PL-CC-28 (SMD)	−40 to 85 °C
▼SDA 1810 D	Q67100-H8730	P-DIP-28	−40 to 85 °C
SDA 1810 N	Q67100-A8230	PL-CC-28 (SMD)	−40 to 85 °C
▼SDA 1810 DN	Q67100-H8735	PL-CC-28 (SMD)	−40 to 85 °C

▼ New type

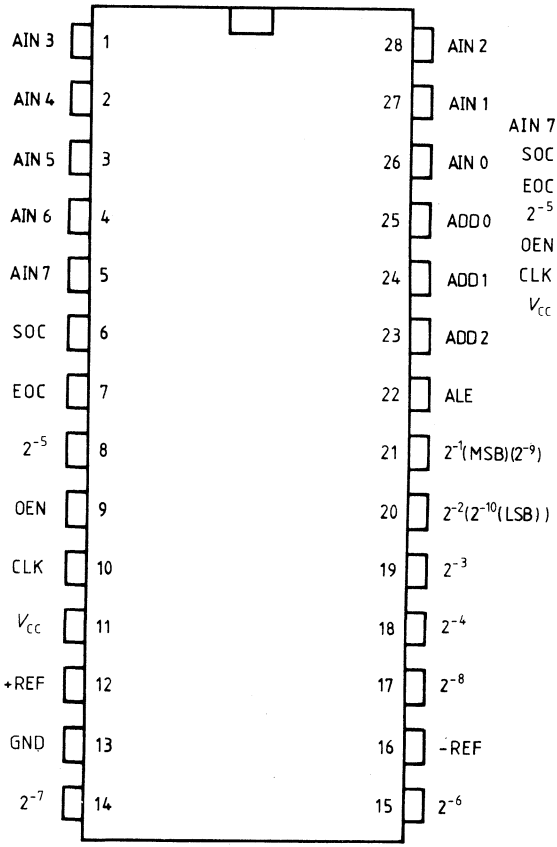
SDA 0810 and SDA 1810 are monolithic 10-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V DC supply. They contain a microprocessor-compatible control logic and an 8-bit data bus and are pin-compatible with the industrial standard ADC 0808 and 0809. The 10-bit data stream is supplied in a 2-byte format for interfacing with 8-bit microprocessors. While the SDA 0810 can be operated at a clock frequency of 1 MHz, the SDA 1810 operates at a clock frequency of 2 MHz. SDA 1810 D offers enhanced dynamic performance for analog input frequencies up to 33 kHz.

The converters use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

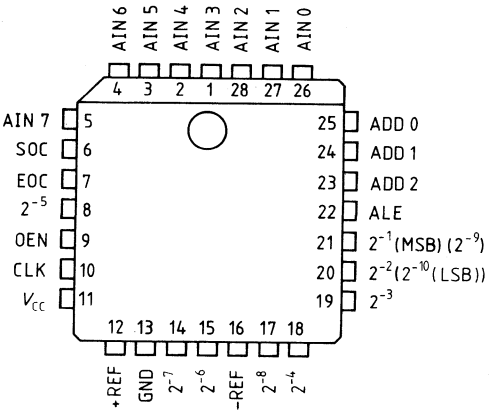
The temperature range of the SDA 0810 N and SDA 1810 N/D is −40 °C to 85 °C, and that of the SDA 0810 B −40 °C to 125 °C.

Pin Configurations
(top view)

SDA 0810 B;
SDA 1810 D;



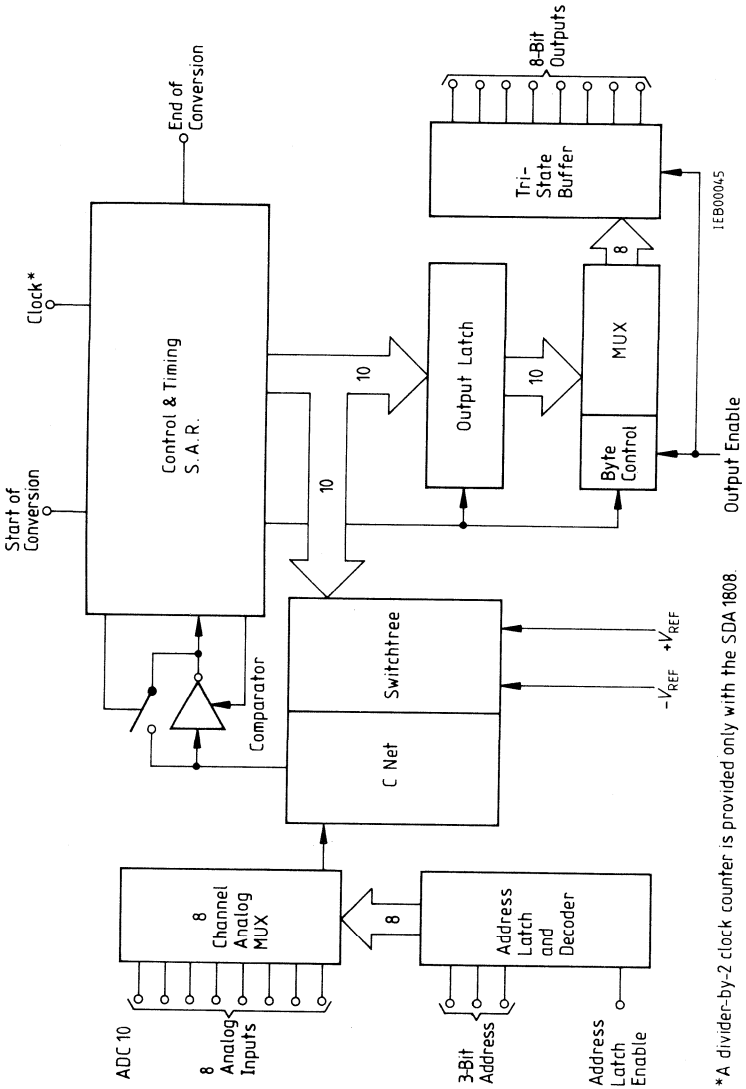
SDA 0810 N;
SDA 1810 N
SDA 1810 DN



Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^{-5}	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11	V_{CC}	Positive supply voltage
12	+ REF	Positive reference voltage
13	GND	Ground
14, 15	2^{-7}, 2^{-6}	Digital output signals
16	− REF	Negative reference voltage
17 to 21	2^{-8} to 2^{-1}	Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs

Block Diagram



Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 50 pF) as a sample and hold circuit, a successive-approximation register and a comparator.

The A/D converter's successive-approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator which is automatically set to zero; it has a high supply rejection factor.

A/D Converter Timing

The values stated apply to the SDA 0810, those in parentheses to the SDA 1810.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 4(8) external clock cycles which will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 4(8) clock cycles.

Conversion of the sampled analog voltage takes place between the 5th and 15th (10th and 30th) clock cycle after sampling has been completed. In the 15th (30th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 16th (32nd) clock cycle.

Multiplexer

The converter provides eight multiplexed analog input channels. The input channels are selected by programming three address lines (AD2, AD1, AD0).

Table 1 shows the input states of the address lines that select a channel. The address is latched on the rising edge of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Reading the Conversion Results

The data is read as two 8-bit bytes. The digital outputs of the converters are positive true. Data is presented left-justified and high byte first. The first OEN high after completion of a conversion enables high byte (2^{-1} to 2^{-8}) to the output buffers, the second OEN pulse enables the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are grounded. The byte control logic determines which byte is to be read. With each reading operation a flipflop is toggled so that in successive reading operations the bytes are output alternately. This flipflop is always reset to the high byte at the end of a conversion.

Data Bit Location

High Byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low Byte	2^{-9}	2^{-10}	0	0	0	0	0	0

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage[1])	V_{CC}		6.5	V
Input voltage range, any input	V_I	−0.3	V_{CC} +0.3	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance system-ambient				
P-DIP-28	$R_{th\ SA}$		50	K/W
PL-CC-28	$R_{th\ SA}$		70	K/W

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage[2])	$+V_{REF}$		V_{CC}	V_{CC}+0.1	V
Negative reference voltage	$-V_{REF}$	−0.1	0		V
Differential reference voltage[10])	$V_{REF} = +V_{REF} - (-V_{REF})$		5		V
Analog input range	V_{AIN}	$-V_{REF}$		$+V_{REF}$	V
Slew rate[11]) (f_{CLK} = 1 MHz/2 MHz)					
SDA 0810 B/N; SDA 1810 N	SR			78	mV/µs
Start pulse duration	$t_{W\ (S)}$	200			ns
Address load control pulse width	$t_{W\ (ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0810	f_{CLK}	50	640	1000	kHz
SDA 1810	f_{CLK}	100	1280	2000	kHz
Ambient temperature					
SDA 0810 N; SDA 1810 N/D	T_A	−40		85	°C
SDA 0810 B	T_A	−40		125	°C

For notes refer to 3 pages hereafter.

Characteristics in the Operating Temperature Range

V_{CC} = 4.75 V to 5.25 V, unless otherwise specified

Total Component

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
High-level input voltage, control inputs	V_{IH}	$V_{CC}-1.5$			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	$V_{CC}-0.4$			V	$I_Q = -360\ \mu A$
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state output current (high impedance-state)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			−3	µA	V_Q = 0
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			−1	µA	V_I = 0
Supply current	I_{CC}		0.3	3	mA	$f_{CLK} = f_{CLK}$ (typ)
Input capacitance, control inputs	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance between pins 12 and 16	R	1	1000		kΩ	

Characteristics

Analog Multiplexer

V_{CC} = 5 V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Channel on-state current[3])	I_{ON}					V_I = 5 V
				2	µA	$f_{CLK} = f_{CLK}$ (typ)
						V_I = 0 V
				−2	µA	$f_{CLK} = f_{CLK}$ (typ)
Channel off-state current	I_{OFF}					V_{CC} = 5 V
			10	200	nA	T_A = 25 °C, V_I = 5 V
						V_{CC} = 5 V
			−10	−200	nA	T_A = 25 °C, V_I = 0
				1	µA	V_{CC} = 5 V, V_I = 5 V
				−1	µA	V_{CC} = 5 V, V_I = 0

For notes refer to 2 pages hereafter.

Characteristics

$T_A = 25\,°C$, $V_{CC} = +V_{REF} = 5\,V$, $-V_{REF} = 0\,V$, $f_{CLK} = f_{CLK}$ (typ), unless otherwise specified

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply voltage sensitivity[4]	k_{SVS}		±0.05		%/V	$V_{CC} = +V_{REF} = 4.75\,V$ to 5.25 V, $T_A = -40\,°C$ to 85 °C
Linearity error[5]				±0.5	LSB	
Zero error[6] (except SDA 1810 D)				±0.5	LSB	
Total unadjusted error[7] SDA 0810 N SDA 0810 B SDA 1810 N			 	 ±0.5 ±0.5 ±1	 LSB LSB LSB	 $T_A = -40\,°C$ to 85 °C $T_A = -40\,°C$ to 125 °C $T_A = -40\,°$ to 85 °C, $f_{CLK} = 1$ MHz
Output enable time **(Figure 1)**	t_{en}		80	150	ns	$C_L = 50$ pF, $R_L = 10$ kΩ
Output disable time **(Figure 1)**	t_{dis}		40	95	ns	$C_L = 10$ pF, $R_L = 10$ Ω
Output turn-off time **(Figure 1)**	t_{OFF}		20	60	ns	$C_L = 10$ pF, $R_L = 10$ kΩ
Conversion time[8] SDA 0810	t_{Conv}	15	25	320	µs	$f_{CLK} = 1$ MHz/640 kHz/ 50 kHz
Conversion time[8] SDA 1810/1810 D	t_{Conv}	15	25	320	µs	$f_{CLK} = 2$ MHz/1280 kHz/ 100 kHz
Delay time, output EOC[9]	$t_{D\,(EOC)}$	0		200	ns	

Characteristics SDA 1810 D only

$T_A = 25\,°C$, $V_{CC} = +V_{REF} = 5\,V$, $-V_{REF} = 0\,V$, $f_{CLK} = 1.28$ MHz unless otherwise specified

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Total Unadjusted Error	*TUE*		±0.5	±1.25	LSB	$T_A = -40\,°C$ to 85 °C
Integral nonlin.	*INL*			±0.5	LSB	$T_A = -40\,°C$ to 85 °C
Differential nonlin.	*DNL*		±0.25	±0.5	LSB	$T_A = -40\,°C$ to 85 °C
Gain error			±0.125	±0.5	LSB	$T_A = -40\,°C$ to 85 °C
Zero error	*OFS*		±0.25	±1	LSB	$T_A = -40\,°C$ to 85 °C
Sampling rate	f_s			66	kHz	$f_{CLK} = 2$ MHz
Effective resolution			8.8		bits	$f_{AIN} = 30$ kHz

For notes refer to next page.

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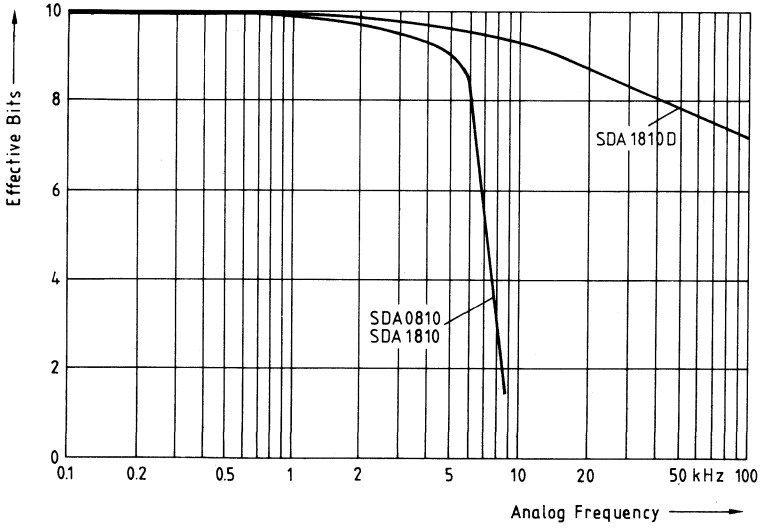
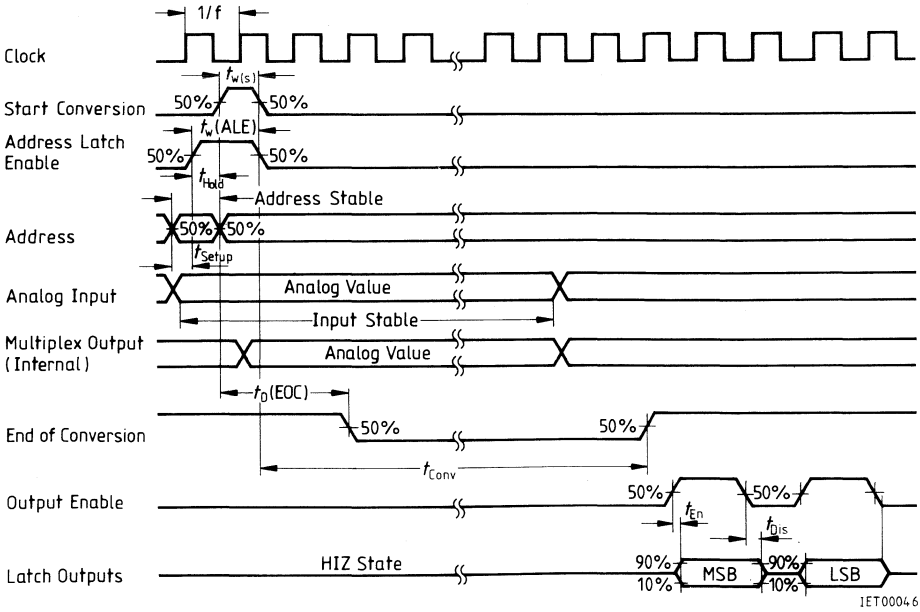
Notes

1) All voltage values refer to the network's ground terminal.
2) Care must be taken that this rating is observed, even during power-up
3) The channel on-state current is primarily generated by the current of the Schmitt trigger and varies directly with the clock frequency.
4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and $+V_{REF}$ are changing together and the change of accuracy is measured with respect to full-scale deflection.
5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.
6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.
7) The total unadjusted error is the total-of-linearity error, zero error, and full-scale error.
8) SDA 0810: $t_{Conv\ max} = 16 \cdot 1/f_{CLK}$, $t_{Conv\ min} = 15 \cdot 1/f_{CLK}$; including sampling time
   SDA 1810: $t_{Conv\ max} = 32 \cdot 1/f_{CLK}$, $t_{Conv\ min} = 30 \cdot 1/f_{CLK}$; including sampling time
9) Refer to the operating pulse diagram
10) For typical error versus reference voltage span refer to diagram page 30.
11) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full-scale errors (not SDA 1810 D!) Filtering by a low pass ($R = 2$ kΩ, $C = 100$ nF) or use of an external sample-and-hold is then required.

Effective Resolution versus Input Frequency
$V_{CC} = 5.0$ V, $+V_{REF} = 5$ V, $-V_{REF} = 0$ V, $f_{CLK} = f_{CLK(typ)}$



Operating Pulse Diagram



Typical Error versus Reference Voltage Span (SDA 0810 A/B/N, SDA 1810 N)

(Total unadjusted error including offset errors, full-scale errors, linearity errors and multiplexer errors). $V_{CC} = 5.0$ V; $f_{CLK} = f_{CLK\ (typ)}$; $\Delta V_{REF} = +V_{REF} - (-V_{REF})$

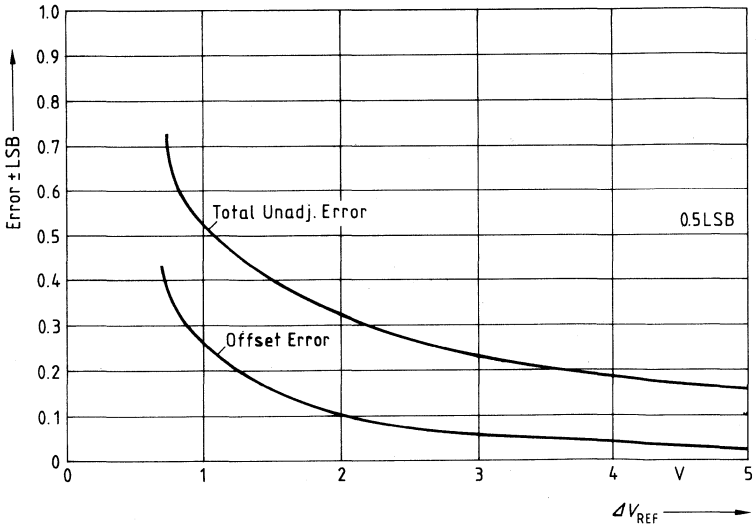
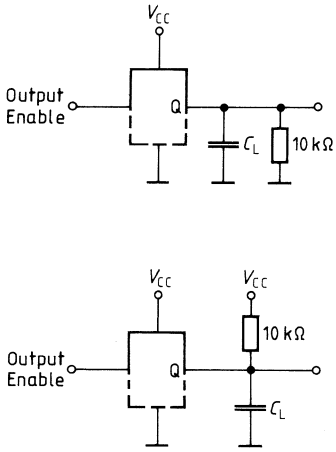
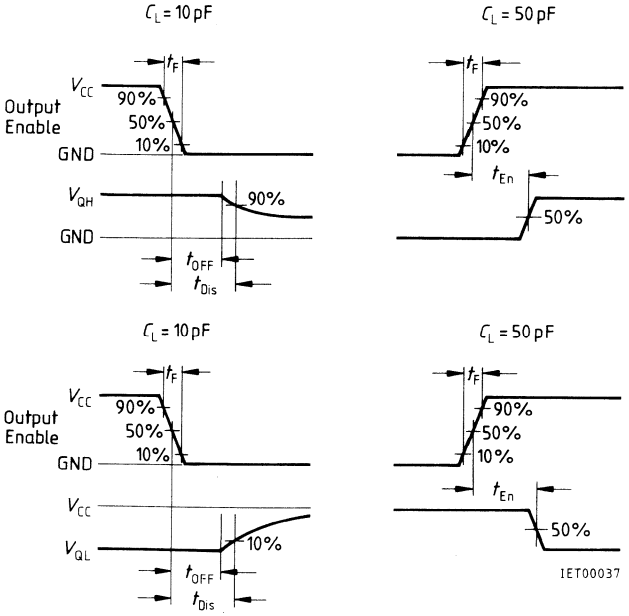


Figure 1
Tristate Measurement Circuits and Pulse Diagrams





Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates.

INTEL Microprocessors

A typical interface is shown in **figure 2.**

Start of Conversion

A write instruction selects one of the analog input channels and starts the conversion.

Write address: $\overline{\text{ADC\_CS}}$

The end of conversion-signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the Conversion Result

With the first read instruction the high byte is read from the $\overline{\text{ADC\_CS}}$ address, with the second read instruction the low byte is read.

6

Figure 2

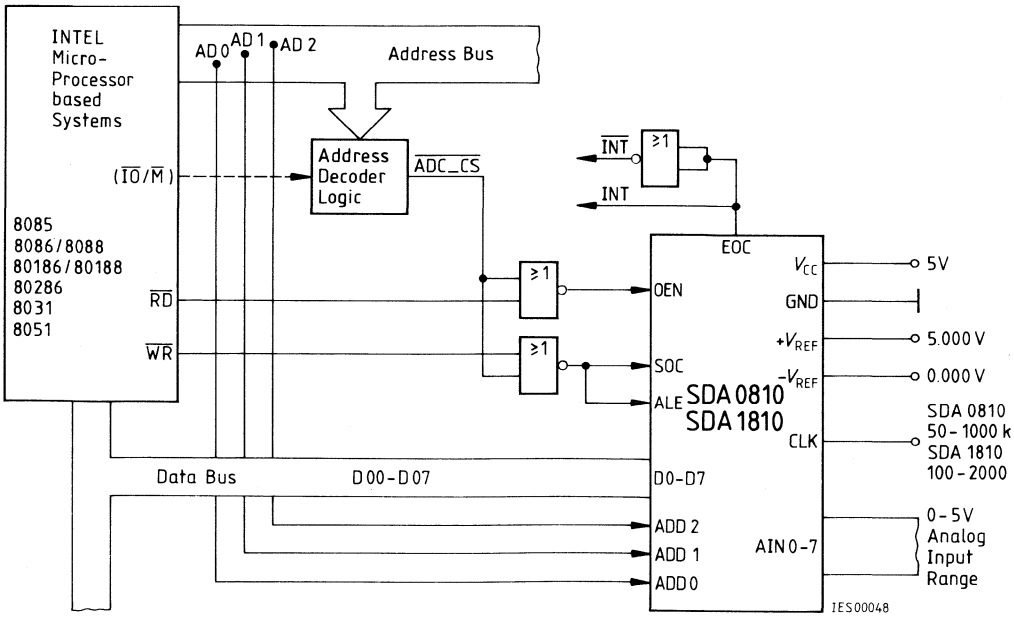
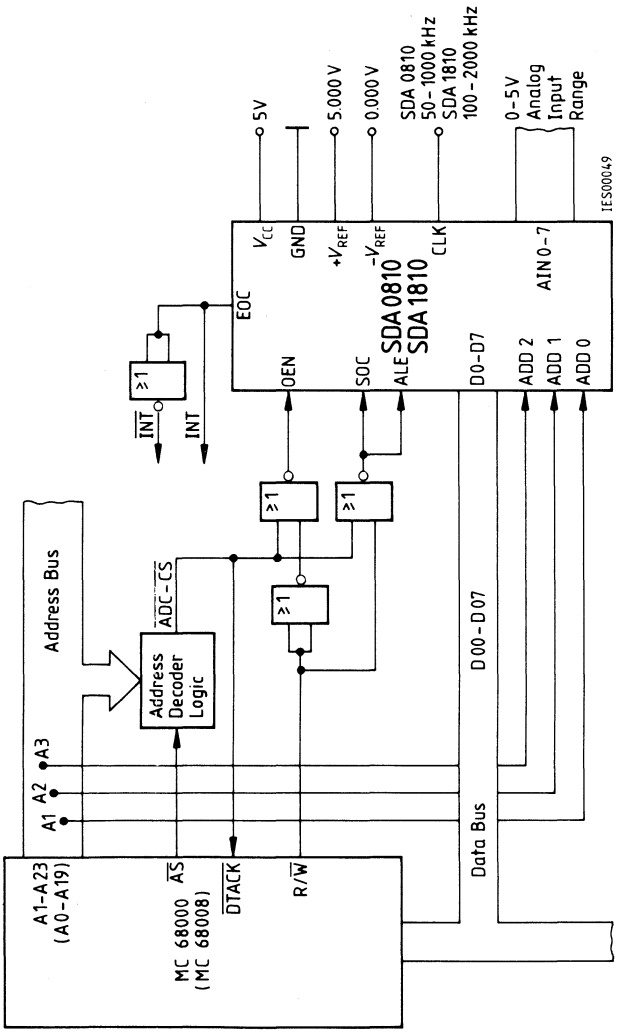


Figure 3

Motorola Microprocessors

A typical interface is shown in **figure 3.**



Application Hints

Power Supply Decoupling

The power supply should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

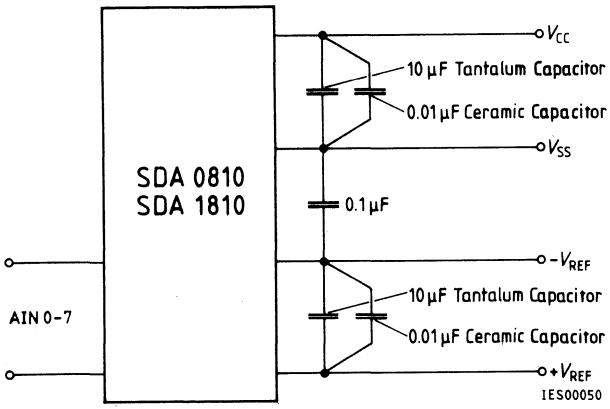
Reference Voltage

To avoid dynamic errors, a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog Input

The high input impedance of the analog channels AIN 0 to AIN 7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq AIN \leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 4 clock cycles for the SDA 0810 and 8 clock cycles for the SDA 1810.

Figure 4
Capacitors



SIEMENS

12-Bit A/D Converter with 4-Channel Multiplexer

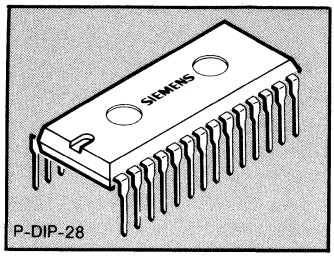
SDA 0812 A
SDA 1812 D

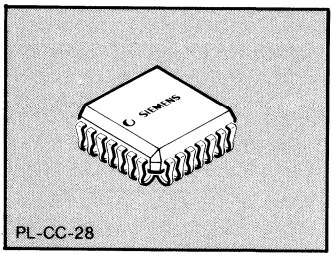
Preliminary Data

CMOS

Features

- 12 bit resolution
- Autocalibration circuitry
- No offset or gain adjustments required
- Total unadjusted error ± 1/2 LSB max. (SDA 0812 A) respectively ± 3/4 LSB max. (SDA 1812 D)
- Fast conversion time (6 µs)
- SDA 1812 D with over 100 kHz sampling rate
- No missing codes
- *S/N + THD* together 71 dB typ
- Single 5 V supply
- 4-channel multiplexer with latched control logic
- Easy interfacing to 8- and 16-bit microprocessors
- Data output in a 2-byte format
- 0 V to 5 V analog input voltage range
- Digital inputs and outputs are TTL compatible
- Standby mode (50 µW typ)
- CMOS low power consumption (10 mW typ)
- Temperature range −40 °C to 85 °C





Type	Ordering Code	Package
SDA 0812 A	Q67100-A8233	P-DIP-28
▼ SDA 0812 AN	Q67100-A8300	PL-CC-28 (SMD)
▼ SDA 1812 D	Q67100-A8291	P-DIP-28
▼ SDA 1812 DN	Q67100-A8301	PL-CC-28 (SMD)

▼ New type

General Description

SDA 0812 A and SDA 1812 D are monolithic CMOS 12-bit analog to digital converters with a 4-channel analog multiplexer. They need only a 5 V supply and achieve a conversion time of 6 µs plus 2.5 µs sample time.

They use the method of successive approximation based on a capacitor network. **An autocalibration circuit guarantees a total unadjusted error within ±1/2 LSB max. (SDA 0812 A) respectively ±1/2 LSB typ. (SDA 1812 D).** Therefore the device needs no external offset or gain adjustments. The converters feature a temperature stabilized differential comparator, a sample and hold function and a 12-bit data output in a 2-byte format. Designed for easy microprocessor interface using the standard control signals $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ the 4-channel input multiplexer is controlled via address inputs A0 and A1.

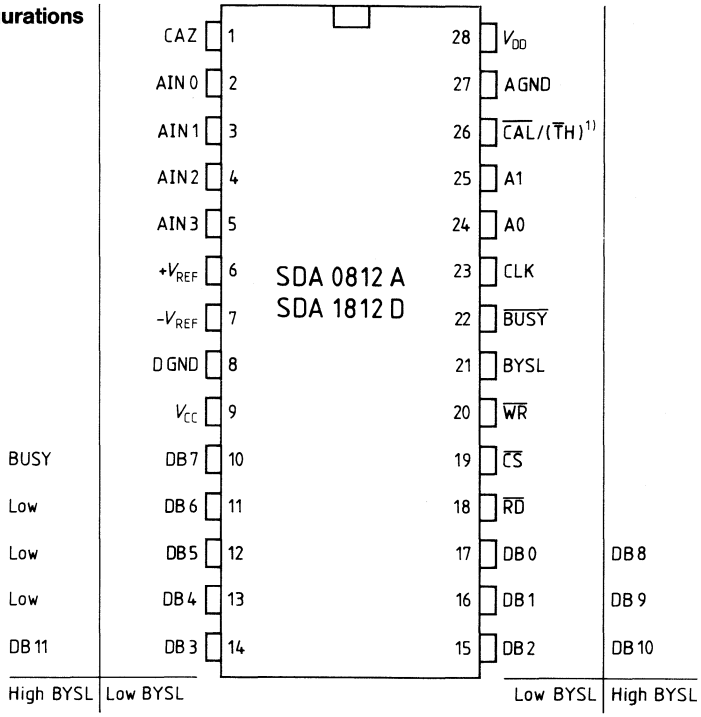
Two converter busy flags are available to facilitate polling of the converter's status.

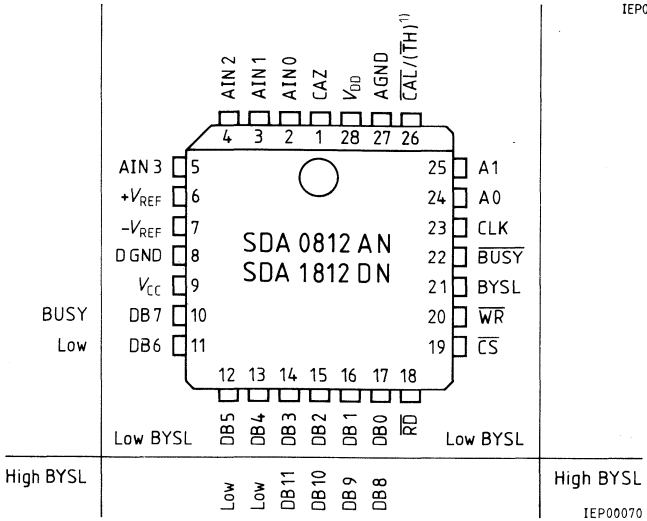
With a sample and hold circuit on chip, the SDA 1812 D is suited for digitizing AC signals as well as DC signals. The maximum sampling rate of the SDA 1812 D is more than 100 kHz according to 2.5 µs sample time plus 6 µs conversion time. The SDA 1812 D is specified with traditional static specifications as well as with dynamic specifications (SNR, THD, effective number of bits).

The temperature range of the SDA 0812 A/1812 D is −40 °C to 85 °C.

6

Pin Configurations
(top view)





[1] $\overline{TH}$: pin refers to SDA 1812 D

Pin Definitions and Functions

Pin	Symbol	Function
1	CAZ	Special function pin (see Reading the Conversion Results, SFR and Internal Clock Operation). Connect to a MP address pin. If not used, CAZ can be connected to AGND or DGND or can be unconnected.
2-5	AIN0 to AIN3	**Analog Input,** channel 0 to channel 3
6	$+V_{REF}$	Pos. voltage reference input, $+V_{REF} = 5$ V
7	$-V_{REF}$	Neg. voltage reference input $-V_{REF} = 0$ V
8	DGND	**Digital Ground,** DGND = 0 V
9	V_{CC}	Logic supply voltage, $V_{CC} = 5$ V must not be applied before V_{DD}!
10-17	DB0-DB7	Three-state data outputs. **Data Bus** output ($\overline{CS}$, $\overline{RD}$ = LOW)
	Symbol (BYSL = HIGH)	Symbol (BYSL = LOW)
10	BUSY	DB7 BUSY is an active high converter status flag. It is high
11	LOW	DB6 during a conversion and during autocalibration.
12	LOW	DB5 LOW Pin 11 to pin 13 are tied to DGND when
13	LOW	DB4 BYSL = HIGH
14	DB11 (MSB)	DB3 DB11 is the MSB.
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0(LSB) DB0 is the LSB.
18	$\overline{RD}$	Read input, active low, is used to read the data outputs in combination with $\overline{CS}$ and BYSL.
19	$\overline{CS}$	**Chip Select** input, active low.
20	$\overline{WR}$	**Write** input, active low, is used to start a new conversion and to select an analog channel via address inputs A0, A1 in combination with $\overline{CS}$ low. The minimum $\overline{WR}$ pulse width is 100 ns. It is independent of internal/external clock operation.
21	BYSL	**Byte Select** input, is used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.

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Pin Definitions and Functions (continued)

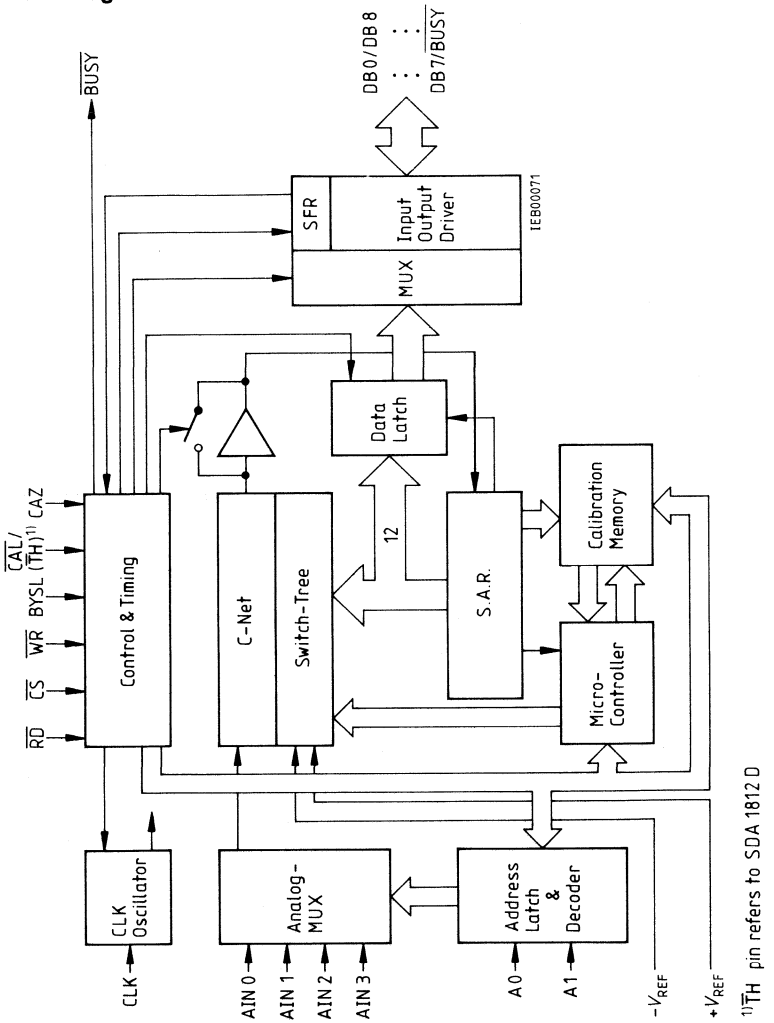
Pin	Symbol	Function
22	$\overline{BUSY}$	Converter status output. $\overline{BUSY}$ is low during conversion or autocalibration. $\overline{BUSY}$ is high after the converter has finished its operation.
23	CLK	**Clock** input for internal/external clock operation. For external clock operation connect pin 23 to a 74HC compatible clock source. For internal clock operation connect pin 23 to a R timing component (see Clock Operation description).
24-25	A0 to A1	**Address** inputs, are used to select one of four analog input channels, in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched with the rising edge of $\overline{WR}$.

A1	A0	Selected Channel
LOW	LOW	AIN0
LOW	HIGH	AIN1
HIGH	LOW	AIN2
HIGH	HIGH	AIN3

26	$\overline{CAL}/\overline{TH}$)[1]	**Calibration** input. An autocalibration cycle is initiated with $\overline{CAL}$ = LOW. If not used, $\overline{CAL}$ can be connected to V_{CC} or unconnected. In this case autocalibration is only initiated by power-up/power-fail, or by SFR. The minimum pulse width of CAL is 100 ns. Using the SDA 1812 D, via SFR the function of pin 26 can be defined as an external Track-Hold ($\overline{TH}$) pin (see SFR description).
27	AGND	**Analog Ground,** AGND = 0 V
28	V_{DD}	Analog supply, V_{DD} = 5 V, must not be applied after V_{CC}!

[1] $\overline{TH}$-pin refers to SDA 1812D

Block Diagram



6

Functional Description

SDA 0812 A and 1812 D are 4-channel 12-bit A/D converters. The successive approximation technique provides 6 µs conversion time. The required sampling time of the on-chip sample-and-hold-circuit is 2.5 µs. An autocalibration technique guarantees a total unadjusted error within ± 1/2 LSB max. (SDA 0812 A) and ± 3/4 LSB max. (SDA 1812 D) over the entire temperature range. The major components are shown in the **block diagram.**

The comparator is a fully differential autozeroed one for a high power supply rejection ratio and very low offset voltages. The charge redistribution design using a binary weighted capacitor network inherents the sampling function to convert AC-signals (SDA 1812 D). A Sub-C Network is used to correct linearity-errors in the Main-Capacitor Network. The correction terms are calculated by a microcontroller in an autocalibration cycle, started by power-up or $\overline{CAL}$ signal. The correction terms are stored in a calibration memory. The stability of integrated C-Networks guarantees the correction terms to be valid over time and temperature. In the case of a power up/power fail (V_{CC} less then 3 V typical) new calibration cycles will be initiated automatically. This guarantees the integrity of the correction terms.

Three-state output drivers with multiplexer for 2-byte data format, an analog multiplexer with address latch and a clock oscillator with external or internal clock operation complete the functional components of the device.

A/D Converter Timing

SDA 0812 A

After a conversion has been started with the rising edge of $\overline{WR}$ the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time. In parallel an offset compensation mechanism reduces the comparators offset error below 1/4 LSB. During this period the converter is susceptable to spikes and noise at the analog input, which may cause erroneous codes at the digital outputs. Therefore RC-filtering at the analog iputs is recommended.

Conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle. The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin. (See Special Function Register).

SDA 1812 D

After a conversion has been started with the rising edge of $\overline{WR}$ the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time.

By starting a conversion with $\overline{WR}$ sampling of the analog signal is defined by the first rising edge of the internal CLK pulse + 4.5 clock cycles + 100 ns (typ) after the rising edge of $\overline{WR}$. For precisely defined sampling point $\overline{WR}$ has to be synchronized with CLK. The conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle.

To avoid synchronizing problems between $\overline{WR}$ and CLK the $\overline{CAL}$ pin is programmable into an external Track-Hold pin ($\overline{TH}$) via SFR. A low to high transition at this pin defines the sampling point of the ADC with a delay time of 5 ns typ. without synchronizing to CLK. The low pulse width of $\overline{TH}$ defines the tracking period of internal sample and hold circuit

and should be 2.5 µs min. Using this $\overline{TH}$ pin an additional offset error of ± 1 LSB may occure. This $\overline{TH}$ pin should be used in combination with on chip clock generator. Using external clock generator in combination with asynchronous $\overline{TH}$ function brings offset errors up to ± 4 LSB via pin coupling effects. By synchronizing the $\overline{TH}$ signal with external CLK this offset error can be reduced again to ± 1 LSB. The best conditions are given by delaying the falling clock slope 20 ns to the rising edge of $\overline{TH}$.

The SDA 1812 D operates with the master clock. The conversion cycle may not begin until up to 1.5 clock cycles after $\overline{TH}$ goes high.

The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin (see Special Function Register).

Autocalibration

An autocalibration cycle is started
- with the rising edge of a $\overline{CAL}$ low pulse
- by setting the DB 1 in the Special Function Register (SFR)
- by power-up/power-fail

and takes 168 clock cycles. Finally a normal conversion (17 clock cycles) is added automatically. During a autocalibration or conversion cycle each power supply voltage and each reference voltage has to be stable. Therefore an internal timer provides a waiting period of 42240 clock cycles between power up/power fail and autocalibration function. Power up calibration is finished after 42425 (42240 + 168 + 17) clock cycles.

Reading the Conversion Results

Normal Mode (Transparent)

The data is read as two 8-bit bytes. The converters digital outputs are positive true. Data is presented in right justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the BYSL input determines which byte is to be read. Because the conversion results are held in a successive approximation register the high byte may be read out before the conversion is finished.

The 4 most significant bits are valid in the 10^{th} clock cycle after starting a conversion with $\overline{WR}$. Valid 12-bit data are available for reading after the $\overline{BUSY}$ pin has gone high, or internal status flag $\overline{BUSY}$ (available on pin 10) has gone low.

Latched Output Mode

An additional function is reading the data is available via an integrated data latch, which is transparent in normal function mode.

The latched output function may be activated by writing high on DB0 and low on DB7 (see Special Function Register SFR) with $\overline{WR}$, $\overline{CS}$ active in combination with CAZ and BYSL pin high.

The data latch is set transparent by power up.

When the latch function is active an internal generated latch enable signal shifts the data from the SAR into a 12-bit latch. This occures when $\overline{BUSY}$ gets inactive (high). The conversion result is valid during the next conversion cycle until new data is latched. Therefore it may be read out even after starting a new conversion.

Figure 1

Starting a Conversion with $\overline{WR}$

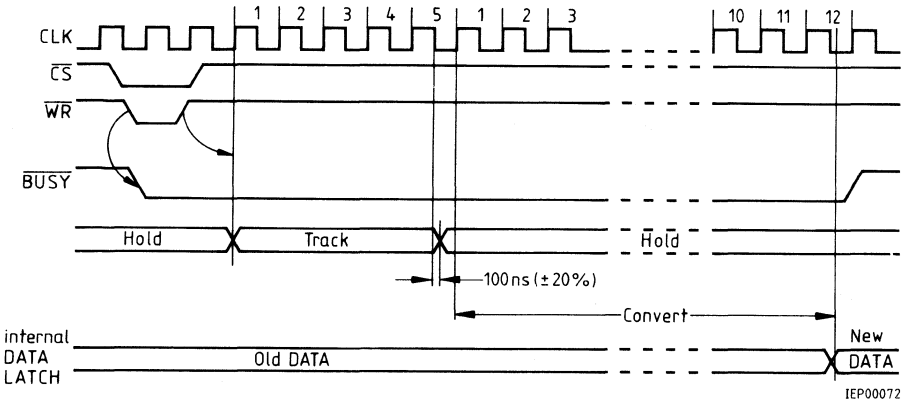
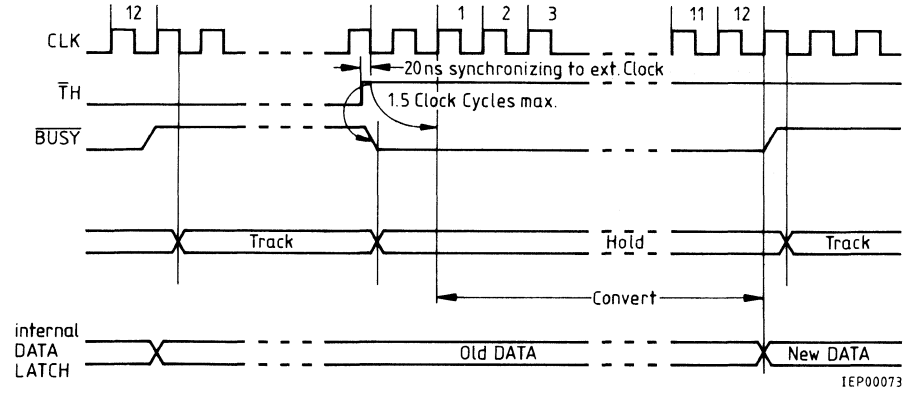


Figure 2

Starting a Conversion with $\overline{TH}$ (SDA 1812 D)

may be asynchronous with internal clock generator and should be synchronized with external clock for best performance.



The Special Function Register (SFR)

An internal register for additional functions programmed by the microprocessor is available.

Special Functions

SDA 0812 A

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-$\overline{\text{CAL}}$ starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-$\overline{\text{CAL}}$ function (168 + 17 clock cycles).
- The converter is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduced to 50 µW typ. Wake up the converter by writing low to DB3, ext. $\overline{\text{CAL}}$, INT-$\overline{\text{CAL}}$ (DB1) or power-up function ($V_{CC} < 3$ V). Applying $\overline{\text{CS}}$ and $\overline{\text{WR}}$ (start of conversion) during standby mode (DB3 high) delivers one correct conversion result, subsequently the converter goes back to standby mode until new conversion start or wake-up signal.
- POWER FAIL FLAG is set if a power fail occured, showing that a new calibration was started ($\overline{\text{BUSY}}$ active) and that the data of SFR (data latch enable) are lost. To reset this flag write low to DB5.
- CAL-ERROR flag is set on DB6 if a calibration overflow occurs (may be in very noisy systems). It is reset by starting a calibration and remains low after a properly finished calibration.
- $\overline{\text{BUSY}}$ flag is high (DB7) if a calibration or a conversion is in process.

SDA 1812 D

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-$\overline{\text{CAL}}$ starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-$\overline{\text{CAL}}$ function (168 + 17 clock cycles).
- The $\overline{\text{CAL}}$ pin function is modified to an ext. Track-Hold ($\overline{\text{TH}}$) function by setting DB2 high. Reset the function to $\overline{\text{CAL}}$ by writing low into DB2. The ext. Track-Hold pin ($\overline{\text{TH}}$) guarantees sampling points precisely defined by the rising edge of $\overline{\text{TH}}$ signal. The internal sampling point is delayed 5 ns typ. to the external $\overline{\text{TH}}$ slope.
- The SDA 1812 D is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduces to 50 µW typ. Wake up the SDA 1812 with writing low to DB3, EXT- $\overline{\text{CAL}}$, INT-$\overline{\text{CAL}}$ (DB1) or power-up function ($V_{CC} > 3$ V). Applying $\overline{\text{WR}}$ and $\overline{\text{CS}}$ or a rising edge on $\overline{\text{TH}}$ pin (Conversion Start) during standby mode (DB3 high) delivers one correct conversion result, subsequently the SDA 1812 D goes back to standby mode until new SOC or WAKE UP signal.
- POWER FAIL FLAG is set if power fail occured (DB5), showing that a new calibration has been started ($\overline{\text{BUSY}}$ active) and that the data of SFR (data latch enable $\overline{\text{CAL}}$/$\overline{\text{TH}}$ pin programming) are lost. To reset this flag write low to DB5.
- $\overline{\text{CAL}}$-ERROR flag is set on DB6 if an calibration overflow occures (may be in very noisy systems), is reset by starting a calibration and remains low after a properly finished calibration.
- $\overline{\text{BUSY}}$ FLAG is high (DB7) if a calibration or a conversion is in process.

Note that all programmable bits of the SFR are reset to low by power-up.

Writing the SFR (SDA 0812 A/1812 D, see figure 9)

The SFR is activated by pulling CAZ and BYSL pins high and loading a data word with a general low on DB 7 by a microprocessor WRITE cycle.

other DB	DB7	DB5	DB3	DB2*)	DB1	DB0	$\overline{CS}/\overline{WR}$	CAZ/ BYSL	Function
reserved	LOW	LOW					active	HIGH	Reset of POWER FAIL FLAG
reserved	LOW	HIGH					active	HIGH	Set POWER FAIL FLAG (not locked)
reserved	LOW		LOW				active	HIGH	Wake-up from STANDBY
reserved	LOW		HIGH				active	HIGH	STANDBY mode active
reserved	LOW			LOW			active	HIGH	$\overline{CAL}$ function on pin 26
reserved	LOW			HIGH			active	HIGH	$\overline{TH}$ function on pin 26
reserved	LOW				LOW		active	HIGH	–
reserved	LOW				HIGH		active	HIGH	INT-$\overline{CAL}$ is initiated
reserved	LOW					LOW	active	HIGH	Output data latch transparent
reserved	LOW					HIGH	active	HIGH	Output data latch enabled

Reading the SFR (SDA 0812 A; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Function
DB0	DATA LATCH State: HIGH enabled, LOW transparent
DB1	CAL FLAG: HIGH during calibration
DB2	RESERVED
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Warning: Reading on CAZ high and BYSL low is prevented for factory use, unpredictable data may appear on the data bus.

*) Refers to SDA 1812 D

Reading the SFR (SDA 1812 D; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Definition
DB0	DATA LATCH state: HIGH enabled, LOW transparent
DB1	$\overline{\text{CAL}}$ FLAG: HIGH during calibration
DB2	$\overline{\text{CAL}}/\overline{\text{TH}}$: HIGH for $\overline{\text{TH}}$, LOW for $\overline{\text{CAL}}$ function
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Reading on CAZ high and BYSL low is reserved for factory use only, unpredictable data may appear on the data bus.

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 3.**

Figure 3
The Internal Clock Frequency only depends on the *R* Value

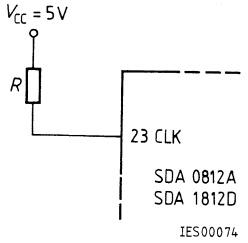
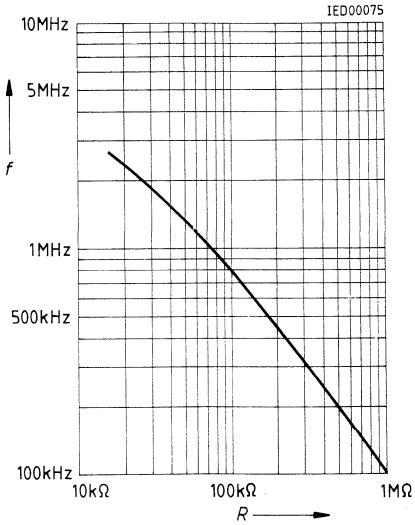


Figure 4
Clock Frequency of Internal Clock Generator versus External Resistor Value

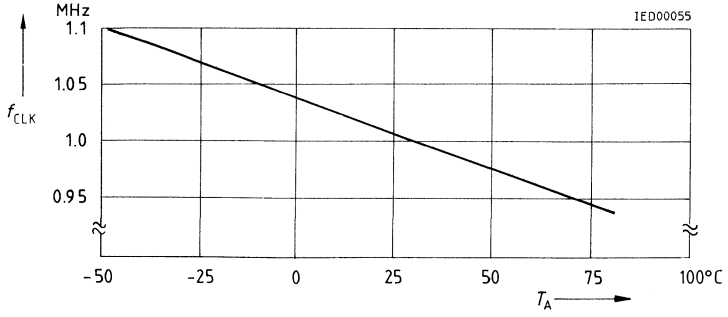


The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.4 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device by up to 20%. This is due to parameter variations of the CMOS process.

Therefore for precisely defined conversion times usage of an external clock generator is recommended.

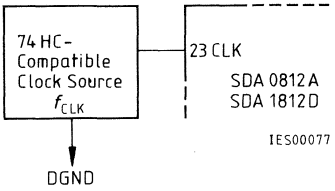
Figure 5
Typical Internal Clock Frequency versus Temperature



External Clock Operation

The required circuitry for external clock operation is shown in **figure 6.**

Figure 6



The external clock source has to provide 0.8 Vmax for low voltage level and 3.5 Vmin for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. $\overline{TH}$ signal. Synchronizing should be provided for optimal performance, see A/D converter timing on page 9. Note that the specification are referenced to $f_{CLK} = 2$ MHz. Typically, the specified accuracy is maintained from 0.5 to 2.2 MHz.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Units
		min.	max.	
Supply voltages[1]	V_{CC}, V_{DD}		6.5	V
Input voltage range (all inputs)	V_I	−0.3	V_{CC} +0.3	V
Package dissipation (at or below 25 °C free-air temperature range)			875	mW
Ambient temperature	T_A	−40	85	°C
Storage temperature	T_{stg}	−65	125	°C

Note:

[1] All voltage values are with respect to network ground terminal

Characteristics (SDA 0812 A)

$V_{DD} = 5\ V \pm 5\%$, $V_{CC} = 5\ V \pm 5\%$, $V_{DD} \geq V_{CC} \geq +V_{REF}$, $-V_{REF} = 0\ V$, DGND = 0 V, AGND = 0 V
$f_{CLK} = 2$ MHz, all specifications T_{min} to T_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Units	Conditions
		min.	typ.	max.		
Accuracy						
Resolution		12			Bit	No missing codes guaranteed
Total unadjusted error[1]	*TUE*			+/−1/2	LSB	All channels, AIN0 - AIN3
Differential nonlinearity	*DNL*			+/−1/2	LSB	
Full scale error (gain error)	*GE*			+/−1/4	LSB	All channels, AIN0 - AIN3
Offset error	*OFS*			+/−1/4	LSB	All channels, AIN0 - AIN3
Channel to channel mismatch				+/−1/4	LSB	
Analog Inputs						
Analog input range	V_{AIN}	$-V_{REF}$		V_{REF}	V	
Slew rate[2]	*SR*			8	mV/µs	
Multiplexer						
Settling time			20		ns	Switch delay after pro-
ON resistance	R_{ON}		2		kΩ	gramming the input channel
OFF resistance	R_{OFF}		10		MΩ	
On channel input capacitance	C_{AIN}		50		pF	
Input leakage current						
at 25 °C	I_{AIN}			10	nA	AIN0 - AIN3
at T_{min} to T_{max}	I_{AIN}			100	nA	
On-state bias current			+/−5		µA	Depends on analog input voltage
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75	5	V_{DD}	V	For specified
Negative reference voltage	$-V_{REF}$		0		V	performance
Input reference current	I_{REF}		10	100	µA	
Power supply rejection	V_{DD}		±1/8		LSB	$V_{DD} = 4.75\ V$ to 5.25 V
Logic Inputs						
$\overline{CAZ}$ (pin 1), $\overline{RD}$ (pin 18), $\overline{CS}$ (pin 19), $\overline{WR}$ (pin 20), BYSL (pin 21), A0 (pin 24), A1 (pin 25), $\overline{CAL}$ (pin 26)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	2.4			V	
Input current						
at 25 °C	I_{IN}	−1		1	µA	$V_{IN} = 0$ to V_{CC}
at −40 °C ... 85 °C	I_{IN}	−10		10	µA	
CLK (pin 23)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	3.5			V	
L-input current	I_{IL}	−10		10	µA	
H-input current	I_{IH}			1.5	mA	100 nA max. during standby

Notes see page 18

Characteristics (continued SDA 0812 A)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Logic Outputs						
DB0 to DB7 (pins 10 to 17), BUSY (pin 22)						
L-output voltage	V_{QL}			0.4	V	$I_{SINK} = 1.6$ mA
H-output voltage	V_{QH}	4.0			V	$I_{SOURCE} = 200$ µA
Floating state leakage current (pins 10-17)		−1		1	µA	$V_{OUT} = 0$ V to V_{CC}
Floating state output capacitance	C_Q			15	pF	
Conversion Time						
With external clock						
	t			24	µs	$f_{CLK} = 500$ kHz
	t	6			µs	$f_{CLK} = 2$ MHz
with internal clock	t	7.5			µs	Using recommended clock
($T_A = 25$ °C)	t			38	µs	components as shown in **fig. 4.** See internal clock operation
sampling time	t	2.5			µs	

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity.

2) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full scale errors. Filtering by a low pass ($R = 2$ kΩ, $C = 100$ nF) or use of an external sample-and-hold is required then.

Functional Range

Supply voltage	V_{DD}		5		V	± 5% for specified performance
	V_{CC}		5		V	± 5% for specified performance
Supply current	I_{DD}			2.5	mA	Typ. 1 mA with $V_{DD} = 5$ V
	I_{CC}		1.0	2.0	mA	$V_{IN} = V_{IL}$ or V_{IH}
Power dissipation	P_D		10	25	mW	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH
Power dissipation (Standby Mode)	P_{DSB}		50		µW	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH

Characteristics (SDA 1812 D)

V_{DD} = 5 V ± 5%, V_{CC} = 5 V ± 5%, $V_{DD} \geq V_{CC} \geq +V_{REF}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications T_{min} to T_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Units	Conditions
		min.	typ.	max.		
DC Accuracy						
Resolution		12			Bits	No missing codes guaranteed
Total unadj. error[1]	*TUE*		± 1/2	± 3/4	LSB	All channels AIN0-AIN3
Differential nonlinearity	*DNL*		± 1/4	± 1/2	LSB	
Full scale error (gain error)	*GE*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error	*OFS*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error with $\overline{TH}$ function			± 1/2	± 1	LSB	with internal clock generator or synchronizing $\overline{TH}$ to ext. CLK
Channel to channel mismatch				± 1/4	LSB	
Dynamic Performance[2] [3]						
Signal to noise ratio	*SNR*	69	71		dB	Full scale input sinwave, 1 kHz *f* sampling is 100 kHz
		66	69		dB	Full scale input sinwave 50 kHz *f* sampling is 100 kHz
Total harmonic distortion	*THD*		75		dB	Full scale input sinwave 50 kHz *f* sampling is 100 kHz
Full power bandwidth (−3 dB)	*BW*		4		MHz	
Aperture delay time			5		ns	$\overline{T}$/H pin
Analog Inputs						
Analog input range	*AIN*	$-V_{REF}$		$+V_{REF}$	V	Selected and unselected channels AIN0-AIN3;
Multiplexer						
Settling time			10		ns	
On channel input						
Capacitance	C_{AIN}		50		pF	
ON-Resistance	R_{ON}		2		kΩ	
OFF-Resistance	R_{OFF}		10		MΩ	
Input leakage current						
+25 °C	I_{AIN}			10	nA	
T_{min} to T_{max}	I_{AIN}			100	nA	
On-state bias current			± 5		µA	Depends on analog input voltage

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity
2) *S/N* includes harmonic distortion
3) Sample tested at 25 °C

Characteristics (SDA 1812 D, continued)

V_{DD} = 5 V ± 5%, V_{CC} = 5 V ± 5%, $V_{DD} \geq V_{CC} \geq +V_{REF}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications T_{min} to T_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Units	Test Conditions
		min.	typ.	max.		
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75		V_{DD}	V	(For specified performance)
Negative reference voltage	$-V_{REF}$	0			V	(For specified performance)
Input reference current	I_{REF}			100	µA	$+V_{REF}$ = 5.0 V
Power Supply Rejection						
Supply voltage	V_{DD}		±1/8		LSB	V_{DD} = 4.75 V to 5.25 V
Logic Inputs						
CAZ (pin 1) $\overline{RD}$ (pin 18), $\overline{CS}$ (pin 19), $\overline{WR}$ (pin 20) BYSL (pin 21), A0 (pin 24), A1 (pin 25) $\overline{CAL}$ (pin 26)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	2.4			V	
Input current						
+25 °C	I_{IN}	−1		1	µA	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	I_{IN}	−10		10	µA	
CLK (pin 23)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	3.5			V	
L-input current	I_{IL}	−10		10	µA	
H-input current	I_{IH}			1.5	mA	100 nA max. during standby
Logic Outputs						
DB0-DB7 (pins 10-17), $\overline{BUSY}$ (pin 22)						
L-output voltage	V_{OL}			0.4	V	I_{SINK} = 1.6 mA
H-output voltage	V_{OH}	4.0			V	I_{SOURCE} = 200 µA
Floating state leakage current (Pins 10-17)		−1		1	µA	
Floating state output Capacitance	C_Q			15	pF	V_{OUT} = 0 V to V_{CC}

6

Characteristics (SDA 1812 D, continued)

$V_{DD} = 5\ V \pm 5\%$, $V_{CC} = 5\ V \pm 5\%$, $V_{DD} \geq V_{CC} \geq +V_{REF}$, $-V_{REF} = 0\ V$, DGND = 0 V, AGND = 0 V
$f_{CLK} = 2$ MHz, all specifications T_{min} to T_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Units	Conditions
		min.	typ.	max.		
Conversion Time						
With external clock	t_{ext}	6			µs	$f_{CLK} = 2$ MHz symmetrically
				24	µs	$f_{CLK} = 500$ kHz
With internal clock	t_{int}		6		µs	Using recommended clock components as shown in **figure 4**. See internal clock
Sampling time[1]	t_s	2.5			µs	operation
Power Requirements						
Analog supply voltage	V_{DD}	4.75	5	5.25	V	
Logic supply voltage	V_{CC}	4.75	5	5.25	V	
Analog supply current	I_{DD}		0.75	2.5	mA	$V_{DD} = 5$ V
Logic supply current	I_{CC}		1.0	2.0	mA	$V_{IN} = V_{IL}$ or V_{IH}
Power dissipation	P_D		10	25	mW	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY} =$
Power dissipation (standby)	P_{DSB}		50		µW	Logic HIGH

Note:

1) Ensure the analog input source to load 50 pF during sampling time to required accuracy.

Timing Specifications[1)]

$V_{DD} = 5\ V \pm 5\%$, $V_{CC} = 5\ V \pm 5\%$, $V_{DD} \geq V_{CC} \geq +V_{REF}$, $-V_{REF} = 0\ V$, DGND = 0 V, AGND = 0 V
$f_{CLK} = 2$ MHz, all specifications T_{min} to T_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Units
		min.	typ.	max.	
Min. $\overline{TH}$ LOW pulse width (SDA 1812 D)	$t_{\overline{TH}\,L}$	2.5			µs
AMUX-settling time after programming the input channel	t_{AMUX}		20		ns
$\overline{CS}$ to $\overline{WR}$ setup time	t_1[2)]	0			ns
$\overline{WR}$ pulse width	t_2[2)]	100			ns
$\overline{CS}$ to $\overline{WR}$ hold time	t_3[2)]	0			ns
$\overline{WR}$ to $\overline{BUSY}$ propagnation delay	t_4	20	50	150	ns
BYSL, CAZ valid to $\overline{WR}$ setup time	t_5	100			ns
BYSL, CAZ valid to $\overline{WR}$ hold time	t_6	20			ns
$\overline{BUSY}$ to $\overline{CS}$ setup time	t_7	0			ns
$\overline{CS}$ to $\overline{RD}$ setup time	t_8[2)]	0			ns
$\overline{RD}$ pulse width	t_9[2)]	100			ns
$\overline{CS}$ to $\overline{RD}$ hold time	t_{10}[2)]	0			ns
BYSL, CAZ to $\overline{RD}$ setup time	t_{11}	50			ns
BYSL, CAZ to $\overline{RD}$ hold time	t_{12}	0			ns
$\overline{RD}$ to valid data (bus access time)	t_{13}[3)]		80	150	ns
$\overline{RD}$ to thre-state output	t_{14}[4)]	20		60	ns
Bus relinquish time	t_{15}[5)]		90	180	ns
Data valid to $\overline{WR}$ setup time	t_{16}	100			ns
Data valid to $\overline{WR}$ hold time	t_{17}	20			ns

Notes:

1) All input control signals are specified with $t_r = t_f = 20$ ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
2) The internal $\overline{RD}$ pulse is performed by a NOR wiring of $\overline{CS}/\overline{RD}$. The internal $\overline{WR}$ pulse is performed by a NOR wiring of $\overline{CS}/\overline{WR}$.
3) t_{13} is measured with the load circuits of **figure 11** and defined as the time required for an output to cross 0.8 V or 2.4 V.
4) t_{14} is defined as the time required for the data lines to change three-state, **see figure 11.**
5) t_{15} is defined as the time required for the data lines to change 10%/90% when loaded with the circuits of **figure 11.**

Figure 7
Start Cycle Timing

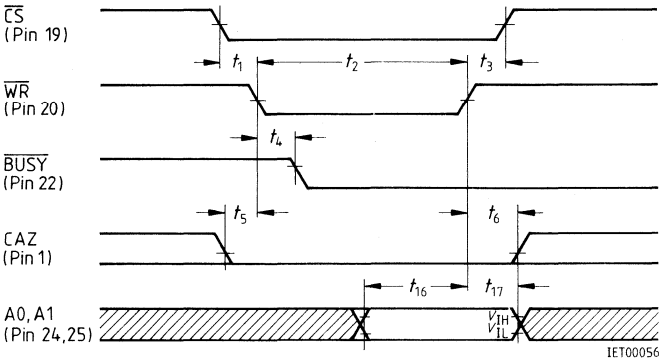
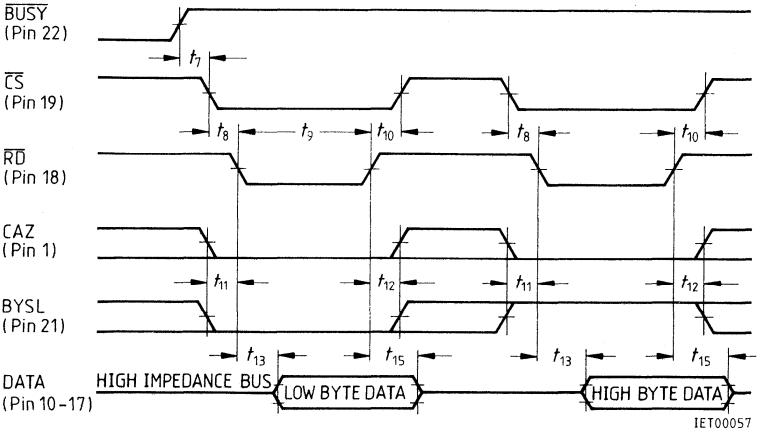


Figure 8
Read Cycle Timing



Notes

The 2-byte conversion result can be read in either order. The figure shows the sequence low byte to high byte. If BYSL changes while $\overline{CS}$ and $\overline{RD}$ are low the data will change to reflect the BYSL input.

Figure 9
Writing to the SFR

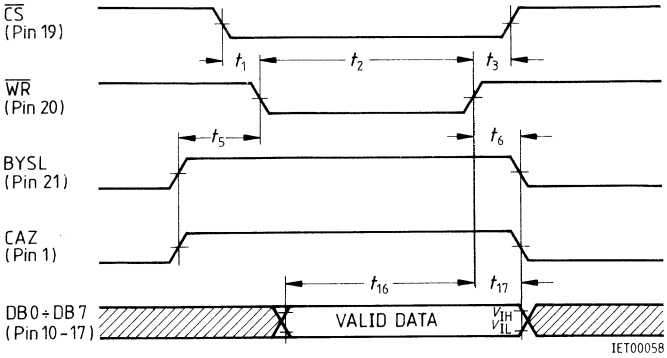


Figure 10
Reading the SFR

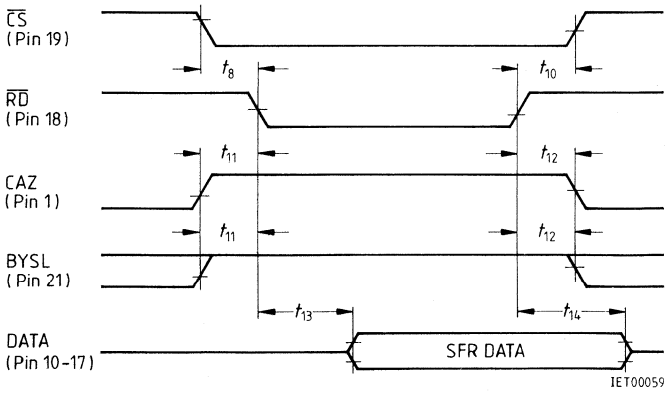
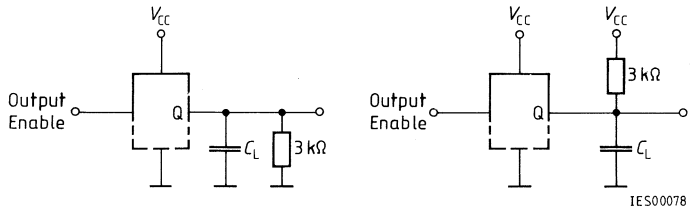
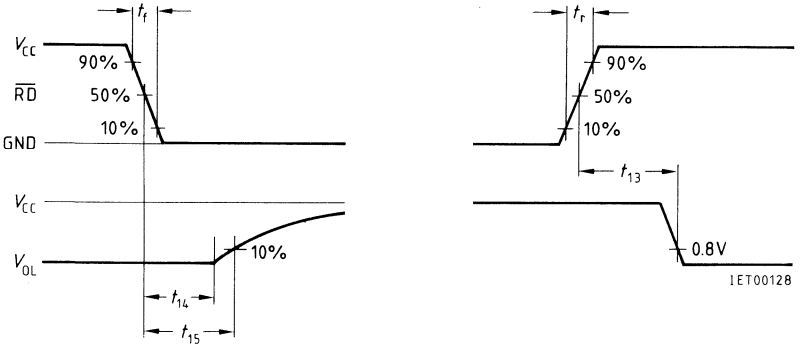


Figure 11
THREE-STATE Test Circuits and Timing Diagrams



C_L = 10 pF

C_L = 50 pF



C_L = 10 pF

C_L = 50 pF

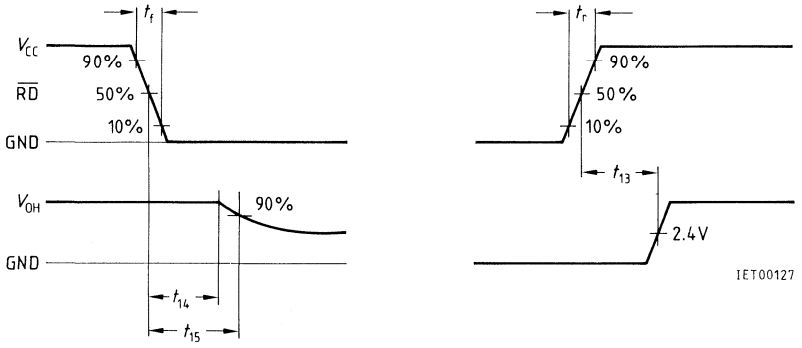


Figure 12

Converter Timing (SDA 0812 A)

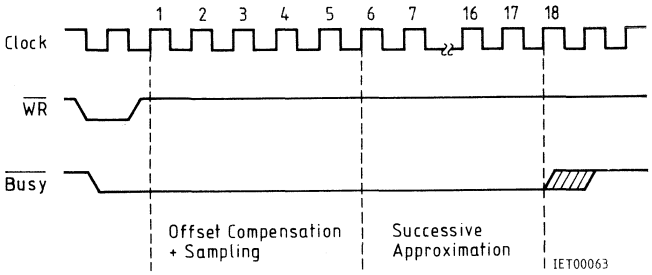


Figure 13

Effective Resolution versus Analog Input Frequency (SDA 0812 A)

$V_{CC} = V_{DD} = +V_{REF} = 5$ V, $-V_{REF} = 0$ V; $f_{CLK} = 1$ MHz

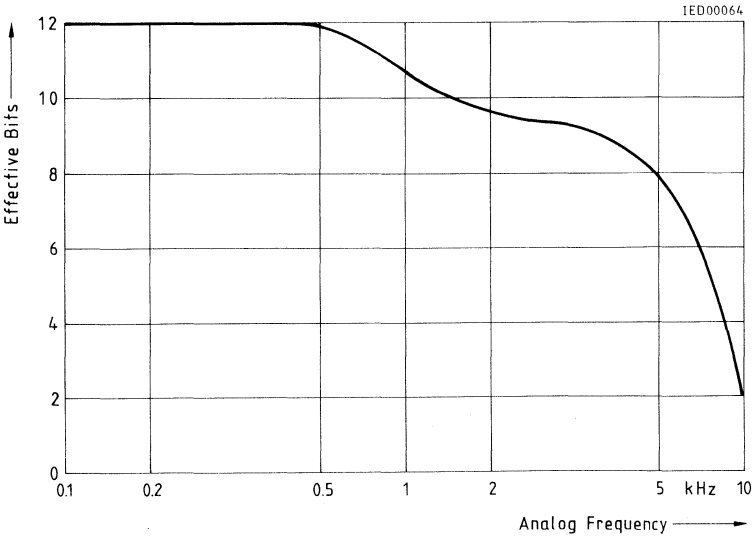
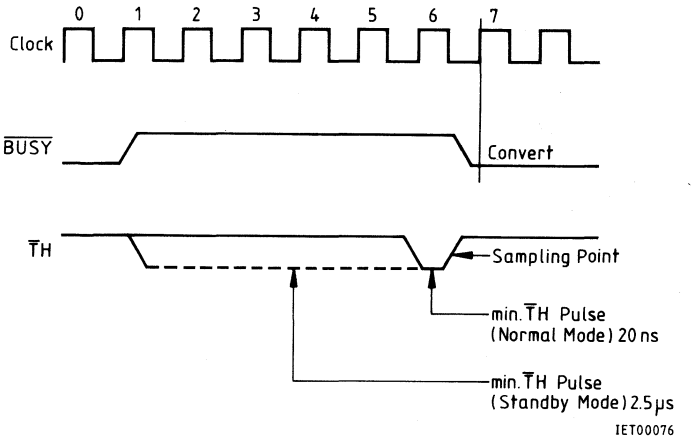


Figure 14
$\overline{TH}$-Timing (SDA 1812 D)



Dynamic Performance (SDA 1812 D)

The SDA 1812 D is specified dynamically as well as with standard DC specifications.

Figures 15 and 16 shows 2048 point FFT plots of the SDA 1812 D with analog input signals of 1 kHz and 50 kHz. When the SNR is calculated it includes harmonics.

Figure 15

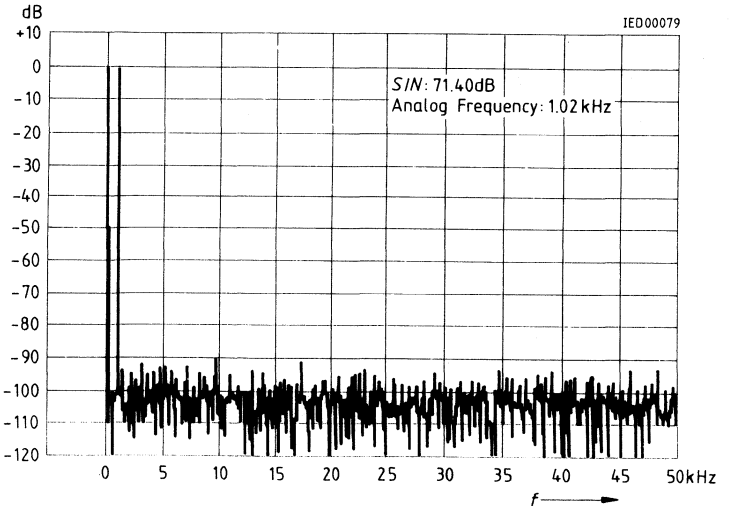
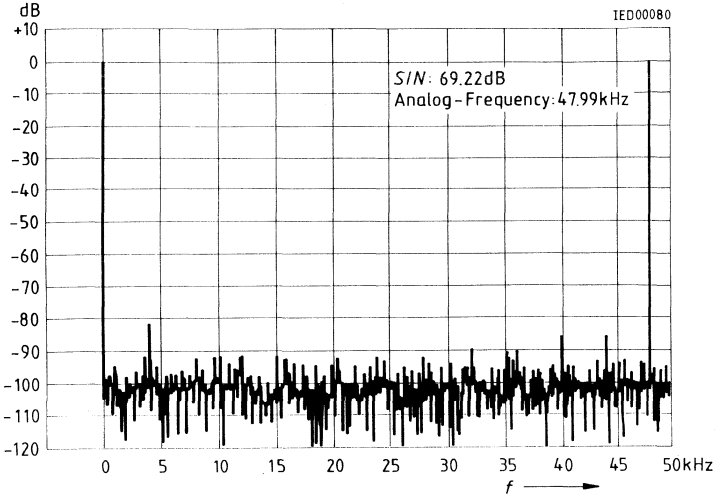


Figure 16

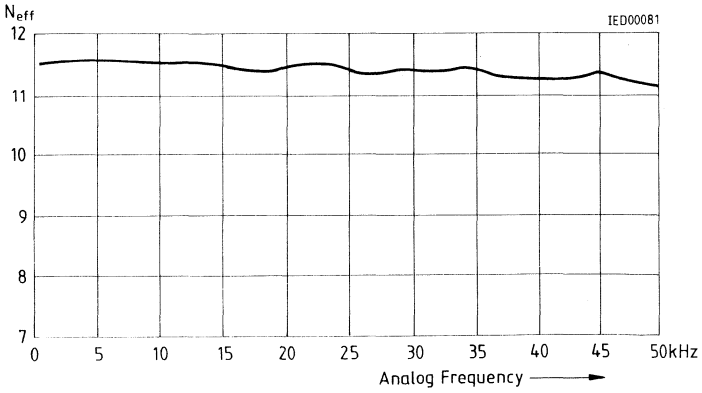


The relationship between Signal-to-Noise Ratio (*SNR* including harmonics) and the resolution of an ideal ADC with no differential or integral linearity errors is expressed in the following equation:

$$N_{eff} = \frac{SNR\ [dB] - 1.76}{6.02}$$

Figure 17

Typ. effective number of bits versus analog input frequency



Microprocessor interfacing

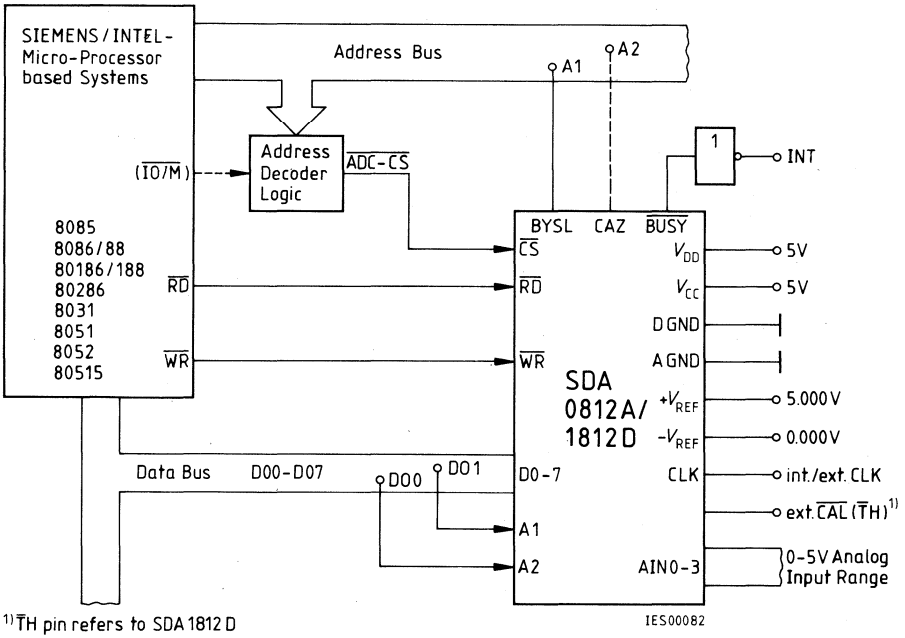
Microprocessor interfacing is straight forward and requires only a few external gates.

SIEMENS/INTEL Microprocessors

A typical interface is shown in **figure 15.**

- Start of Conversion:
  A write instruction selects one of the analog input channels and starts the conversion. Write Address: $\overline{\text{ADC-CS}}$, DATA pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate an interrupt to the microprocessor (INT).
- Read the Conversion Result:
  A read instruction from the $\overline{\text{ADC-CS}}$-address fetches the low byte, a read instruction from $\overline{\text{ADC-CS}}$-address + 2 the high byte.

Figure 18

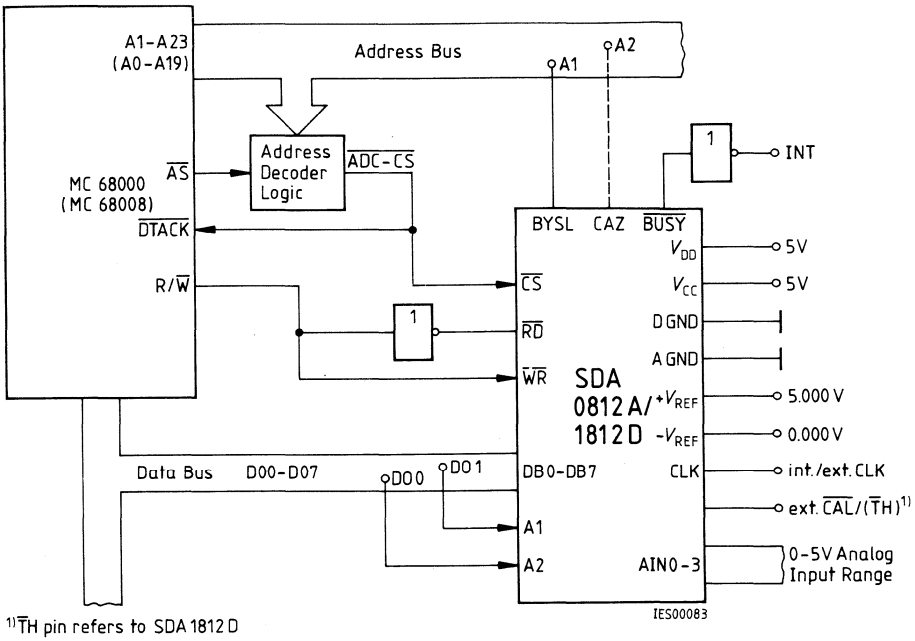


1) TH pin refers to SDA 1812 D

Motorola Microprocessors

A typical interface is shown below

Figure 19



1) TH pin refers to SDA 1812 D

- **Start of Conversion**

  A WRITE instruction to an address decoded by the address decoder logic will start a conversion. The lower 2 bits of the data bus select the input channel. MOVE.W D0, ADC-ADDRESS.

- **Read the Conversion Result**

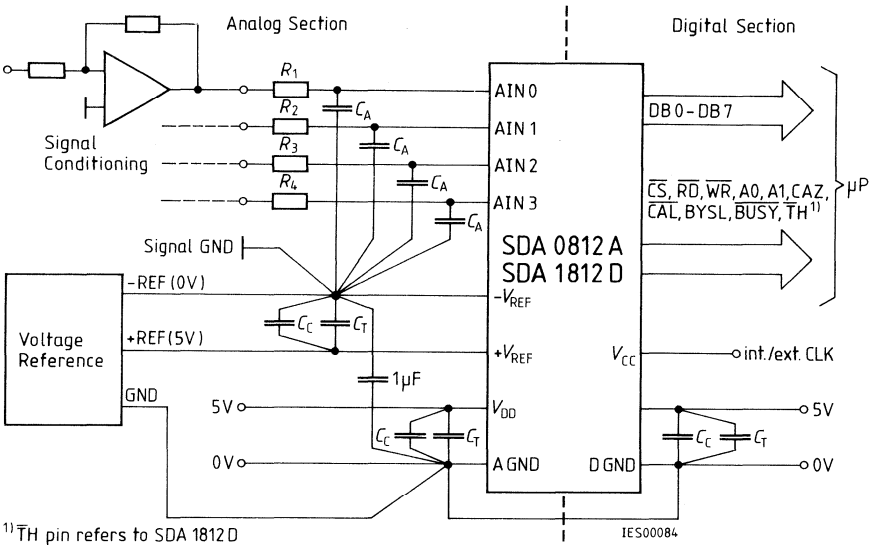
  A READ instruction to the ADC-ADDRESS puts the conversion result to the data bus: MOVE.PW $000 (ADC-ADDRESS), D0 places the 12-bit result of the conversion in the D0 register. The address decoder has to pull down ADC-CS wire at ADC-ADDRESS and ADC-ADDRESS + 2.

  Figure 20 shows how the result is placed in register D0.

Figure 20

		BUSY	0	0	0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Figure 21
Application Hints



1) $\overline{TH}$ pin refers to SDA 1812 D

	SDA 0812 A	SDA 1812 D
C_A	... 5 nF	... 10 nF
C_C	... 10 nF Ceramic	... 10 nF Ceramic
C_T	... 10 µF Tantal	... 10 µF Tantal
$R_1 ... R_4$	... 50 Ω	... 100 Ω

Power Supply Decoupling

The digital respectively analog 5 V power supply should be connected with a 10 µF tantalum capacitor to DGND respectively AGND. To ensure good HF performance this capacitor should be connected in parallel with a 10 nF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Note, that logic supply voltage V_{CC} must not be applied before V_{DD}!

Reference Voltage

To avoid dynamic errors a 10 µF tantalum capacitor connected in parallel with a 10 nF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 1 µF capacitor should be placed between $-V_{REF}$ and AGND.

Analog Inputs

The high input impedance of the analog channels AIN 0 to AIN 3 allows simple analog interfacing. Signal sources $-V_{REF} \leq AIN \leq +V_{REF}$ can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 5 clock cycles.

All converter measurements are done with respect to the reference voltages, analog ground only powers the chip. Therefore $-V_{REF}$ has to be used as the signal ground. The simple RC-filter 50 Ω, 5 nF (100 Ω, 10 nF) is recommended in order to protect the analog input against spikes and noise during the offset compensation period.

Application Note

For operation without any interferences, $+V_{REF}$ must not exceed V_{DD} (see characteristics: $V_{DD} \geq V_{CC} \geq +V_{REF}$), especially not during switching-on. Please start autocalibration using pin CAL after all voltages (V_{DD}, V_{CC}, $+V_{REF}$, $-V_{REF}$) are stable.

Note

Values in brackets refer to SDA 1812 D.

Selector Guide

Type	Package	Function	Page
SAB 0529	P-DIP-18	Programmable digital timer	485
SAB 0529 G	P-DSO-20 (SMD)	Programmable digital timer	485
SAE 0530	P-DIP-18	Programmable timer for 50 Hz line frequency	501
SAE 0531	P-DIP-18	Programmable timer for 60 Hz line frequency	501
SAE 0532 G	P-DSO-20 (SMD)	Timer for 50/60 Hz line frequency switchable	501

Characteristics of Line-Commutated Clock Generators

Type		SAB 0529/G	SAE 0530	SAE 0531	SAE 0532 G
Package		P-DIP-18, P-DSO-20	P-DIP-18	P-DIP-18	P-DSO-20
		same pin configuration			
Line frequency		50 Hz	50 Hz	60 Hz	50/60 Hz switchable
Clock line separated from N pin		no	no	no	yes
Temperature range		0 to 70 °C	−25 to 85 °C		
Response delay at S		for rising edge	for rising and falling edge		
Response delay at R		no	yes		
Timer start behavior when V_S is applied	S = L	no timer start	no timer start		
	S = H	undefined	timer start		
Integrated pull-up resistor to S		no	yes		
Clamping diodes at S		no	yes		
Switching thresholds at A, B, C, S, FC, R		0.6 V	1.8 V		
Switching thresholds at N or FT (SAE 0532)		1.2 V	1.3/1.8 V hysteresis of 0.5 V		
Condition of the pins D to I after reset		L	H		
Output voltage at T at 100 mA		1.8 V	1 V		
Operation as pulse generator		with additional circuit	without additional circuit		

(For further slight deviations refer to characteristics/maximum ratings)

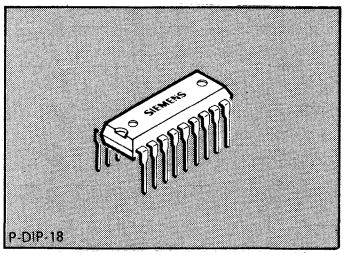
SIEMENS

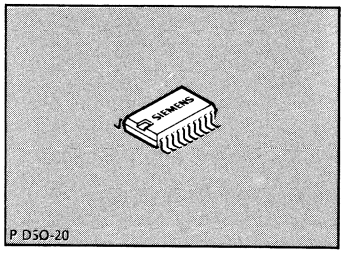
Programmable Digital Timer — SAB 0529

Bipolar IC

Features

- Direct operation from AC line or DC supply possible
- Time base is 50 Hz line frequency
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for resistive, inductive and capacitive loads
- Triac gate trigger current up to 100 mA
- Continuous output current to relay actuation max. 100 mA
- 8 overlapping timing periods between 1 second and 31 1/2 hours (at 50 Hz)
- 2 operating modes: momentary switching or switch off delay, both are retriggerable
- Upon request, delay times can be adjusted to customer's specification, requiring only minimum external components. This is possible through mask programming, but is based on minimum order quantities.





Type	Ordering Code	Package
■ SAB 0529	Q67000-H2176	P-DIP-18
■ SAB 0529 G	Q67000-H2952	P-DSO-20 (SMD)

■ Not for new design.

With the digital timer SAB 0529, delay times between 1 second and 31 1/2 hours can be set. Time base is the 50 Hz line frequency. A triac may be triggered by the SAB 0529 IC.

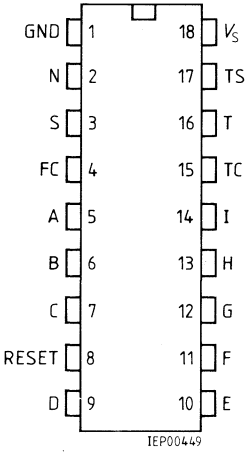
The SAB 0529 can be programmed to two operating modes: "momentary switching" and "switch-off delay" (according to DIN 46120). In the first mode, a rising edge at the start input activates the triac and starts the timing period. In the switch-off delay mode, the rising edge at the start input activates the triac; but the falling edge starts the timing period.

The versatile IC SAB 0529 covers a great variety of applications, e.g. electronic timers, cooking equipment control, espresso machines, hand-driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

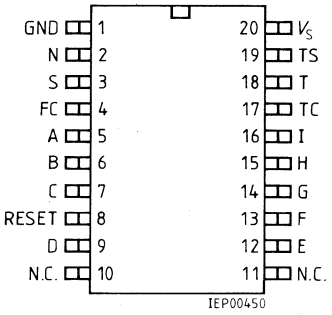
Pin Configurations

(top view)

SAB 0529



SAB 0529 G



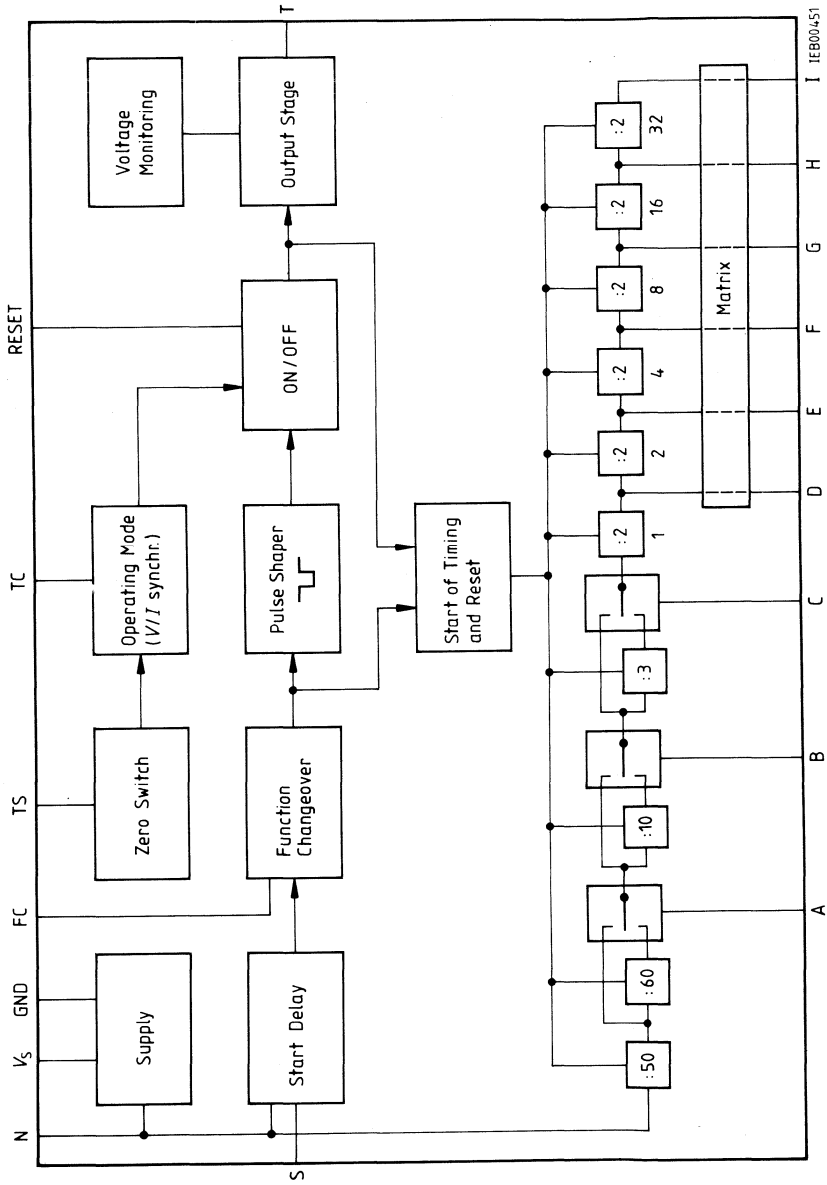
Pin Definitions and Functions

SAB 0529 Pin	SAB 0529 G Pin	Symbol	Function
1	1	GND	Circuit ground
2	2	N	Line voltage via series resistor
3	3	S	Start
4	4	FC	Function changeover
5	5	A	Programming of basic timing unit
6	6	B	Programming of basic timing unit
7	7	C	Programming of basic timing unit
8	8	R	Reset
9	9	D	Basic timing unit x 1
10	12	E	Basic timing unit x 2
11	13	F	Basic timing unit x 4
12	14	G	Basic timing unit x 8
13	15	H	Basic timing unit x 16
14	16	I	Basic timing unit x 32
15	17	TC	Triac operation mode setting
16	18	T	Triac triggering
17	19	TS	Triac synchronization
18	20	V_S	Positive supply voltage

These values apply to the standard SAB 0529 version. By mask programming, each of those pins may be assigned a value between 1 and 63.

With the P-DSO-20-package (SAB 0529 G), pins 10 and 11 are not connected.

Block Diagram



7

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage at impressed dc voltage	V_S	−0.3	5.5	V	
Peak current at N	I_{Np}	−35	35	mA	50 Hz operation
DC from N (rms)	$-I_{Nrms}$		12.5	mA	with $V_S \leq 7.5$ V
AC at N with impressed current	I_{Nrms}		25	mA	50 Hz operation with $V_S \leq 7.5$ V
Voltage at S, FC, A, B, C, R	V	−0.3	7.5	V	
Voltage at N, with N utilized as clock input	V_{NT}	−0.3	V_S	V	
Voltage at TC	V_{TC}	−0.3	V_S	V	
Current at TS	I_{TS}	−4	4	mA	
Voltage at T	V_T	−0.3	7.5	V	
Peak current in T	I_{Tp}		150	mA	1 ms (10 ms interval)
Continuous current in T	I_T		100	mA	
Current in D, E, F, G, H, I	I		0.5	mA	D, E, F, G, H, I on-state
Voltage at D, E, F, G, H, I	V	−0.3	7.5	V	D, E, F, G, H, I off-state
Short-term peak current at N	I_{Np}	−350	350	mA	0.3 ms (100 ms interval) with $C_{ch} > 40$ µF
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance system – air SAB 0529	$R_{th\ SA}$		70	K/W	
SAB 0529 G	$R_{th\ SA}$		105	K/W	

All voltages are referred to pin 0, unless otherwise specified.

Operating Range

Supply voltage at impressed DC voltage Impressed DC or impressed AC at N[2])	V_S	4.5	5.5	V	Voltage between pin 0 and V_S
DC supply from N (rms)	$-I_N$	2,5[1])	12.5	mA	**see application circuit**
AC supply at N (rms)	I_{Nrms}	5[1])	25	mA	**see application circuit**
Ambient temperature	T_A	0	70	°C	

[1]) Only the supply current for the IC, i.e. without triac gate current. The rms gate current additionally flows through N. (The IC may be operated with DC or AC; **see also application circuits)**.

[2]) The voltage between 0 and V_S is between 5.5 V and 7.0 V for impressed AC and between 6.0 V and 7.5 V for impressed DC. Operation, however, is also assured if V_S falls to 4.5 V (e.g. due to ripple at V_S with DC supply).

Characteristics

V_S = 4.5 V to ≤ 5.5 V (7.5 V)[1]), T_A = 0 °C to 70 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply current at V_S and/or N	I_S		1.4	2.5	mA	$I_S = -I_N$
V_S with impressed current at N:						
Impressed ac	V_S	5.5	6.2	7.0	V	$I_{N\,rms}$ = 5 mA
Impressed dc	V_S	6.0	6.8	7.5	V	$-I_N$ = 2.5 mA
Switching threshold at:						
A, B, C, S, FC, R	$V_{A...}$	0.3	0.6	1	V	
N (if N is clock input)	V_N	0.6	1.2	2	V	
TC	V_{TC}		3.5	4.5	V	
TS (for voltages > V_S)	$V_{TS}+$		V_S+1.3		V	
TS (for voltages < V_S)	$V_{TS}-$		V_S–1.3		V	
L-input current at:						
A, B, C, S, FC, R	$-I_{I\,L}$			20	µA	$V_{A...}$ = 0 V
N (if N is clock input)	$-I_{I\,NL}$			40	µA	V_N = 0 V
H-input current at:						
A, B, C, S, FC, R	$I_{I\,H}$			20	µA	$V_{A...} = V_S \leq 5.5$ V
N (if N is clock input)	$I_{I\,NH}$			10	µA	$V_N = V_S$
TC	$I_{I\,TCH}$			50	µA	4.5 V ≤ $V_{TC} \leq V_S$
Pos. switching current at TS	$I_{TS}+$	27	45	81	µA	$V_{TS} = V_{TS}+$
Neg. switching current at TS	$I_{TS}-$	18	30	54	µA	$V_{TS} = V_{TS}-$
L-voltage at D, E, F, G, H, I	V_L			0.3	V	I_L = 0.5 mA
Reverse current at D, E, F, G, H, I	I_H			1	µA	
L-output voltage at T	$V_{Q\,TL}$		1.5	1.8	V	I_T = 1 mA
			1.6	2	V	I_T = 10 mA
			1.8	2.3	V	I_T = 100 mA

[1]) with impressed current at N.

Functional Description

Through division of the line frequency into the portions 1:50, 1:60, 1:10, and 1:3, the basis for 8 timing periods is created. The timing period is selected via inputs A, B, and C, according to the following truth table.

Timing range	A	B	C	Basic timing unit	Max. time at 50 Hz line	
1	L	L	L	1 s	63 s	(approx. 1 min)
2	L	L	H	3 s	189 s	(approx. 3 min)
3	L	H	L	10 s	630 s	(10.5 min)
4	L	H	H	30 s	1890 s	(31.5 min)
5	H	L	L	1 min	63 min	(approx. 1 hr)
6	H	L	H	3 min	189 min	(approx. 3 hrs)
7	H	H	L	10 min	630 min	(10.5 hrs)
8	H	H	H	30 min	1890 min	(31.5 hrs)

L and H potentials are referred to terminal 0, e.g. L = 0, H = V_S

The time basis of the set period is multiplied by the corresponding value in the flipflops 1, 2, 4, 8, 16, 32.

The delay time at output T results from connecting a terminal between D and I with terminal R. Should several of the pins D to I be connected to R, the corresponding delay times are added.

Reset during a timing period is accomplished by interrupting the connection to *R*, or by applying an H potential to R (in the latter case a protective resistor between R and D through I is necessary as those pins are not protected against short circuit to V_S), or by turning on and off V_S.

Application Hint

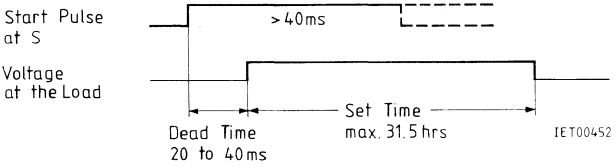
If R is connected to one of the pins D through I via a multiposition switch, and if during the changeover a reset of the timing period is to be avoided, a suitable capacitor is required between R and 0.

With the **connection of the supply voltage,** the circuit is automatically reset. A timing period does not commence if 0 potential is applied to S.

The SAB 0529 allows two operating modes to be set via pin FC (function changeover):

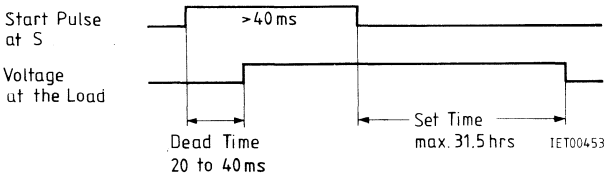
1. **"Momentary Switching Function"** in accordance with DIN 46120

   The triac at pin T turns on with the rising edge at the start input S and turns off when the set time has passed, independent of the start pulse length.



2. **"Switch-Off Delay"** in accordance with DIN 46120

   The triac turns on with the rising edge at S. The falling edge at S starts the timing period. The triac remains in on-state until the set period has passed.



To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms for its positive switching edge, depending on the phase of the 50-Hz line.

Both operating modes are **retriggerable** during the timing period.

Function Changeover

FC	Function
L	momentary switching
H	switch-off delay

Triac Stage

Pin TS (triac synchronization) is the input of a zero voltage switch and serves to synchronize the output T (open collector) with the load voltage or the load current.

With $V_S < 3$ V, the output current is disconnected.

The input TC has a double function:

- to change TS over to voltage synchronization
- to adjust the triac trigger pulse width (by connecting a capacitor C_e to TC) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operating Mode 1

TC to V_S: Output T is connected to the zero voltage switch. T operates when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$.

Is utilized in case of voltage synchronization; **see application circuit 1** (operation with resistive load) and **pulse diagram.**

Operating Mode 2

TC via C_e to Q: Output T is connected to the zero voltage switch via a monoflop. If $V_S - 1.3$ V has fallen below or $V_S + 1.3$ V exceeded at TS, the output T releases a triac gate trigger pulse determined by C_e.

Is utilized in case of current synchronization; **see application circuit 2** and **pulse diagram.**

Operating Mode 3

TC and TS to V_S: Output T conducts after release of start pulse.

Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac **(see application circuits 3, 4, 5).**

Operation with Line Voltage

A series resistor R_s and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_s (anode to N), the rms current consumption is halved. The series resistor may also be an *RC* network **(see application circuit 6).**

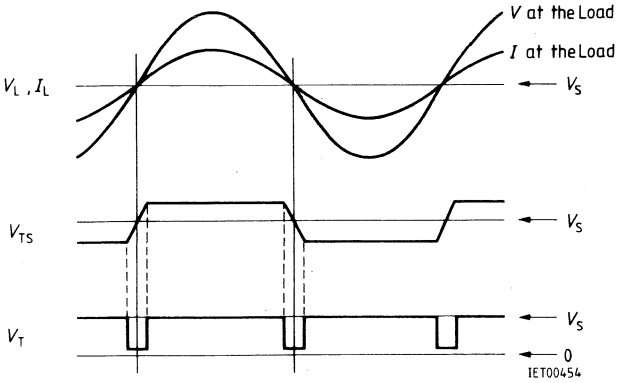
Operation with DC Voltage

This IC can also be operated with dc voltage or current **(see application circuits 4 and 5).**

Pulse Diagrams for Triac Operation Modes 1 and 2

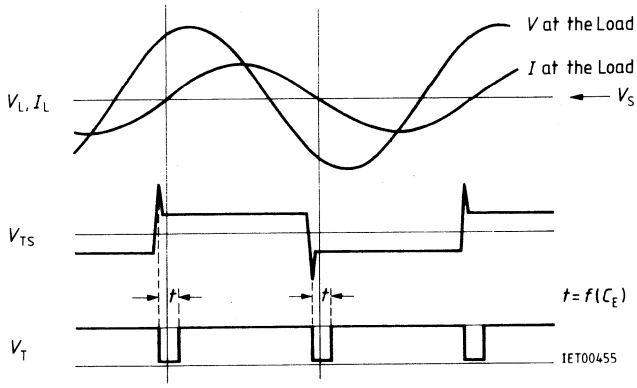
Operating Mode 1

Voltage synchronization with resistive loads (TC to V_S)



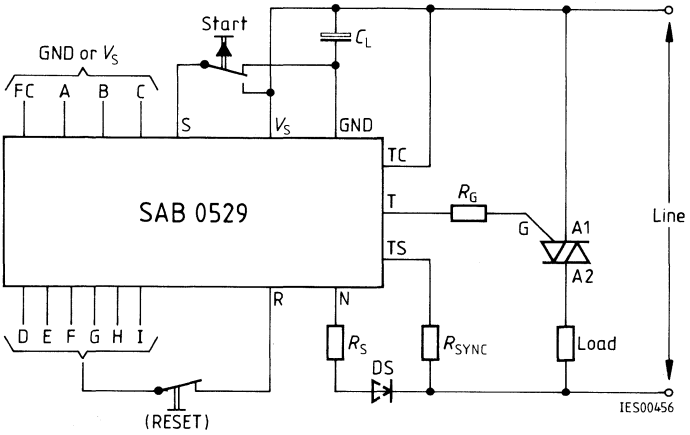
Operating Mode 2

Current synchronization with nonresistive loads (capacitance C_e to TC)

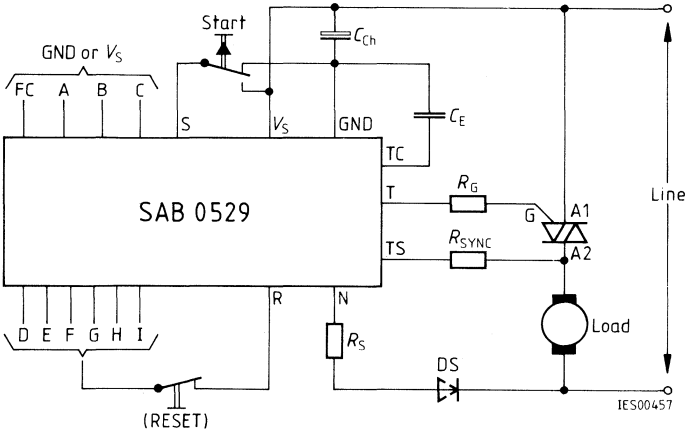


Application Circuits

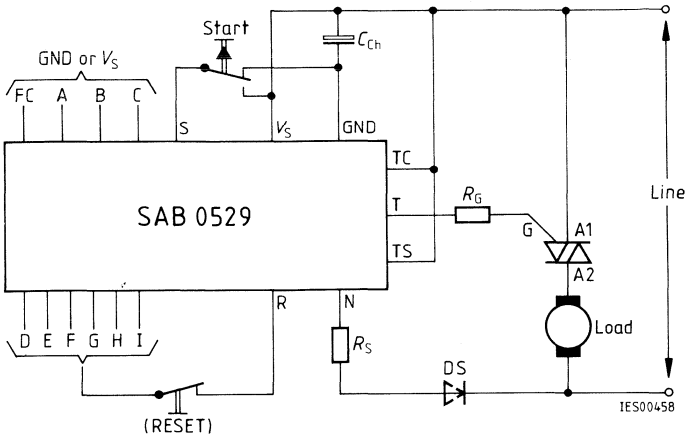
1. Operation with Resistive Loads



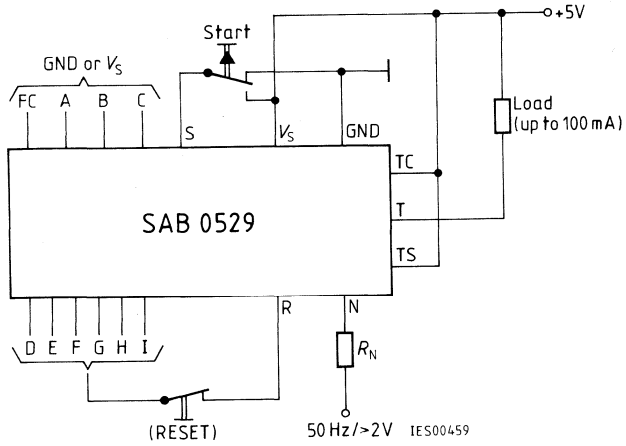
2. Operation with Resistive, Capacitive, or Inductive Loads



3. Operation with any Load and Continuous Triac Triggering

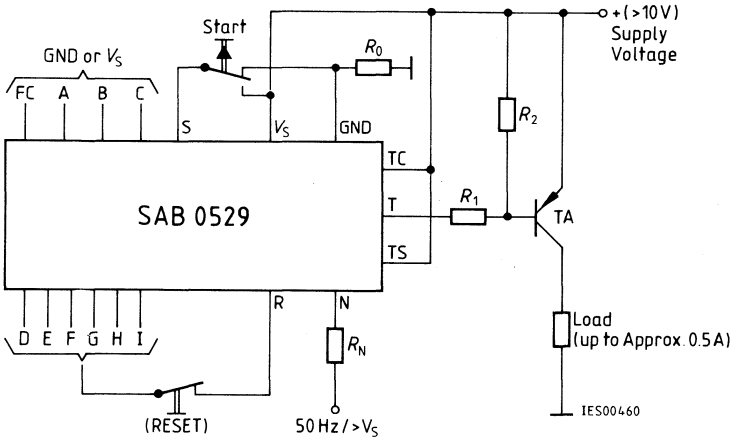


4. Operation with 5 V DC Voltage



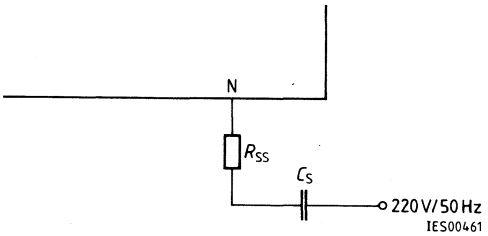
Note: The diode D in **application circuits 1 to 3** must not necessarily be used. This diode, however, may halve the power dissipation at R_S.

5. Operation with DC Voltage > 10 V (limited only by transistor TA)



6. Operation with Capacitive Series Resistor

In the **application circuits 1 to 3,** a series connection of R and C may be utilized instead of R_s or R_S and D.



Note: If not required, the reset key may be omitted in **application circuits 1 to 5.**

Dimensioning the Application Circuits

The following formulae give reference values for operation with sine-shaped ac voltages of 50 Hz. The triac is always triggered in the 2nd and 4th quadrant (negative gate trigger current).

Trigger pulse length Z: $Z = \frac{5 \text{ x holding current}}{\text{rms load current}}$ (ms); applies to $Z \leq 1$ ms

$$R_G = \frac{V_S - V_{ATL} - \text{gate trigger voltage}}{\text{gate trigger current}}$$

$$R_s = \frac{0.5 \text{ x rms line voltage} - V_S}{I_S + \text{average gate trigger current}}$$ (with or without diode D)

average gate trigger current = gate trigger current x $\frac{Z}{10}$ (Z in ms)

Power dissipation at R_s:

$$\text{(without diode D)} = \frac{(\text{rms line voltage})^2}{R_s}$$

$$\text{(with diode D)} = 0.5 \text{ x } \frac{(\text{rms line voltage})^2}{R_s}$$

$$C_{ch} = 20 \text{ x } \frac{\text{rms line voltage}}{R_s}$$ (µF, V, kΩ)

(residual ac voltage at $V_{Spp} \leq 0.5$ V)

Note for C_{ch}

If short-term line failures are to be compensated, C_{ch} has to be accordingly larger (approx. 1000 µF for ≤ 5 s line failure).

Application Circuit 1 (voltage synchronization for resistive load)

$$R_{SYNC} = \frac{0.22\ Z \text{ x rms line voltage} - 1.3}{0.04} \geq \frac{\text{peak line voltage}}{4}$$ (kΩ, V, mA, ms)

Notes for Application Circuit 1

An average I_{TS} of 0.04 mA was inserted into the formula approximating R_{SYNC}.

As $I_{TS}+$ and $I_{TS}-$ contain production deviations, utilizing the determined R_{SYNC} requires certain tolerances to be taken into account for pulse length Z.

To minimize the effect of these tolerances, a resistor may be connected between V_S and TS, which generates a constant current of $\frac{V_{TS}}{R}$ to be added to I_{TS}.

However, a TC of −4 mV/K should be noted for V_{TS}.

Application Circuit 2 (current synchronization)

$C_e = 22 \times Z$ (nF, ms)

$$R_{SYNC} \geq \frac{\text{max. on-state voltage} - 1.3}{I_{TSmin}}$$

$$R_{SYNC} \geq \frac{\text{peak line voltage}}{4}$$

The largest value applies (kΩ, V, mA)

$$R_{SYNC} \leq \frac{\text{gate trigger voltage} - 1.3}{I_{TSmax}} \quad \text{(kΩ, V, mA)}$$

Notes for Application Circuit 2

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the holding current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering.

The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYNC} and should not exceed 20 V.

Application Circuit 3

Dimensioning of R_S, R_G, and C_{ch} as described at the beginning of this section.

Application Circuit 4

$R_N \approx 15 \times$ ac voltage (50 Hz) (kΩ, Vrms)

Application Circuit 5

R_N see above. The AC voltage for the timing base must be greater than (supply voltage −4.8 V).

$$R_0 = \frac{\text{supply voltage} - 6.8\ \text{V}}{I_S + I_{R1}} \qquad I_{R1} = I_{B(TA)} + I_{R2}$$

$$R_1 = \frac{6.8\ \text{V} - V_{QTL} - V_{B(TA)}}{I_{R1}} \qquad I_{R2} \approx 0.05\ I_{B(TA)}$$

$$R_2 = \frac{V_{B(TA)}}{I_{R2}}$$

Application Circuit 6

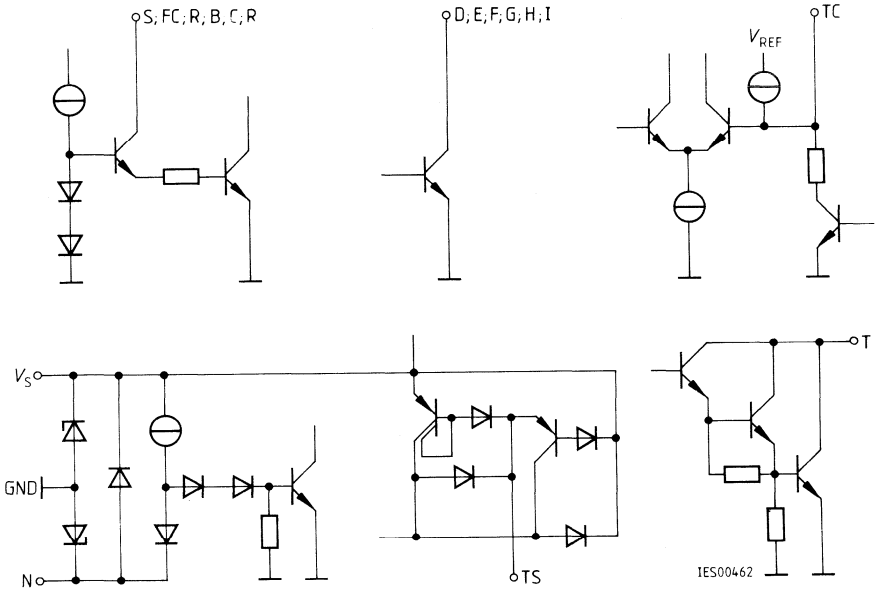
$$C_s = \frac{3.5}{R_s}\ (\mu\text{F, k}\Omega)$$

$$R_{ss} = 0.2\ R_s$$

applies to 50 Hz

To limit the inrush current, R_{ss} has to be $\geq 0.2\ R_s$. Otherwise, the circuit may be damaged.

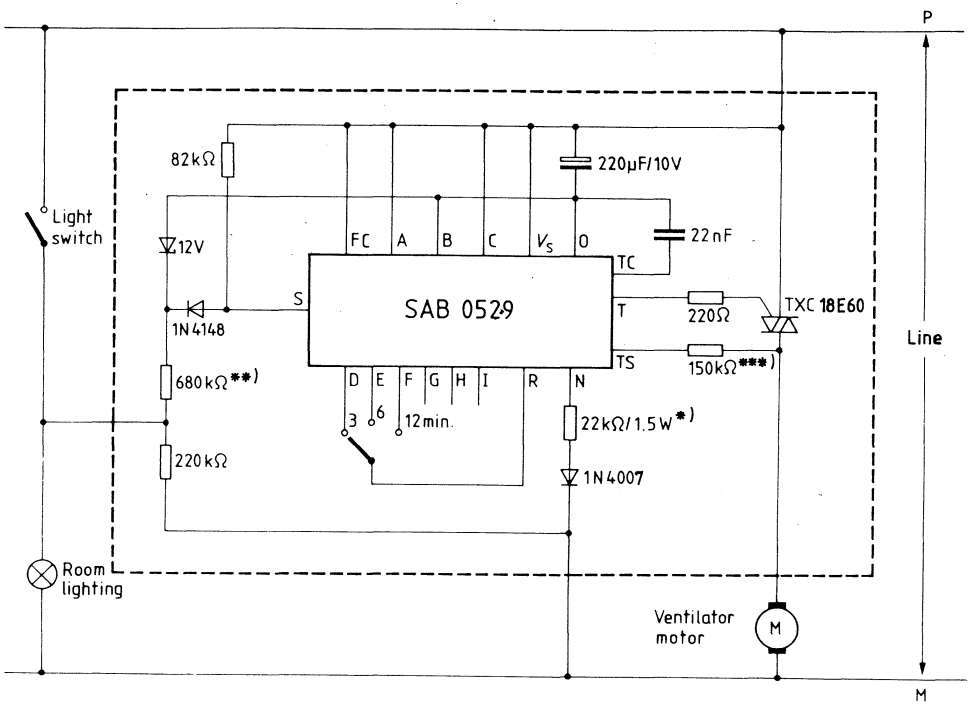
Internal Connection of Inputs, Outputs, and Supply Pins



7

Typical Application

Time control for ventilator motor, adjustable to 3, 6, or 12 minutes' ventilation



*) for 220 Vac, 10 kΩ for 110 Vac;
**) for 220 Vac, 330 kΩ for 110 Vac;
***) for 220 Vac, 82 kΩ for 110 Vac;
} (high-voltage proof)

SIEMENS

Programmable Timer

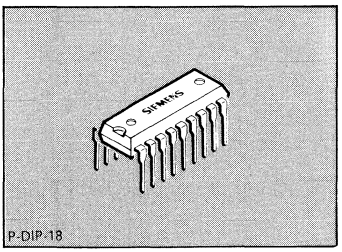
SAE 0530
SAE 0531
SAE 0532

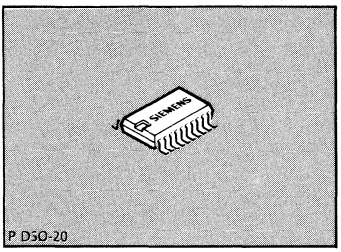
Bipolar IC

Preliminary Data

Features

- Direct operation from AC line or DC supply
- Time base: 50/60 Hz line frequency or any clock frequency up to 10 kHz
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for inductive and capacitive loads
- Triac gate trigger current up to 150 mA
- Continuous output current for relay actuation
- (max. 100 mA)
- Input and output delay can be retriggered
- 8 overlapping timing periods between 1 second and 32.5 hours
- Extended temperature range: −25 °C to 85 °C





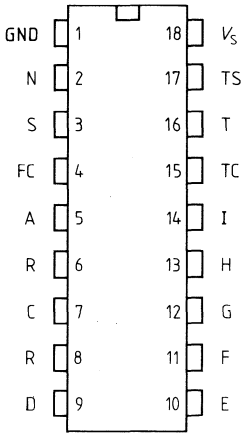
7

Type	Ordering Code	Package	Line Frequency
SAE 0530	Q67000-H8403	P-DIP-18	50 Hz
SAE 0531	Q67000-H8431	P-DIP-18	60 Hz
SAE 0532 G	Q67000-H8432	P-DSO-20 (SMD)	50/60 Hz

With these programmable timers (50 Hz, 60 Hz, 50/60 Hz, respectively) delay times between 1 second and 31.5 hours can be set. Among other purposes they serve for triggering triacs in an AC line. The power may be supplied either by the AC line or by a DC source. The time base is the line frequency. The versatile programmable timers can be imployed in a great variety of applications, such as electronic timers, cooking equipment control, espresso machines, hand driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

Pin Configurations

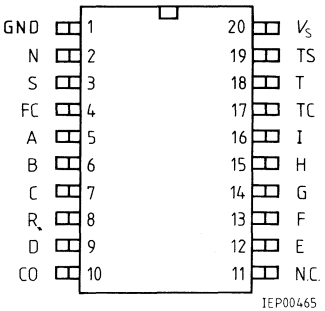
SAE 0530
SAE 0531



IEP00464

Pin Configuration

SAE 0532 G

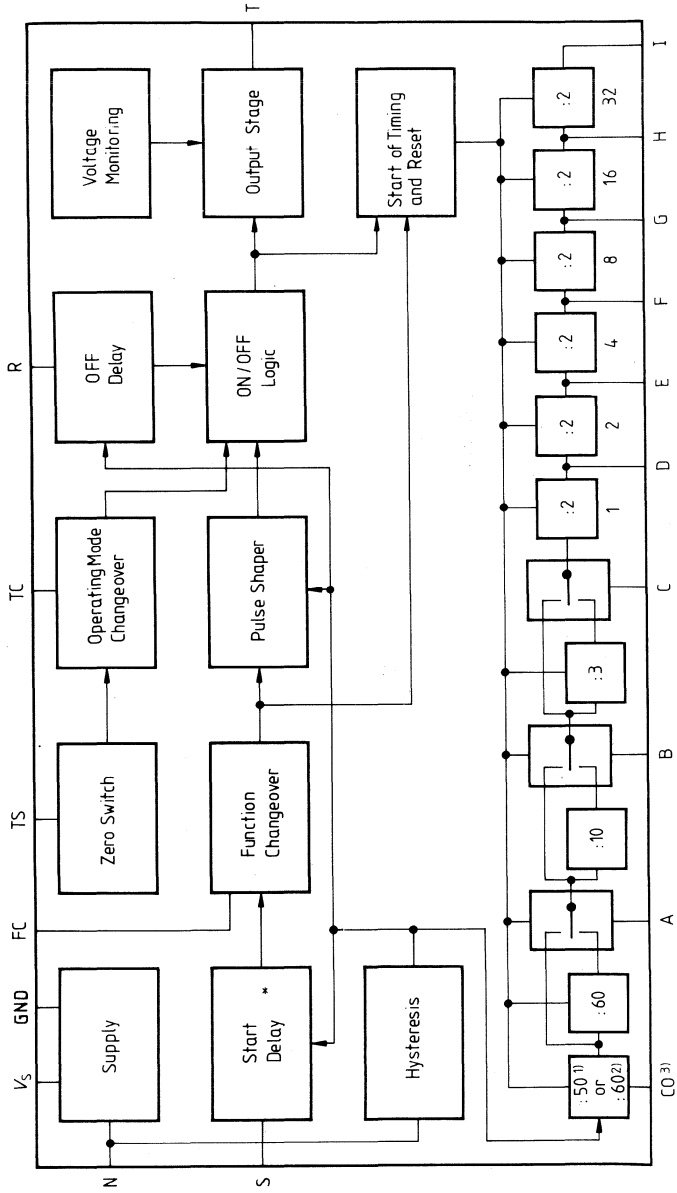


IEP00465

Pin Definitions and Functions

SAE 0530 SAE 0531			SAE 0532 G		
Pin	**Symbol**	**Function**	**Pin**	**Symbol**	**Function**
1	GND	Circuit Ground	1	GND	Circuit Ground
2	N	Line voltage	2	N	Line voltage
3	S	Start	3	S	Start
4	FC	Function changeover	4	FC	Function changeover
5 6 7	A B C	Programming of basic timing unit	5 6 7	A B C	Programming of basic timing unit
8	R	Reset	8	R	Reset
9	D	Basic timing unit x 1	9	D	Basic timing unit x 1
10	E	Basic timing unit x 2	10	CO	50/60 Hz changeover
11	F	Basic timing unit x 4	11	N.C.	not connected
12	G	Basic timing unit x 8	12	E	Basic timing unit x 2
13	H	Basic timing unit x 16	13	F	Basic timing unit x 4
14	I	Basic timing unit x 32	14	G	Basic timing unit x 8
15	TC	Triac op. mode setting	15	H	Basic timing unit x 16
16	T	Triac triggering	16	I	Basic timing unit x 32
17	TS	Triac synchronization	17	TC	Triac op. mode setting
18	V_S	Positive supply voltage	18	T	Triac triggering
			19	TS	Triac synchronization
			20	VS	Positive supply voltage

Block Diagram



* for positive and negative edge

1) Refers to SAE 0530/SAE 0532 G
2) Refers to SAE 0531/SAE 0532 G
3) Refers to SAE 0532 G

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Functional Description

Programming of Delay Times

On input N there is a Schmitt trigger for detecting the clock signal plus rectifier and Z diodes for deriving the operating voltage from the clock source (e.g. line voltage).

The clock signal is applied to a basic divider (1:50 or 1:60) to generate a seconds clock from the line frequency, three switchable dividers (1:60, 1:10 and 1:3) for setting the basic timing and six 1:2 dividers with open-collector outputs. The set time will have expired when the appropriate outputs go high. The basic-timing dividers are controlled by the wiring of inputs A, B and C (and CO)*. At 50 or 60 Hz clock frequency it is possible to set the following basic timing:

Changeover (SAE 0532 G)

CO	Line frequency
L	60 Hz
H	50 Hz

Timing range	A	B	C	Basic timing	Max. time
1	L	L	L	1"	1'3"
2	L	L	H	3"	3'9"
3	L	H	L	10"	10'30"
4	L	H	H	30"	31'30"
5	H	L	L	1'	1h3'
6	H	L	H	3'	3h9'
7	H	H	L	10'	10h30'
8	H	H	H	30'	31h30'

L: connected to 0; H: connected to V_S

The basic timing of the set range is doubled in flipflops 1, 2, 4, 8, 16 and 32. The flipflops are connected to pins D, E, F, G, H and I so that the latter adopt a certain value, i.e. 1, 2, 4, 8, 16 and 32. The required delay time on output T (triac driver) is calculated by the following equation: delay = basic timing x value D through I. This time is then produced by connecting the appropriate pins D through I to pin R (reset). If a number of the outputs D through I are connected to R, the times add up.

* Information in parentheses apply to SAE 0532 G.

Functional Description (cont'd)

Output	Period	Contribution to delay
D	2 x basic timing	1 x basic timing
E	4 x basic timing	2 x basic timing
F	8 x basic timing	4 x basic timing
G	16 x basic timing	8 x basic timing
H	32 x basic timing	16 x basic timing
I	64 x basic timing	32 x basic timing

Example:

Line frequency 50 Hz (SAE 0530/31G) or 60 Hz (SAE 0531/32); set range 1 (basic timing = 1 s); D, F and I connected to R (value = 37): so the delay is 37 s.

Types of Delay

The circuit permits two different functions, which are selected on pin FC (function changeover). The two functions can be retriggered while the timing is running.

1. Turn-on interval DIN 46120 **(Figure 1)**
   The triac connected to T turns on with the rising edge on the start input S and off when the set time has elapsed, and does this independently of the length of the start pulse. The effect of noise pulses on the start input is minimized by the dead times.
2. Dropout delay to DIN 46120 **(Figure 2)**
   The triac turns on with the rising edge on S. The falling edge on S triggers the timing. The triac remains turned on until the set time has expired.

FC	Function
L	Turn-on interval
H	Dropout delay

Figure 1
Turn-On Interval

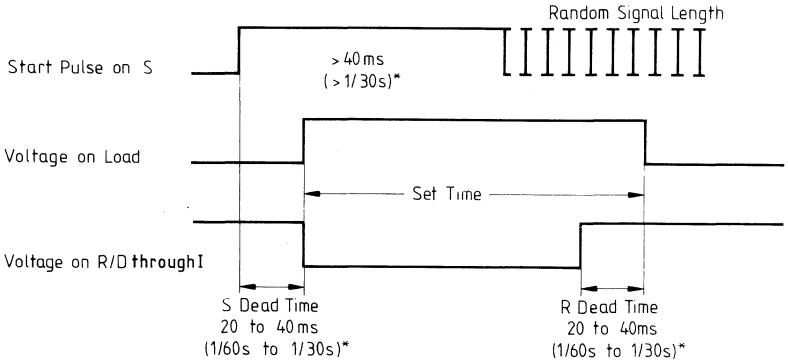
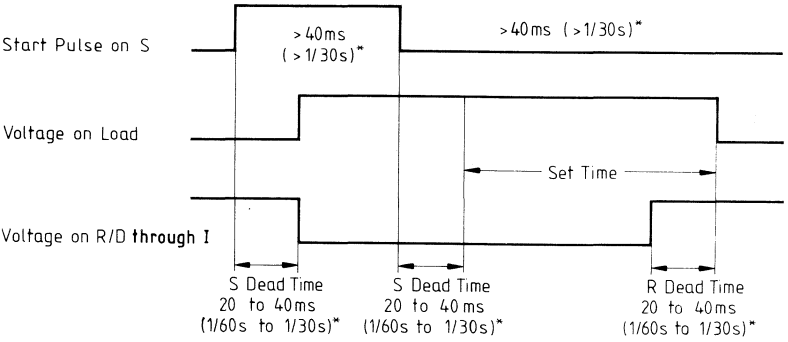


Figure 2
Dropout Delay



* Figures in parentheses apply to SAE 0531/32 G in 60-Hz mode.

Functional Description

Start of Time Measurement (Figure 1, 2)

The frequency divider (and thus the time measurement) is started

- for the turn-on interval function (FC = L) with start input S = H by two negative edges on N,
- for the dropout delay function (FC = H) with S = H during at least two negative edges on N and then S = L by two more negative edges on N.

New Start of Time Measurement and Counter Reset

If, with the reset input R = L, the start input S is toggled (observing the condition: at least two negative edges on N), the time measurement is started again each time (retrigger function). When R = H and there are two negative edges on N, the counter is reset (reset function). This clocked control ensures a large degree of resistance to noise pulses that are coupled in. The reset function is also enabled by turning on the supply voltage, because the IC has a startup circuit. But this only takes effect if the preceding interruption of the supply voltage was long enough (in the region of a few ms). This avoids reset caused by interference on the supply voltage.

Output Stage

The output stage is also controlled by S and R. The open-collector output T is enabled by S = H and disabled by R = H when there are two negative edges on N (and when the supply voltage is turned on).

If start input S and reset input R are high at the same time, the output is enabled by the second negative edge and turned off again by the next positive edge (as long as R has not gone low in the meantime, as is usually the case). If the operating voltage drops below the operating limit of the circuit (approx. 3 V), the output is turned off for this duration.

Functional Description (cont'd)

Triac Modes (Figure 3, 4)

Different modes can be set for the enabled output by appropriate wiring of inputs TC (triac mode) and TS (triac synchronization):

- Mode 1 (TC on V_S) (voltage synchronization)
  Output T is connected to the zero-voltage switch. T conducts when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$; **see Application Circuit 1** (operation of resistive loads).
- Mode 2 (TC via C_e on GND or open) (current synchronization)
  Output T is connected to the zero-voltage switch via a monoflop. T issues a driving pulse, determined by C_e, when $V_S - 1.3$ V is no longer maintained on TS or $V_S + 1.3$ V is exceeded; **see Application Circuit 2.**

  In the current-synchronization mode, gate-trigger current is supplied to T until the triac has fired. If the triac does not fire because the load current is too small, the trigger current flows permanently, which can lead to a drop in the supply voltage. In this way the current is reduced further and the supply voltage continues to drop until ultimately the output is turned off because the lower limit of the operating voltage is reached. The circuit remains in this state until T is finally disabled by the timing control. This process can be avoided by ensuring that the triac fires in all operating conditions.
- Mode 3 (TC and TS on V_S)
  Output T conducts after the start pulse. This is used for any load in continuous driving of the triac (e.g. at low power levels) or if, instead of the triac, another load is operated; **see Application Circuits 3, 4 and 5.**

Inputs N, S, R, FC, A, B, C (and CO)* have an internal pullup resistor, i.e. they are high if not wired. On start input S there are also clamping diodes to V_S and GND so that it is possible to start with external potential. Reset input R is usually connected to one or more of the open-collector outputs D through I, enabling cutout of the load and resetting of the counter when the set delay has elapsed. These outputs are turned off (R = H) in their basic state (after reset), conduct when the time measurement starts (R = L) and are turned off again (R = H) after the delay **(see Figure 1 and 2)**.

* Figures in parentheses apply to SAE 0532 G.

Operation with Line Voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC network **(see Application Circuit 6).**

Operation with DC voltage

This IC can also be operated with DC voltage or current **(see Application Circuits 4 and 5)**.

Useful Hints

- To obtain better noise immunity the pins D through I which are not connected are to be applied to GND.

- C_L
  If short-term line failures are to be compensated, C_L has to be accordingly higher.

- **Application Circuit 1** (voltage synchronization for resistive load)
  An average I_{TS} of 0.025 mA was inserted into the formula approximating R_{SYN}. As I_{TS+} and I_{TS-} contain production deviations, utilizing the determined R_{SYN} requires certain tolerances to be taken into account for pulse length Z.

- **Application Circuit 2** (current synchronization)
  In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the hold current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering. The noise band and/or the noise amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYN} and should not exceed 20 V.

- **Application Circuit 6**
  To limit the inrush current, R_{SS} has to be $\geq 0.2\ R_S$. Otherwise, the circuit might be destroyed.

- **Application Circuit 9**
  If the delay is made selectable by using a mechanical switch, it should be noted that all inputs, because of the pullup, are high in an unwired condition.

  Brief interruptions can be made ineffective by wiring with a capacitor. On S and R there is extra protection through the clocked control with a decision interval of one to two clock cycles.

Figure 3
Pulse Diagrams for Triac Operating Modes 1 and 2

Operating Mode 1: Voltage synchronization with resistive loads (TC at V_S)

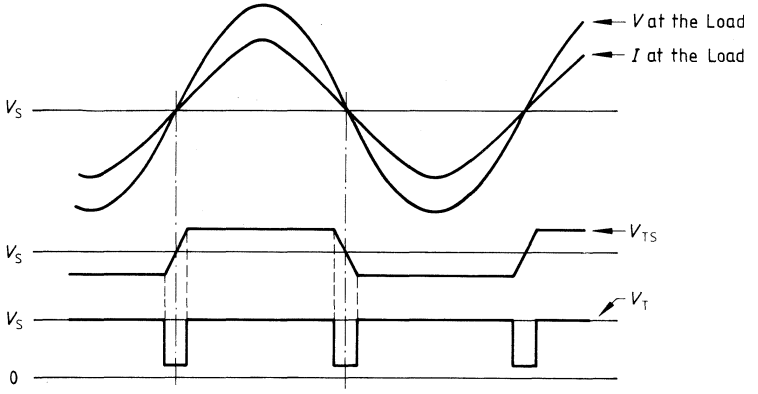
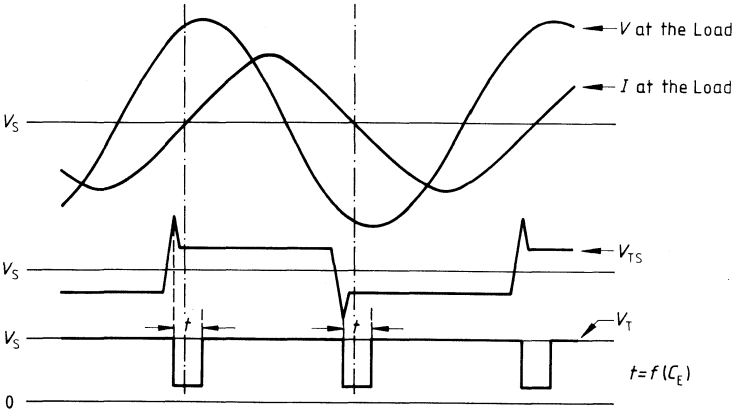


Figure 4
Operating Mode 2: Current synchronization with non-resistive loads
(Capacitance C_e at TC)



Absolute Maximum Ratings

$T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage[1])	V_S	−0.3	5.5	V	
AC at N[2]) DC from N[2]) Peak current at N[2])	$I_{N\,rms}$ $-I_N$ I_{Np}	 −18 −200	35 18 200	mA mA mA	RMS value Average value 2 ms, 100 ms interval
Voltage at A, B, C, FC, N, R, S, TC, CO Voltage at D, E, F, G, H, I, T Voltage at TS	$V_{A...}$ $V_{D...}$ V_{TS}	−0.3 −0.3 $V_S - 0.7$	$V_S + 0.3$ 20 $V_S + 0.7$	V V V	 D...T off-state
Current in D, E, F, G, H, I Current at S[3]) Continuous current in T Peak current in T Current at TS	$I_{D...}$ I_{IS} I_T I_{Tp} I_{TS}	 −2 −4	0.5 2 100 150 4	mA mA mA mA mA	D...I on-state T on-state 1 ms / 10 ms interval
Junction temperature Storage temperature range Thermal resistance system – air	T_j T_{stg} $R_{th\,SA}$ $R_{th\,SA}$	 −55 	125 125 70 90	°C °C K/W K/W	 P-DIP-18 P-DSO-20

Operating Range

Supply voltage[4])	V_S	4.5	5.5	V	
Supply current (DC)[4]) Supply current (AC)[4])	$-I_N$ $I_{N\,rms}$	2.5 5	18 35	mA mA	[5]) [5])
Ambient temperature	T_A	−25	85	°C	

Notes

1) with impressed voltage at V_S
2) with impressed current at N
3) with impressed current at S
4) The IC can be operated with impressed voltage or with impressed current. With impressed voltage at V_S the voltage that is applied can be between 0 and $V_{S\,max}$ V (see maximum ratings).
With impressed DC or AC at N, V_S is internally limited and thus ranges between 6 and 8.2 V (typ. 7.5 V). Operation, however, is also ensured if V_S falls to 4.5 V.
5) Only supply current for I_S, i.e. without triac gate current. The rms gate current additionally flows through N.

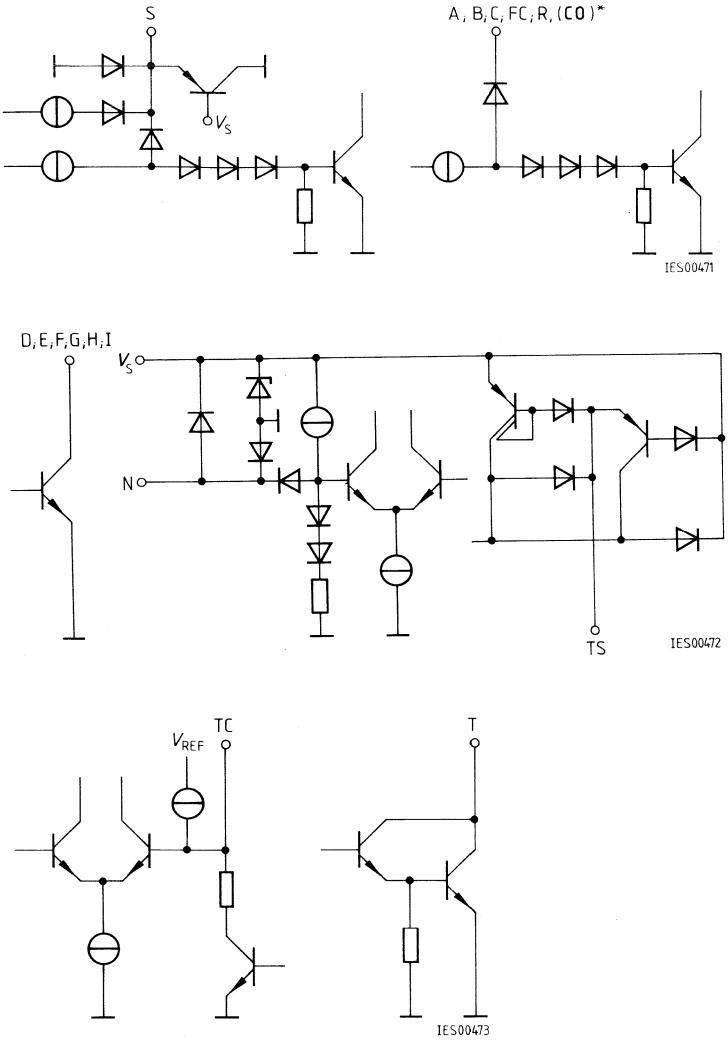
Characteristics

$V_S = 5.5$ V; $T_A = 25$ °C

Parameter	Symbol	Test Conditions	Test Circuit	Limit Values min.	typ.	max.	Unit
Supply current[1])	I_S	$V_{IS} = 0$ V	1		1.6	2.5	mA
V_S (impressed DC)[2])	V_S	$-I_N = 2.5$ mA	1		7.5	8.0	V
V_S (impressed AC)[2])	V_S	$I_{N\,rms} = 5$ mA	1		7.5	8.0	V
Voltage at S[3])	V_{IS}	$I_{IS} = 2$ mA			V_S+0.9	V_S+1.0	V
		$-I_{IS} = 2$ mA		−0.9	−0.8		V
Switching threshold at A, B, C, S, FC, R, CO	$V_{A...}$		2	1.0	1.8	2.4	V
H-switching threshold at N[4])	V_N		2		1.8	2.4	V
L-switching threshold at N[4])	V_N		2	0.8	1.2		V
Switching hysteresis at N[4])	V_N		2	0.4	0.6	0.9	V
Switching threshold at TC (capacitor charge)	V_{TC1}		2	0.8	1.4	2.2	V
Switching threshold at TC	V_{TC2}		2	2.5	3.3	4.0	V
Switching threshold at TS	V_{TS+}	$V_{TS} > V_S$	2		V_S+1.3		V
	V_{TS-}	$V_{TS} < V_S$	2		V_S−1.3		V
L-input current at A, B, C, FC, R, CO	$-I_{A...}$	$V_{A...} = 0$ V	1		20	35	µA
L-input current at S	$-I_{IS}$	$V_{IS} = 0$ V	1		60	105	µA
L-input current at N[4])	$-I_N$	$V_N = 0$ V	1		40	70	µA
H-input current at A, B, C, S, FC, R, CO	$I_{A...}$	$V_{A...} = V_S$	1			1	µA
H-input current at N[4])	I_N	$V_N = V_S$	1			1	µA
H-input current at TC	I_{TC}	$4.5 \le V_{TC} \le V_S$	1		20	45	µA
L-input current at TC	I_{TC}	$V_{TC} = 0$ V	1		20	45	µA
Pos. switch-over current at TS	I_{TS+}	$R_{SYN} = 0$	2	10	25	40	µA
Pos. switching hysteresis at TS	I_{Hy+}	$R_{SYN} = 0$	2	0.3	1.0	4	µA
Neg. switch-over current at TS	I_{TS-}	$R_{SYN} = 0$	2	10	25	40	µA
Neg. switching hysteresis at TS	I_{Hy-}	$R_{SYN} = 0$	2	0.3	1.0	4	µA
L-voltage at D, E, F, G, H, I	$V_{D...}$	$I_{D...} = 0.5$ mA	1		0.15	0.4	V
H-reverse current at D, E, F, G, H, I	$I_{D...}$		1			1	µA
L-output voltage at T	V_Q	$I_T = 1$ mA	1		0.7	1.1	V
	V_Q	$I_T = 10$ mA	1		0.8	1.2	V
	V_Q	$I_T = 100$ mA	1		1	1.5	V

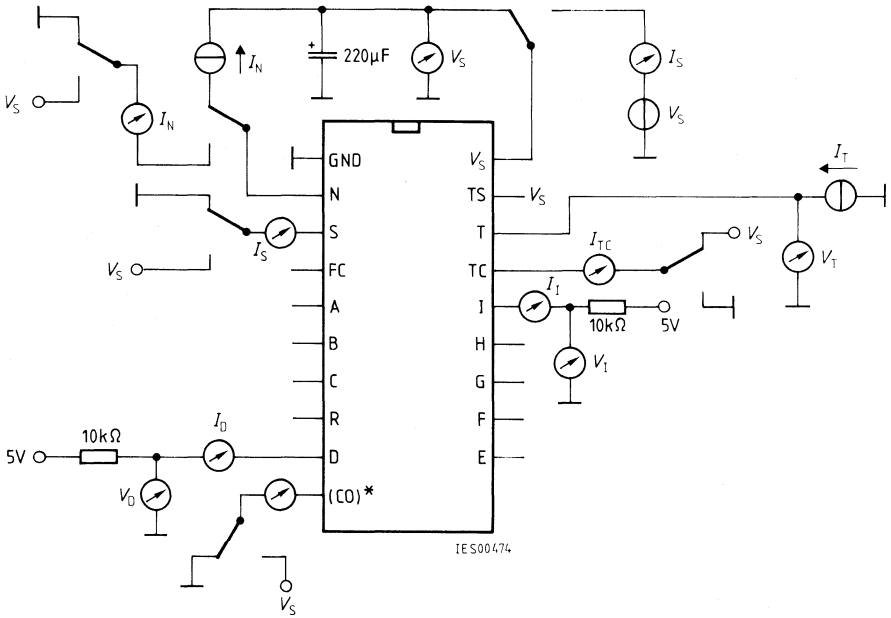
[1]) with impressed voltage at V_S
[2]) with impressed current at N
[3]) with impressed current at S
[4]) if N is clock input

Internal Wiring of Inputs/Outputs and Supply Pins



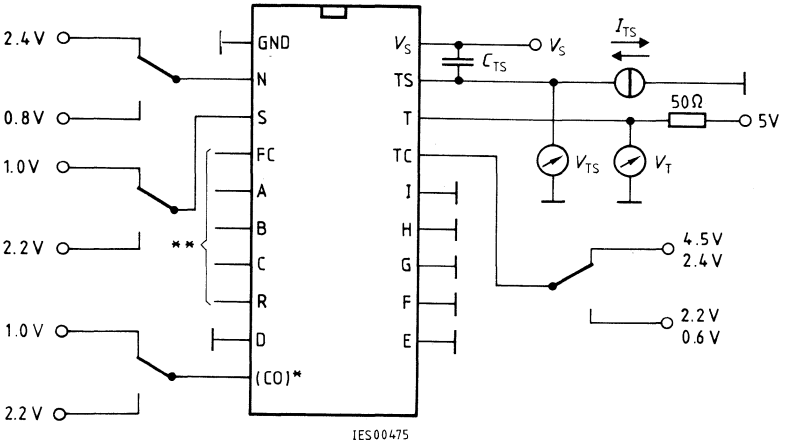
* Figures in parentheses apply to SAE 0532 G.

Test Circuit 1



Note: The external wiring of pins FC to R equals to that of pin S (Test Circuit 1)

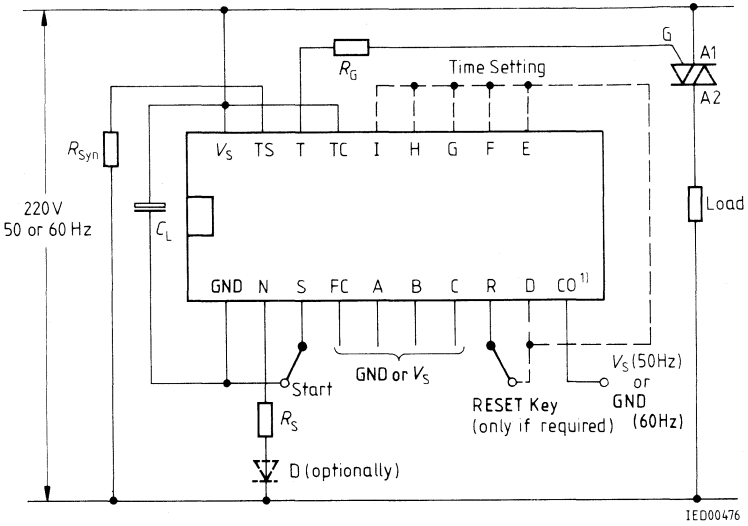
Test Circuit 2



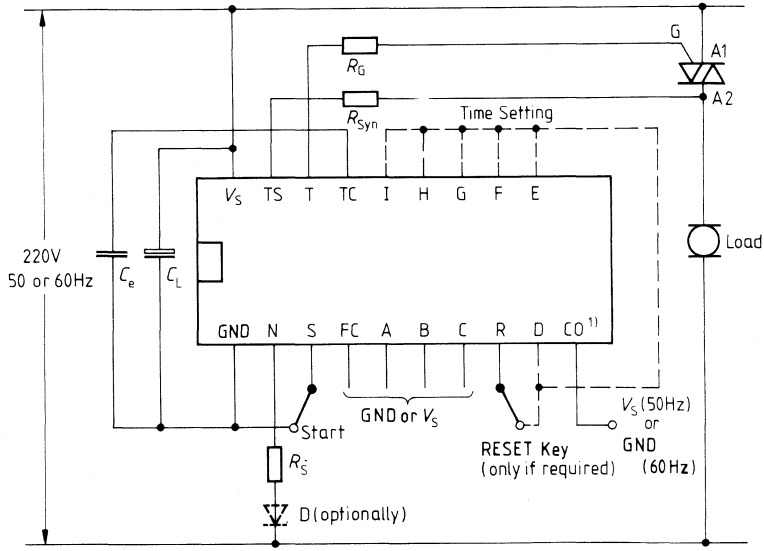
* The symbol in parentheses applies to SAE 0532.

Note: The external wiring of pins FC to R equals to that of pin S (Test Circuit 2)

Application Circuit 1
Operation with resistive load



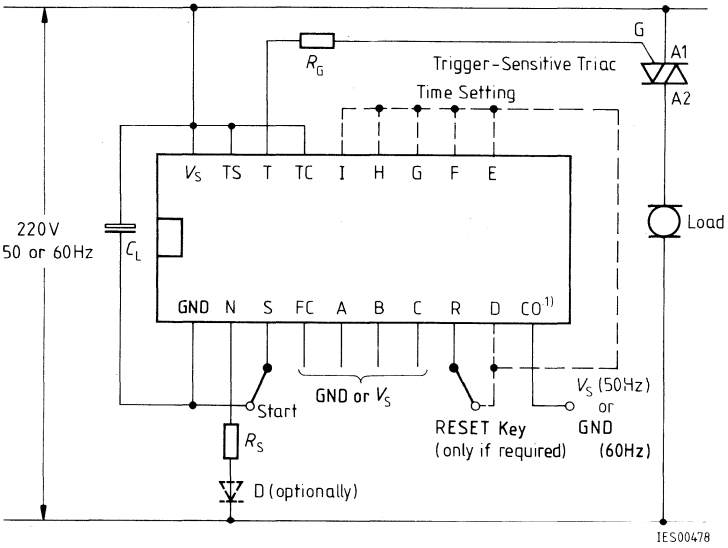
Application Circuit 2
Operation with resistive, capacitive and inductive load



1) Refers to SAE 0532 G

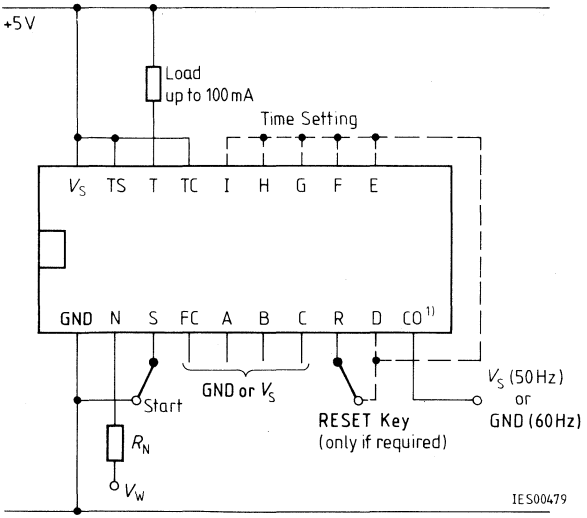
Application Circuit 3

Operation with any load and continuous triac triggering



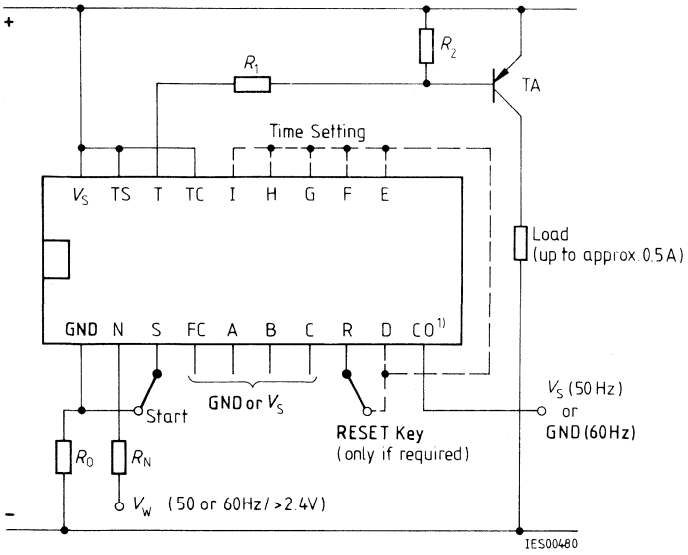
Application Circuit 4

Operation with 5 V DC voltage



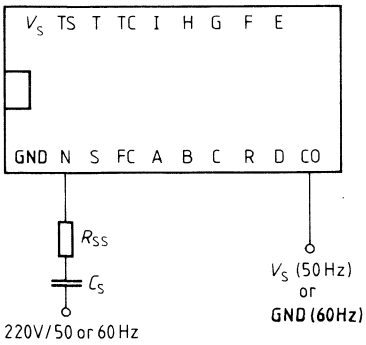
1) Refers to SAE 0532G

Application Circuit 5
Operation with DC voltage > 5.5 V



Application Circuit 6
Operation with capacitive series resistor

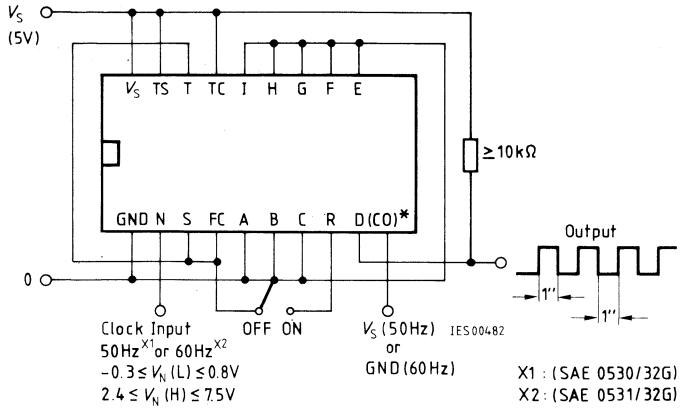
In the application circuits 1 to 3 a series connection of R and C may be utilized instead of R_S or R_S and D.



1) Refers to SAE 0532G

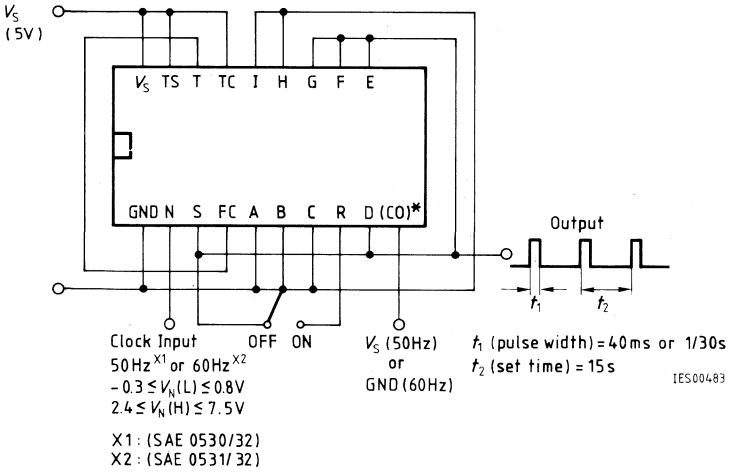
Application Circuit 7

Squarewave Generator



Application Circuit 8

Pulse Generator



Note

The pulse width t_1 is determined only by the clock frequency $f = 50$ Hz (SAE 0530/32 G) or $f = 60$ Hz (SAE 0531/32 G) on input N: for 50/60 Hz: $t_1 = 2/f = 2/50$ (or 2/60) = 40 ms (or 1/30 s). Immediately after turn-on the first pulse t_1 and accordingly the first cycle t_2 can be up to 20 ms (or 1/60 s) shorter (according to the phase of the 50-Hz or 60-Hz network).

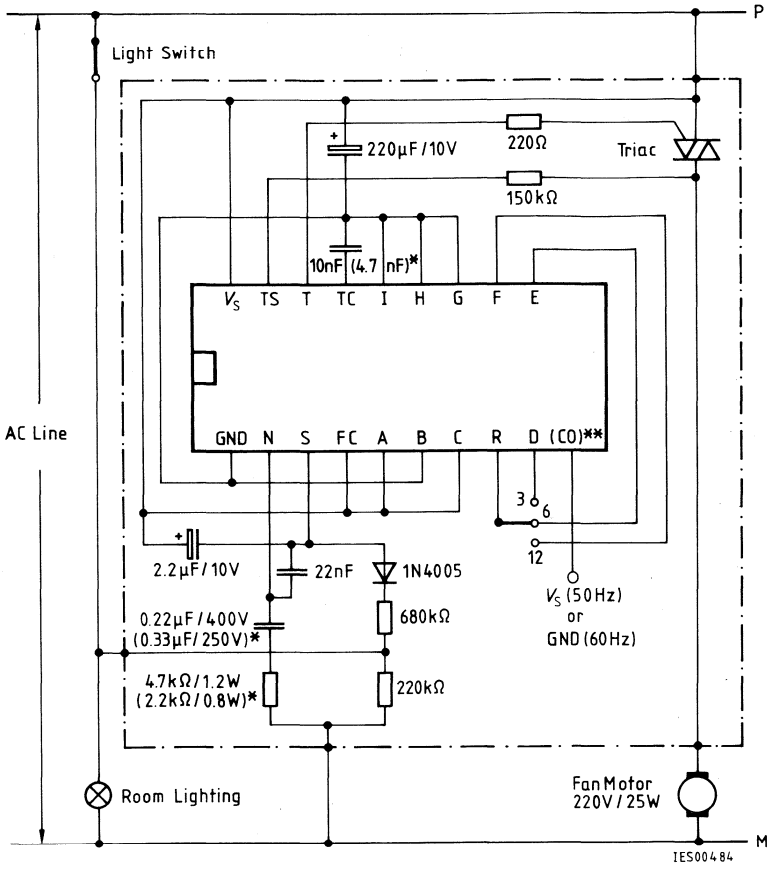
After turn-on output T conducts and stays on L potential throughout operation.

* Figures in parentheses apply to SAE 0532 G.

Application Circuit 9

Timing Control for Ventilator

(Adjustable to 3, 6, or 12 min follow-up)



Function of Circuit

The fan motor starts up when the room lighting is turned on and switches itself off automatically 3 (6 or 12)** minutes after the lighting is turned off.

* Figures in parentheses apply to 60-Hz mode (SAE 0531/32G), all other figures to 50-Hz mode (SAE 0530/32G).
** Figures in parentheses apply to SAE 0532G.

Dimensioning of Application Circuits

The following equations provide guideline values for operation with sinusoidal alternating voltages of 50 Hz (SAE 0530/32G) or 60 Hz (SAE 0531/32G). The firing of the triac always occurs in the 2nd and 3rd quadrant (negative trigger current).

$$\text{T (trigger-pulse length)} = \frac{5\ (4.18)^{*}) \text{ x holding current}}{\text{rms load current}}\ \text{[ms]} \quad (\text{for } T \leq 1.5 \text{ ms})$$

$$R_G = \frac{V_S - V_{TL} - \text{trigger voltage}}{\text{trigger current}}$$

$$R_V = \frac{0.5 \text{ x rms line voltage} - V_S}{I_S + \text{averaged trigger current}} \quad \text{(with or without diode D)}$$

Averaged trigger current = 0.1 (0.12)*) x trigger current x T (T in ms)

$$\text{Dissipation on } R_V \text{ (without diode D)} = \frac{(\text{rms line voltage})^2}{R_V}$$

$$\text{Dissipation on } R_V \text{ (with diode D)} = \frac{0.5\ \text{x (rms line voltage)}^2}{R_V}$$

$$C_L = \frac{20(17)^{*}) \text{ x rms line voltage}}{R_V}\ [\mu\text{F, V, k}\Omega] \text{ (residual AC voltage on } V_S \leq 0.5\ V_{pp})^{***})$$

Application circuit 1 (voltage synchronization for resistive load)

$$R_{syn} = \frac{0.22\ (0.27)^{*}) \text{ T x rms line voltage} - 1.3}{0.025} \geq \frac{\text{peak line voltage}}{4}$$

[kΩ, V, ms] (for T ≤ 1.5 ms)

Application circuit 2 (current synchronization)

C_e = 16.7 x T [nF, ms]***)

$$R_{syn}{}^{**}) \geq \frac{\text{max. forward voltage} - 1.3}{I_{TSmin}}\ [\text{k}\Omega, \text{V, mA}]$$

$$R_{syn}{}^{**}) \geq \frac{\text{peak line voltage}}{4}\ [\text{k}\Omega, \text{V}]$$

$$R_{syn} \leq \frac{\text{trigger voltage} - 1.3}{I_{TSmax}}\ [\text{k}\Omega, \text{V, mA}]^{***})$$

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32G).
**) The larger value applies.
***) See application notes.

Application circuit 3

See R_G, R_V, C_L

Application circuit 4

The level of the AC voltage V_{ac} must be greater than 2.4 V_p.

$R_N \approx 5 \times V_{ac} + 5$ [kΩ, V_p]

Application circuit 5

V_{ac}, R_N: see application circuit 4 (V_{ac} referred to pin 0)

$$R_o = \frac{V_S - 5.5}{I_S + I_{R1}}$$

$$R_1 = \frac{5.5 - V_{TL} - V_{B(TA)}}{I_{R1}}$$

$$R_2 = \frac{V_{B(TA)}}{I_{R2}}$$

$$I_{R1} = I_{B(TA)} + I_{R2}$$

$$I_{R2} \approx 0.05 \times I_{B(TA)}$$

Application circuit 6

$$C_V \approx \frac{4\ (3.3)^*)}{R_V}\ [\mu F, k\Omega]$$

$R_{VV} = 0.2 \times R_V$**)

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32G).
**) See application notes.

Selector Guide

Type	Package	Function	Technical Data	Page
Acoustic Signal Generators				
SAB 0600	P-DIP-8	**Three-tone chime IC,** melodious and voluminous three-tone sound, few external components, integrated output stage for 80 Ω loudspeakers	V_S = 7 to 11 V Standby current < 1 µA	525
SAB 0601		**Single-tone chime**		525
SAB 0602		**Double-tone chime**		525
SAE 0700	P-DIP-8	**Signal-tone generator,** produces two subsequent, periodical tone frequencies in the ratio 1.4:1.	V_S = 9 to 25 V or ac voltage from 10 V_{rms}	534

SIEMENS

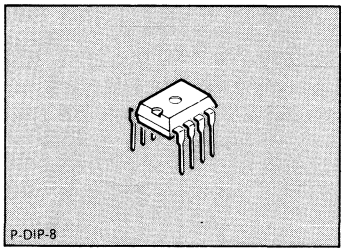
Three-Tone Chime
Single-Tone Chime
Dual-Tone Chime

SAB 0600
SAB 0601
SAB 0602

Bipolar IC

Features

- Melodious sound
- Few components required
- Integrated output stage for 8 Ω loudspeaker
- Standby current < 1 µA



	Type	Ordering Code	Package
S	SAB 0600	Q67000-H1948	P-DIP-8
S ■	SAB 0601	Q67000-H2312	P-DIP-8
S ■	SAB 0602	Q67000-H2313	P-DIP-8

■ Not for new design

Single-Tone Chime SAB 0601 and Dual-Tone Chime SAB 0602

The two variants SAB 0601 and SAB 0602 were derived from type SAB 0600 by suppressing the last two tones or last tone, respectively, of the three-tone sequence. The SAB 0600 data applies correspondingly.

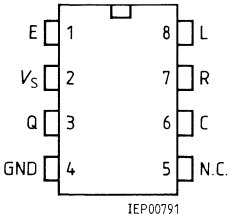
Three-Tone Chime SAB 0600

This IC generates the tone sequence of a 3-tone chime. The sound pattern is created by three harmonically tuned frequencies which are switched in succession to a summing point and decay individually in amplitude.

The tone color is adjusted by an external *RC* network (R_1, C_1, C_2). An 8 Ω loudspeaker can be connected directly via a 100 µF capacitor.

An appropriate design of the loudspeaker housing (shaped as tube or horn) enhances the volume and tone quality and contributes to a pleasant, melodious sound.

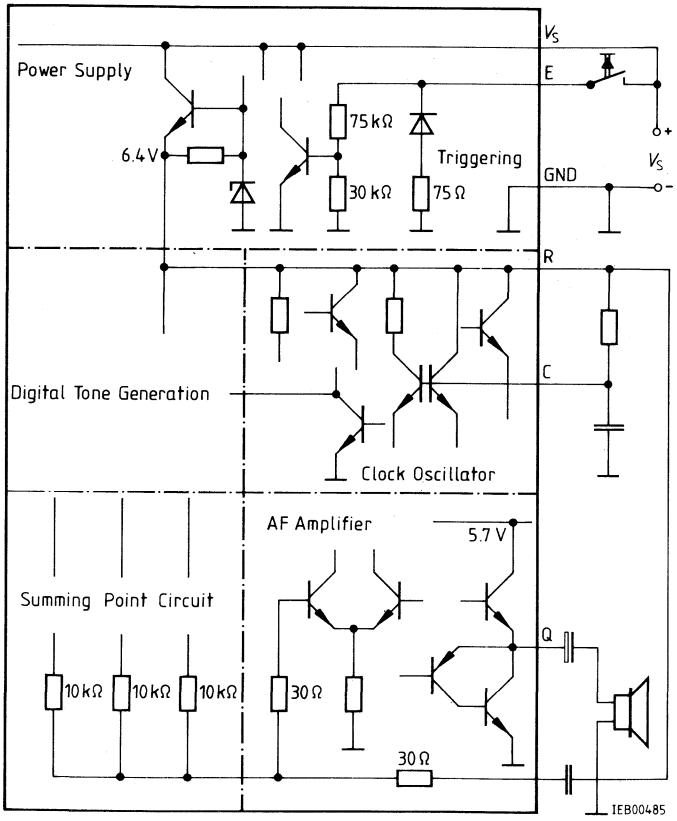
Pin Configuration



Pin Definitions and Functions

Pin	Symbol	Function
1	E	Input
2	V_S	Voltage Supply
3	Q	Output
4	GND	Ground
5	N.C.	Not connected
6	C	Oscillator
7	R	Reference
8	L	Compensation

Figure 1
Block Diagram



8

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S	−0.5	11	V
Input voltage at E	V_E	−0.5	V_S	V
Neg. input current at E	$-I_E$		2	mA
Load resistance at Q	R_L	7		Ω
Current consumption at start of tone sequence } refer to measurement circuit	I_{SM}		90	mA
Current consumption at end of tone sequence } refer to measurement circuit	I_{SO}		35	mA
Oscillator frequency at C (due to power dissipation)	f_{OSC}	6		kHz
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system – air)	$R_{th\ SA}$		120	K/W

Operating Range

Supply voltage	V_S	7	11	V
Ambient temperature	T_A	0	70	°C
Oscillator frequency at C	f_{OSC}	6	100	kHz

Characteristics

$V_S = 7$ V to 10 V; $T_A = 25$ °C

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Standby input current	I_0		< 1	10	µA
Supply current with open output	I_{SO}		20	35	mA
Max. output power at 8 Ω (tone 3)	P_Q		0.16		W
Max. output voltage at Q (tone 3)	$V_{Q\ pp}$		2.8	4.0	V
Deviation of the max. individual amplitudes referred to tone 3	ΔV_{QM}		± 5		%
Frequency variation of basic oscillator with R_1, C_1 = const.	Δf_o		± 5		%
Triggering voltage at E	V_E	1.5		V_S	V
Input current at E ($V_E = 6$ V)	I_E	500	700		µA
Noise voltage immunity at E	$V_{EN\ pp}$		0.3		V
Triggering delay at $f_o = 13.2$ kHz (t_D varies in inverse proportion to f_o)	t_D	2		5	ms
Min. value of external load resistor	R_1		10		kΩ
Max. value of external load resistor	R_1		100		kΩ

Figure 2
Test Circuit

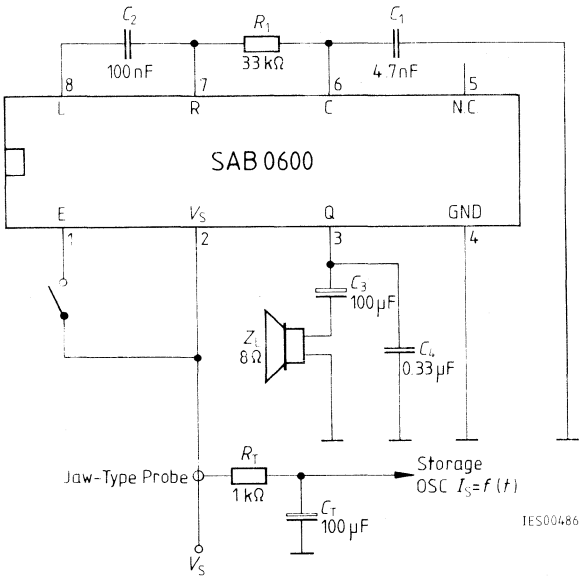


Figure 3
Integral Current Consumption in the Measurement Circuit

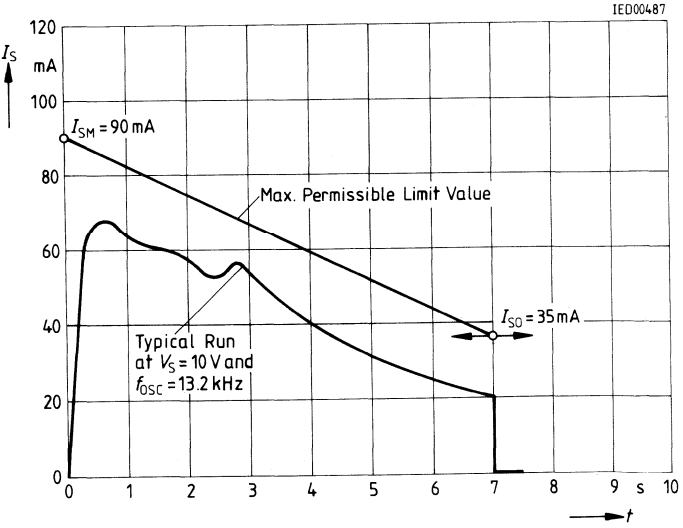
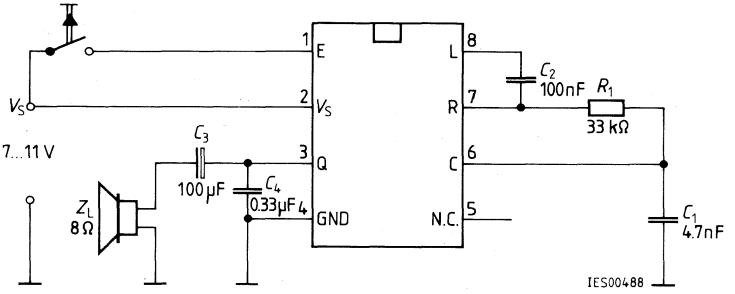


Figure 4
Typical Application Circuit



Functional Description

The three frequencies – 660 Hz, 550 Hz, and 440 Hz – are obtained by dividing the output of a 13.2 kHz oscillator. One of these three frequencies is divided again to obtain the time base for the tone-decay process. From this time base, 4-bit D/A converters (one for each tone) generate the decay voltage with which the three tones are successively activated and, overlapping each other, are attenuated. The basic frequency is determined by an external *RC* network (pins R and C).

The output stage can drive an 8 Ω loudspeaker with approximately 0.16 W via 100 µF. The output voltage is of square shape. To obtain a melodious output tone as required, the higher harmonics may be reduced by shunting pin L through a suitable capacitor to ground. The output volume can be regulated here by means of a potentiometer.

The circuit only draws current in the active state, and automatically switches off after the tones have decayed. The circuit is activated by a short pulse, between 1.5 V and V_S in amplitude, applied to the triggering connection E (pin 1). If the trigger voltage is still, or again, present when the tones have decayed, the three tones are repeated.

The circuit is not activated when a trigger pulse on E is shorter than 2 ms (interference suppression).

To prevent triggering of the circuit by cross-talk voltages, especially in case of long input lines, the noise voltage peaks should be limited to 0.3 V at the IC input. For this purpose the control line (possibly in front of a series resistor) can be shunted to ground through a suitable capacitor.

Application for AC and DC Triggering (Figure 5)

The input can alternatively be triggered with direct or alternating current. An internal diode circuit hereby short-circuits the input for negative halfwaves.

The peak voltage of the positive halfwave is added to the battery voltage. A series resistor must be connected into the trigger line to limit the voltage at input E (pin 1) to a maximum value equal to V_S.

The minimum input current at pin E of the SAB 0600 (pin 1) is 500 µA at 6 V. If the voltage dropoccuring at 500 µA at the series resistor R_3 **(Figure 5)** amounts to at least the AC peak voltage between A and B ($\hat{V}_{AB}$ AC), the IC will be safe.

The formula $$R_{3\,min} = \frac{\hat{V}_{AB\,max.}}{500\ \mu A}$$

determines the lower limit for R_3.

The upper limit for R_3 is determined by the lowest trigger voltage between A and 0 (pin 4). In the application shown in **Figure 5**, this will be the battery voltage if the device is also to be operated independently of the bell system (triggering by short circuit of A and B).

For reliable triggering, the SAB 0600 requires a current of at least 50 µA with approx. 1.5 V at pin E. Assuming this current, the voltage drop at R_3 must, therefore, not exceed $V_S - 1.5$ V.

The formula $$R_{3\,max} = \frac{V_{S\,min.} - 1.5\ V}{50\ \mu A}$$

results in the upper limit for R_3.

8

Calculation Example for the Circuit in Figure 5

max. $V_{AB\,rms} = 25$ V max. $\hat{V}_{AB} = 25\ V \times \sqrt{2} = 35.4$ V

$$R_{3\,min} = \frac{35.4\ V}{500\ \mu A} = 70.8\ k\Omega$$

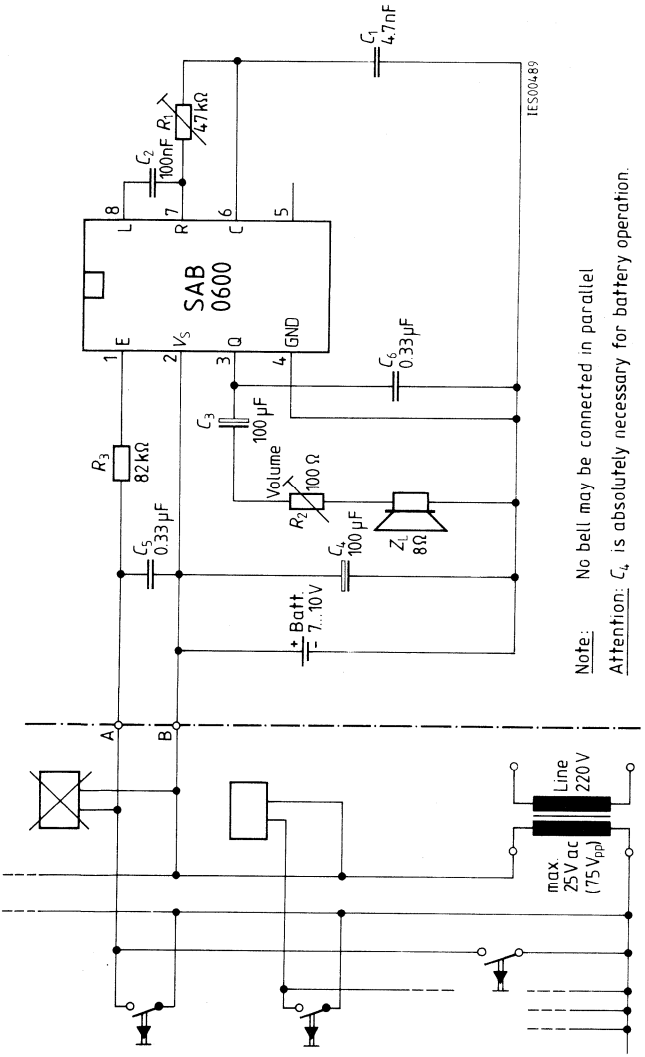
min. $V_S = 6$ V

(The operating range of the SAB 0600 may extend to 6 V for individual components).

$$R_{3\,max} = \frac{6\ V - 1.5}{50\ \mu A} = 90\ k\Omega$$

In this example, a value of 82 kΩ ± 10% would be suitable for R_3.

Figure 5
Circuit for SAB 0600 Application in Home Chime Installations Utilizing AC and DC Triggering; Adjustable Sound and Volume



PCB layout information: Because of the peak currents at V_S, Q, and GND and to avoid RF oscillations, the lines should be designed in a flatspread way or as star pattern. Star points are the terminals of capacitor C_4.

Further Details Regarding the Circuit in Figure 5

Since an ohmic contact between A and B causes triggering of the chime, no bell may be connected in parallel to the chime. However, paralleling several chimes does not cause any problems.

In older batteries, the higher internal resistance of the battery may cause voltage drops becoming apparent as distortions. C_4 serves as a buffer element expanding the service life of the battery.

The trigger line connected to pin A acts – in open state – as antenna for noise pulses which could trigger the chime unintentionally. Capacitor C_5 will largely suppress such interference.

If there is the risk of incorrect polarity connection when changing the battery, the battery line should be protected by a diode.

For the selection of components, the following recommendations are given:

Capacitors:

C_1: 4.7 nF/≥ 10 V, ± 5%; e.g. MKT
C_2: 100 nF/≥ 10 V, ± 20%; e.g. MKT
C_3: 100 µF/≥6.3 V, ± 100/—10%; e.g. aluminum electrolytic
C_4: 100 µF/≥ 10 V, + 100/—10%; e.g. aluminum electrolytic
C_5, C_6: 330 nF/≥ 50 V, + 100/—20%; e.g. ceramic

Resistors:

R_3: 82 kΩ/0.1 W, ± 10%, carbon film resistor
R_1: When a fixed resistor is used, 0.1 W ± 5% metal film resistor.

8

SIEMENS

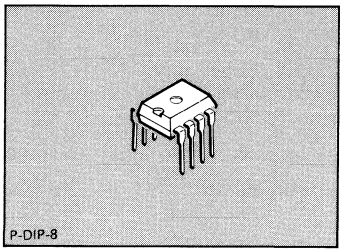
Audible Signal Device

SAE 0700

Bipolar IC

Features

- Direct AC-voltage feeding possible through integrated bridge rectifier
- Integrated overvoltage protection through Z-diode, approx. 28 V
- Bridge rectifier provides for protection against reverse polarity in DC operation
- Few external components (one resistor and one capacitor minimum)



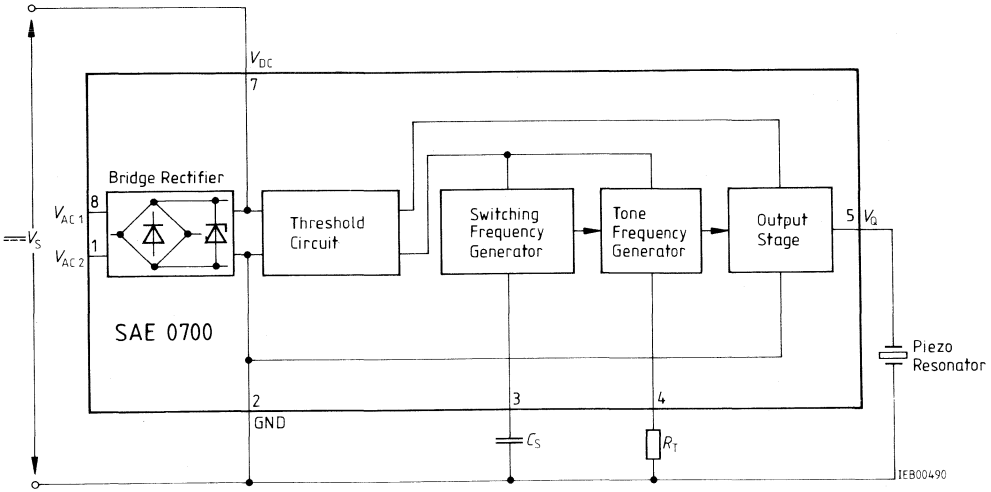
Type	Ordering Code	Package
S SAE 0700	Q67000-A2445	P-DIP-8

The audible signal device SAE 0700 generates two tone frequencies in a ratio of approx. 1.4:1 that follow one another in a periodic sequence. The tone frequency can be varied throughout a range between 100 Hz and 15 kHz by an external resistor. The switching frequency of 0.5 to 50 Hz is set by an external capacitor. The SAE 0700 can be used to drive either a loudspeaker or a piezo-ceramic transducer. The SAE 0700 can be supplied with voltage in two ways:

1. rms AC voltage from 10 V
2. DC voltage from 9 to 25 V

The SAE 0700 issues the tone sequence for as long as the supply voltage is applied. After application of the supply voltage, the tone sequence commences with the higher of the two tones.

Figure 1
Block Diagram (with external components for DC supply)



8

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{AC2}	AC-voltage input
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	Q	Output
6	N.C.	Not connected
7	V_{DC}	DC-voltage input
8	V_{AC1}	AC-voltage input

Functional Description

The audible signal device SAE 0700 (see block diagram, **fig. 1**) includes the following functional blocks:

- bridge (for voltage supply) and overvoltage protection
- threshold circuit
- switching-frequency generator
- tone-frequency generator
- output stage

Bridge rectifier: The bridge rectifier enables direct feeding with AC voltage or DC voltage (independent of polarity). DC-voltage supply without integrated bridge is also possible via pins V_{DC} and GND.

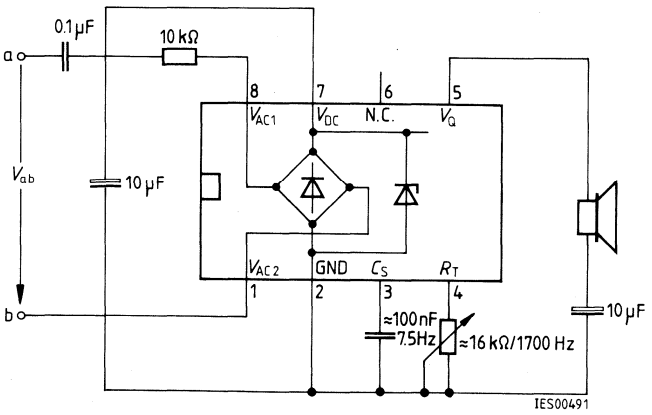
If the voltage is supplied via the bridge, the input voltage V_{81} should be dimensioned such that at least 9 V appear at the pin V_{DC} (also with output loading). It should also be noted that in the case of voltage supply via the bridge, the maximum output current has to be limited to 50 mA.

Response of the SAE 0700 as a result of spikes on the AC line is prevented by a built-in initial resistance R_{INI}. In a voltageless condition R_{INI} provides for discharging the storage capacitor of V_{DC} to ground.

The Z-diode following the bridge serves as overvoltage protection. The bridge circuitry shown in **figure 2** efficiently protects the SAE 0700 against damage as a result of the following voltage values:

- overvoltages in acc. with VDE 0433 (2 kV – 10/700 µs)
- AC voltages up to 220 V/50 Hz for a duration of 30 s

Figure 2



Threshold circuit: With a threshold voltage of typically 8.6 V this ensures that the SAE 0700 is not activated by noise pulses.

Switching-frequency generator: This switches periodically between the two frequencies produced by the tone-frequency generator. Wiring with a capacitor C_S produces a switching frequency f_S according to the following formula:

$$f_S\,[\text{Hz}] = \frac{750}{C\,[\text{nF}]} \pm 25\% \quad \text{(valid from 0.5 to 50 Hz)}$$

Tone-frequency generator: This generates a squarewave voltage with the two tone frequencies f_{T1} and f_{T2}. The basic frequency f_{T1} and the second tone frequency f_{T2} are calculated according to the following formulae:

$$f_{T1}\,[\text{Hz}] = \frac{2.72 \times 10^4}{R\,[\text{k}\Omega]} \pm 25\% \quad \text{(valid from 0.1 to 15 kHz)}$$

$$f_{T2}\,[\text{Hz}] = f_{T1} \times (0.725 \pm 5\%)$$

The tone-frequency generator is temperature-compensated for better stability.

Output stage: This boosts the generated tone voltage for direct driving of a piezo-ceramic transducer or a loudspeaker, possibly across a dropping resistor.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Voltage at pin 7	V_{DC}	−0.5	26	V
Voltage at pin 3	$V_{3\,2}$	−0.5	5.5	V
Voltage at pin 4	$V_{4\,2}$	−0.5	7	V
Output voltage at pin 5	V_Q	−0.5	V_{DC} +0.5	V
AC voltage at pin 8 and 1 (peak value)	V_{AC}		28	V
Input current of bridge	$I_{8\,1}$	−50	50	mA
AC input current of bridge	$I_{8\,1\,rms}$		25	mA
Output current (50 µs, duty cycle 1:10)	I_Q	−100	100	mA
Output current	$I_{Q\,rms}$		50	mA
Total power dissipation ($T_A = 25\,°C$)	P_{tot}		0.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance system – air	$R_{th\,SA}$		120	K/W

Operating Range

Supply voltage	V_{DC}	9	25	V
Tone frequency	f_{T1}	0.1	15	kHz
Ambient temperature	T_A	−25	85	°C

Characteristics

$T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
Current consumption	I_{DC}		1.5	1.8	mA	$V_{DC} = 9$ V to 25 V without load
Switching threshold	$V_{DC\,ON/OFF}$	8	8.6	9	V	
Initial resistance	R_{INI}	3.5	4.7	6	kΩ	see characteristic, **figure 3**
Output-voltage swing	V_Q	V_{DC}−3.7	V_{DC}−3		V	$I_Q = \pm 10$ mA
Tone frequency	$f_{T\,1}$	1.275	1.700	2.125	kHz	$V_{DC} = 15$ V, $V_{3\,2} = 0$ V $R_T = 16$ kΩ
Switching frequency	f_S	5.6	7.5	9.4	hZ	$V_{DC} = 15$ V, $C_S = 100$ nF
Tone frequency ratio	$f_{T\,1}/f_{T\,2}$	1.31	1.38	1.45		
Temperature coefficient of tone frequencies	TC_f		8×10^{-4}		K^{-1}	

Characteristic Curves

Figure 3
Current consumption versus supply voltage V_{DC} without output load

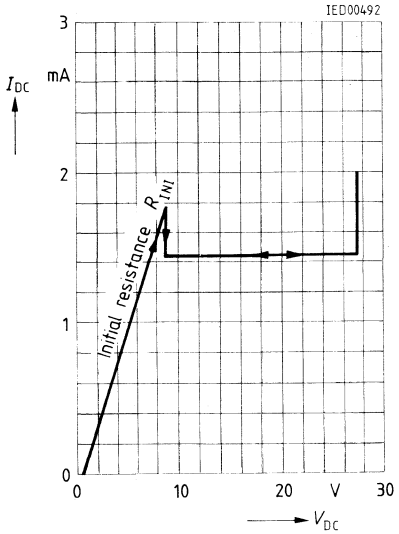


Figure 4
Tone frequencies f_{T1} and f_{T2} versus resistance R_T

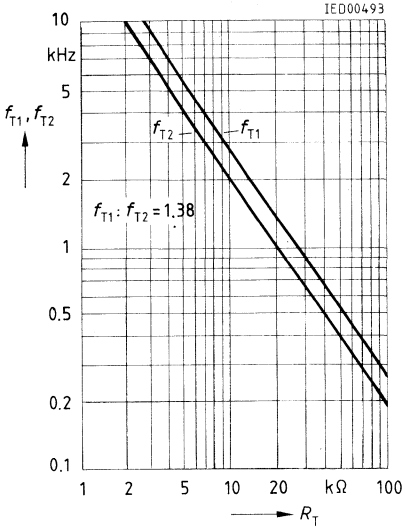
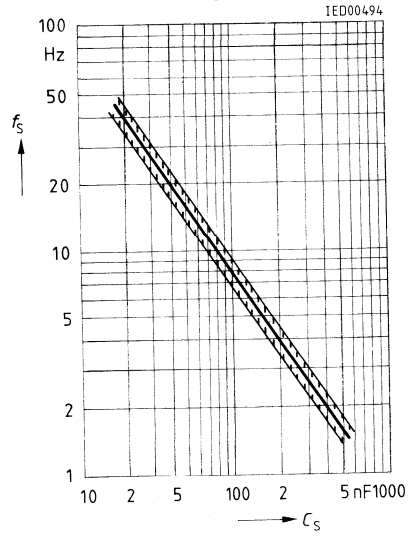


Figure 5
Switching frequency f_S versus capacitance C_S



8

Leistungs-OP, Leistungsbrücken, Spezielle Motoransteuerungen

Power Op Amps, DC Motor Drivers, Special Control ICs

Selector Guide

Type			Features								Page
			Peak output current	Operating range V_S	Max. Supply voltage V_S	Short-circuit proof to $+V_S$	Short-circuit proof to $-V_S$	Clamp diodes	Inhibit	Package	
Power Operational Amplifiers	Single	TCA 365 B	4 A	40 V	42 V	●	●	●		P-T66-5-H	543
		TCA 1365 B	4 A	40 V	42 V	●	●	●	●	P-T66-7-H	553
	Dual	TCA 2365	2.5 A	30 V	36 V	●	●		●	P-SIP-9	563
		TCA 2365 A	2.5 A	30 V	36 V	●	●		●	P-DIP-18-L9	563
		TCA 2465	2.5 A	40 V	42 V	●	●	●	●	P-SIP-9	573
		TCA 2465 A	2.5 A	40 V	42 V	●	●	●	●	P-DIP-16-L10	573
		TCA 2465 G	2.0 A	40 V	42 V	●	●	●	●	P-DSO-20-L12	573
Full-Bridge DC Motor Drivers	DC Motor ICs	TLE 4201 A1	1 A	17 V	36 V		●			P-DIP-18-L9	590
		TLE 4201 S1	1 A	17 V	36 V		●			P-SIP-9	590
		TLE 4202	1.5 A	17 V	36 V		●			P-T66-7-H	599
		TLE 4202 B	2 A	17 V	36 V		●	●		P-T66-7-H	599
		TLE 4203	4 A	26 V	45 V	●	●	●		P-T66-7-H	617
		TLE 4204	3 A	24 V	45 V	●	●	●		P-T66-7-H	625
		TLE 4205	1 A	32 V	45 V		●	●	●	P-DIP-18-L9	633
	Stepper Motor ICs	TCA 1561 B	2.5 A	40 V	45 V	●		●	●	P-SIP-9	641
		TCA 1560 B	1.25 A	40 V	45 V			●	●	P-DIP-18-L9	641
		TCA 1560 G	1.0 A	40 V	45 V					P-DSO-20-L12	641
		TCA 3727	1 A	50 V	60 V	●		●		P-DIP-20-L16	660
Control ICs		SLE 4520	20 mA	5 V	6 V					P-DIP-28	677
		TCA 955	200 mA	16 V	16 V					P-DIP-16	688

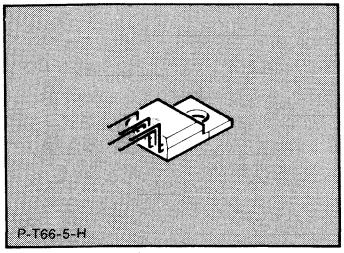
SIEMENS

Power Operational Amplifier

TCA 365 B

Preliminary Data

Bipolar IC



Features

- High peak output current, up to 4 A
- High supply voltage, up to 42 V
- Thermal overload protection
- Internal power limitation
- DC voltage short-circuit proof to $+V_S$ and $-V_S$
- Integrated clamp diodes

Applications

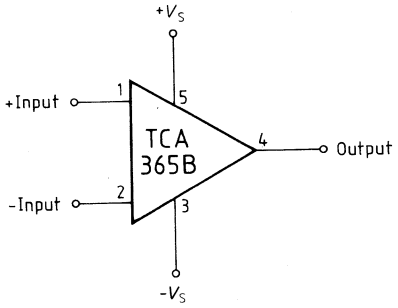
- Power comparator
- Power Schmitt trigger
- Speed control of DC motors

Type	Ordering Code	Package
TCA 365 B	Q67000-A8189	Plastic power package P-T66-5-H (similar to TO-220)

The TCA 365 B is a power op amp in a plastic package P-T66-5-H. At a maximum supply voltage of ± 21 V, the IC produces a high output current of 4 A. The op amp is protected against thermal overload and short circuits.

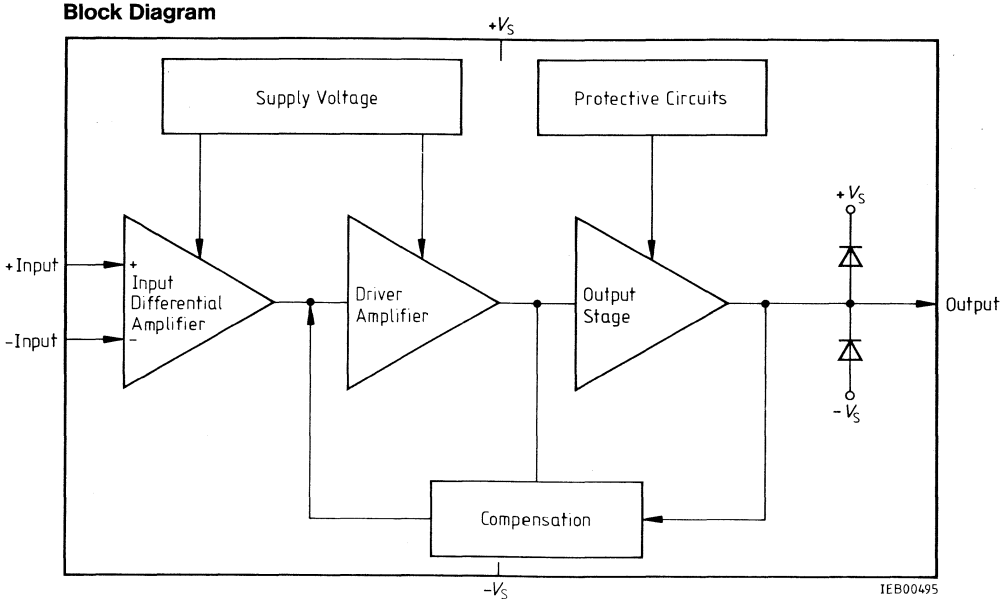
9

Pin Configuration



Pin 3 is electrically connected to cooling fin.

Block Diagram



Absolute Maximum Ratings

$T_C = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage	V_S	0	±21	V	
Differential input voltage	V_{ID}	$-V_S$	$+V_S$	V	
Supply current	I_S	−3.5	4.0	A	
Output current	I_Q	−4.0	4.0	A	
Output current	I_Q	−2.0		A	$V_S \geq \pm 15$ V, $V_Q < -V_S$
Output current	I_Q	−3.0		A	$V_S \geq \pm 10$ V, $V_Q < -V_S$
Ground current	I_{GND}	−4.0	3.5	A	
Power dissipation at $T_C = 85\,°C$	P_D		20	W	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	125	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−25	85	°C	$P_D = 13$ W
Voltage gain	$G_{V\,min}$	20		dB	
Forward current of clamp diode	I_F		3	A	$T_{j\,max} = 125\,°C$
Thermal resistance					
junction – ambient	$R_{th\,jA}$		65	K/W	
junction – case	$R_{th\,jC}$		3	K/W	

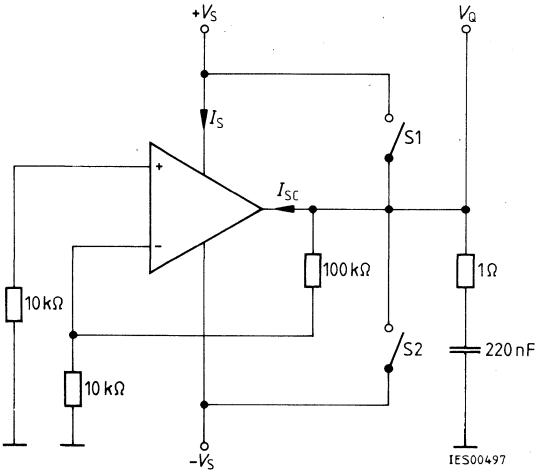
Characteristics

$V_S = \pm 15$ V, $T_j = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Open-loop supply current consumption	I_S		20	40	mA	1
Input offset voltage	V_{IO}	−10		10	mV	2
Input offset current	I_{IO}	−100		100	nA	3
Input current	I_I		0.2	1	µA	3
Output voltage						
$R_L = 12\ \Omega$; $f = 1$ kHz	$V_{Q\,pp}$	± 13.0	± 13.5		V	4
$R_L = 4\ \Omega$; $f = 1$ kHz	$V_{Q\,pp}$	± 12.5	± 13.0		V	
Input resistance $f = 1$ kHz	R_I	1	5		MΩ	4
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70	80		dB	5
Common-mode input voltage range	V_{IC}	+13/−15	+13.5/−15.1		V	6
Common-mode rejection	k_{CMR}	70	80		dB	6
Supply voltage rejection	k_{SVR}	−70	−80		dB	7
Temperature coefficient of V_{IO} $-25\,°C \le T_j \le +85\,°C$	α_{VIO}		50		µV/K	2
Temperature coefficient of I_{IO} $-25\,°C \le T_j \le +85\,°C$	α_{IIO}		0.4		nA/K	3
Slew rate of V_Q for non-inverting operation	SR		2		V/µs	8
Slew rate of V_Q for inverting operation	SR		2		V/µs	9
Noise voltage referred to input (DIN 45405)	V_n		2	5	µV	1
Short-circuit current						
(S1 closed)	I_{SC}		0.75		A	1
(S2 closed)	I_{SC}		−0.75		A	1

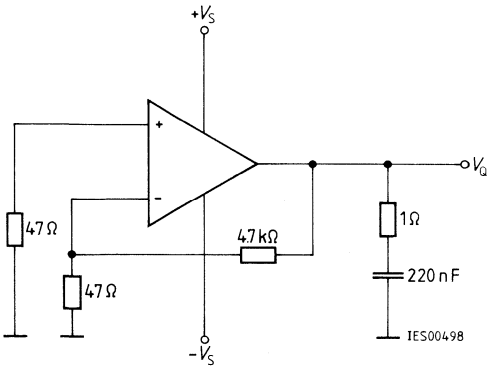
Test and Measurement Circuits

Figure 1
Open-Loop Supply Current Consumption, Noise Voltage



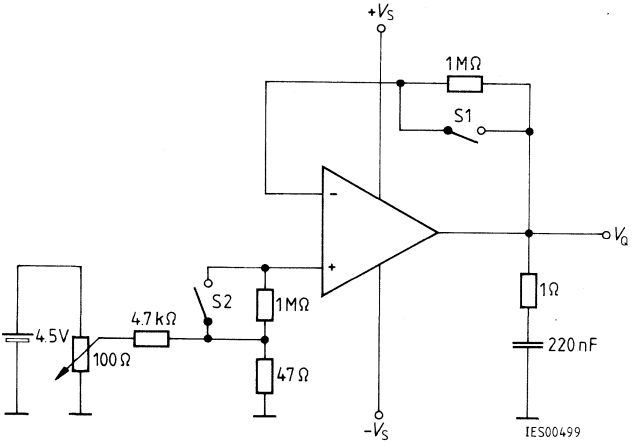
S1 and S2 as shown unless otherwise specified

Figure 2
Input Offset Voltage, Temperature Coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3
Input Offset Current; Input Current, Temperature Coefficient of I_{IO}



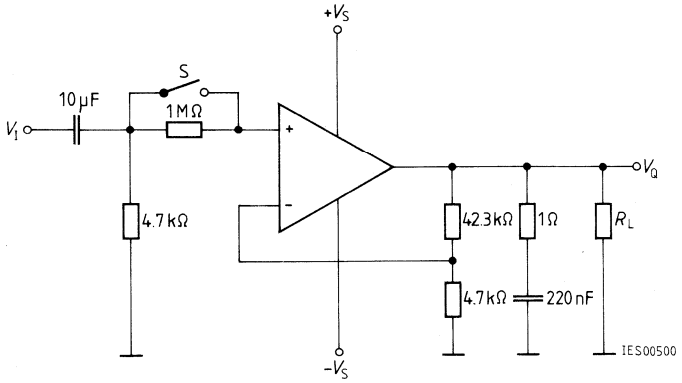
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

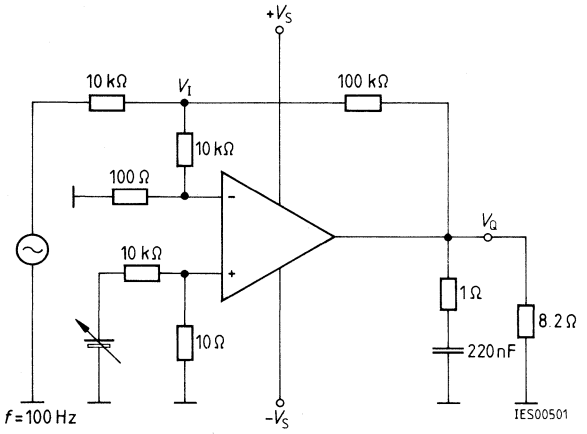
S1 closed – S2 closed: offset alignment

Figure 4
Output Voltage, Input Resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-Loop Voltage Gain



$$G_{V0} = \left| 20 \log 101 \frac{V_Q}{V_I} \right| \text{(dB)}$$

Figure 6
Common-Mode Voltage Gain G_{VC}
Common-Mode Rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

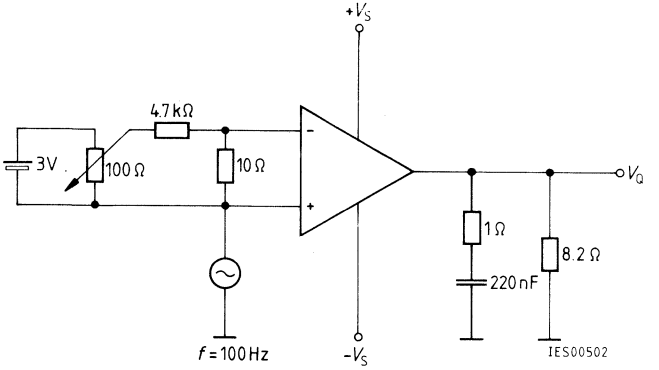
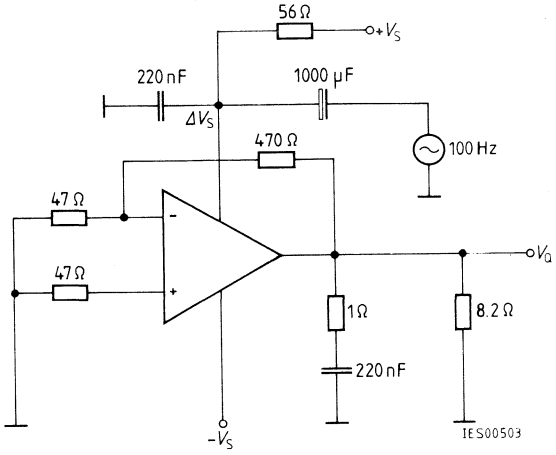


Figure 7
Supply Voltage Rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ (dB)}$$

Figure 8
Slew Rate for Non-Inverting Operation

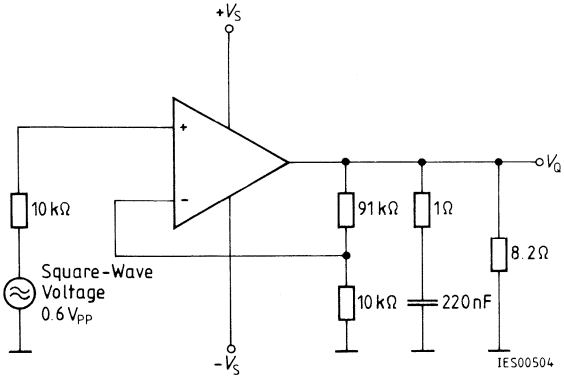


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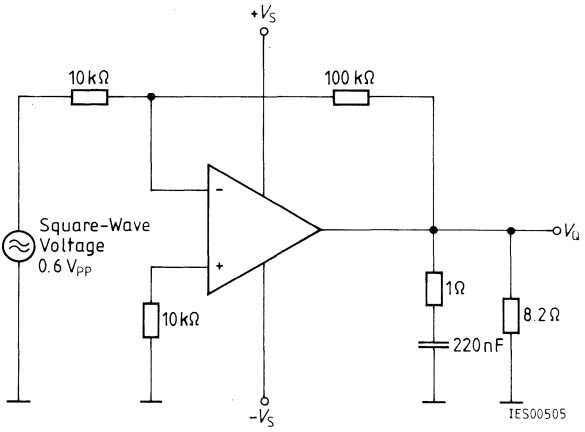
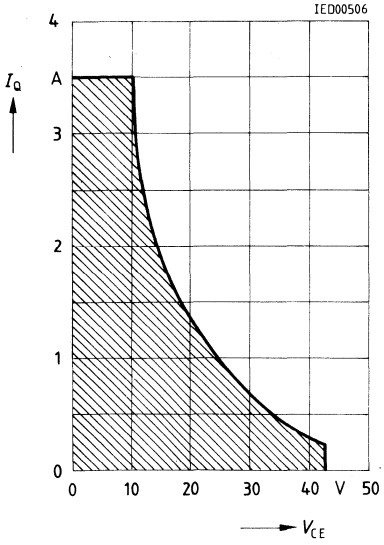
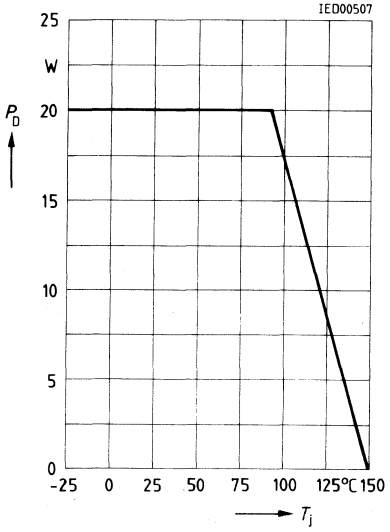
Figure 9
Slew Rate for Inverting Operation



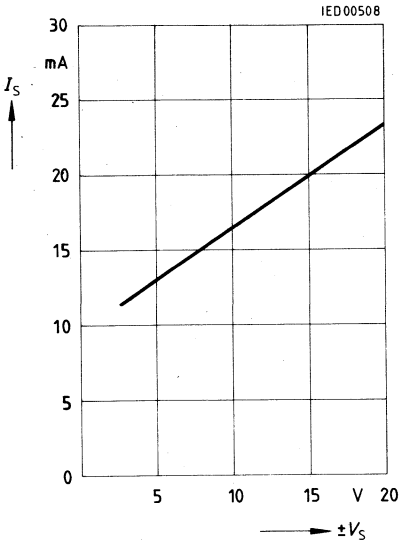
Safe Operating Area of Output Stage
Output Current versus Collector
Emitter Voltage $T_j = 25\,°C$
$V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$



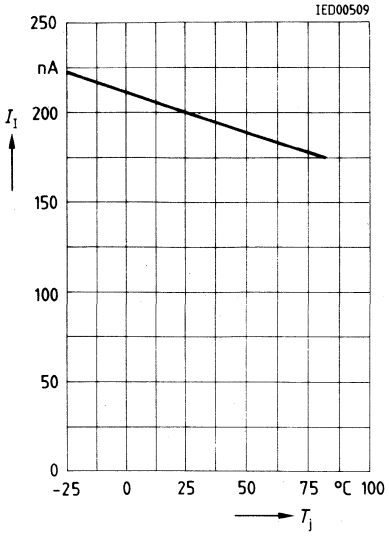
Maximum Permissible Power
Dissipation versus
Case Temperature



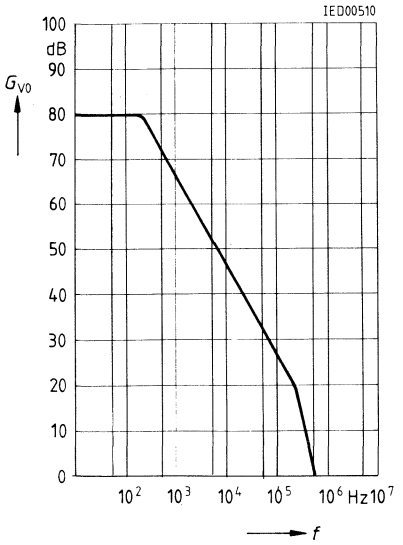
Supply Current versus Supply Voltage
$T_j = 25\,°C$



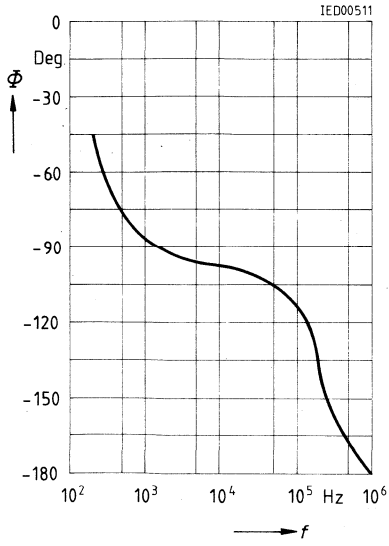
Input Current versus Junction Temperature
$V_S = \pm 15\,V$



Open-Loop Voltage Gain versus Frequency
$V_S = \pm 15\,V$, $T_j = 25\,°C$

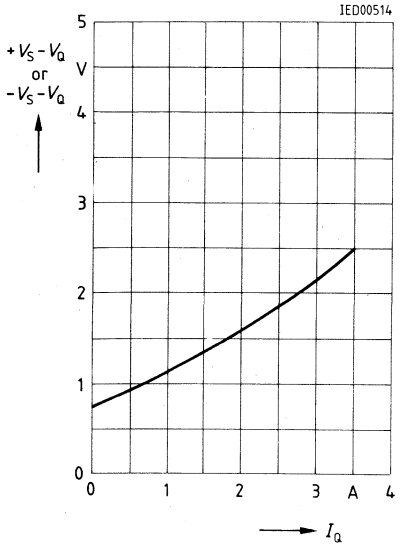


Phase Response versus Frequency
$V_S = \pm 15\,V$, $T_j = 25\,°C$

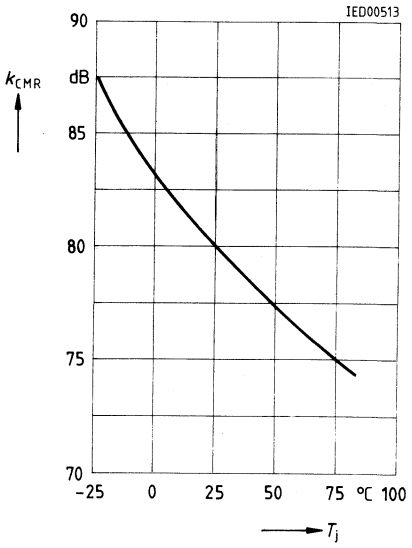


9

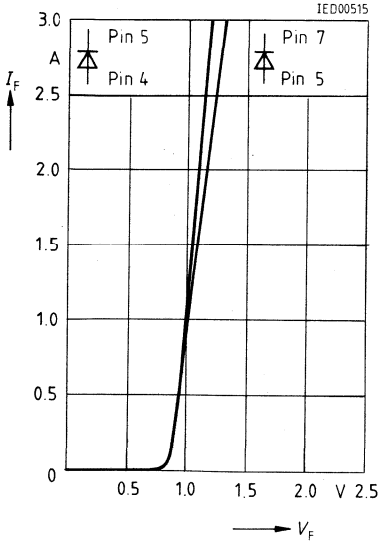
Saturation Voltage versus Output Current
$T_j = 25\,°C$



Common-Mode Rejection versus Junction Temperature
$V = \pm 15\,V$



Forward Current versus Forward Voltage
$T_j = 25\,°C$



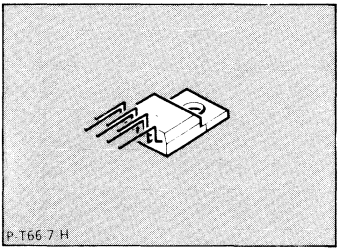
SIEMENS

Power Operational Amplifier

TCA 1365 B

Preliminary Data

Bipolar IC



Features

- High peak output current up to 4 A
- High supply voltage up to 42 V
- Suitable up to gain of 1
- Thermal overload protection
- Internal power limiting
- External compensation
- Inhibit input
- DC short-circuit protection to $+V_S$ and $-V_S$
- Integrated clamp diodes

Applications

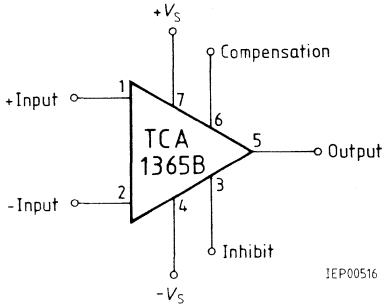
- Power comparator
- Power Schmitt trigger
- Speed control of DC motors
- Power buffer

Type	Ordering Code	Package
TCA 1365 B	Q67000-A8190	Plastic power package P-T66-7-H (similar to TO-220)

9

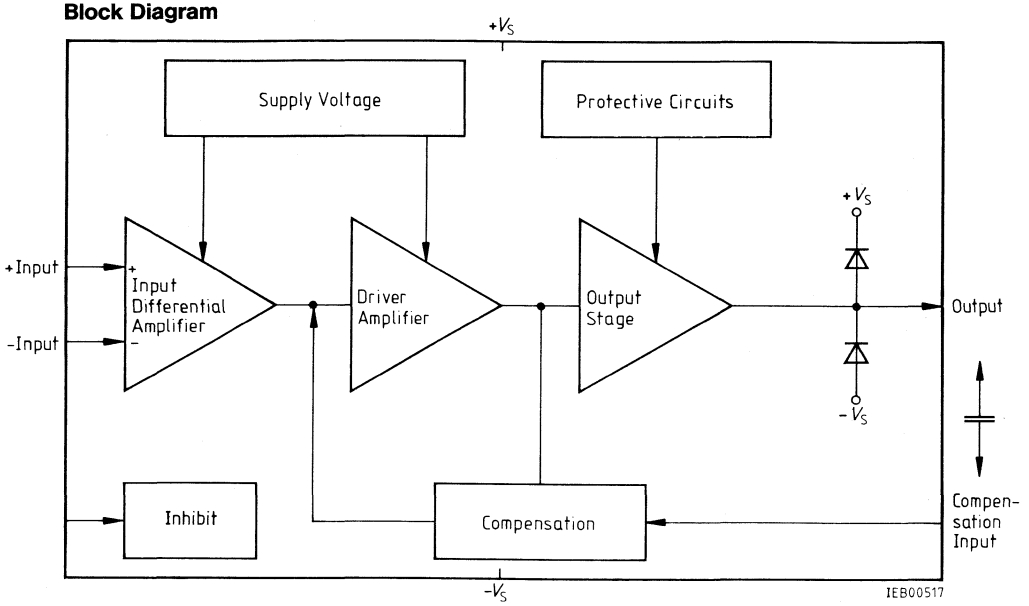
The TCA 1365 B is a power op amp in a plastic power package P-T66-7 H. At maximum supply voltage of ± 21 V it produces a high output current of 4 A. The op amp is protected against short circuits and thermal overload.

Pin Configuration



Pin 4 is electrically connected to cooling fin.

Block Diagram



Absolute Maximum Ratings

$T_A = -25\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage	V_S	0	±21	V	
Differential input voltage	V_{ID}	$-V_S$	$+V_S$	V	
Supply current	I_S	−3.5	+4.0	A	
Output current	I_Q	−4	+4	A	
Output current	I_Q	−2		A	$V_S \geq \pm 15$ V; $V_Q < -V_S$
Output current	I_Q	−3		A	$V_S \geq \pm 10$ V; $V_Q < -V_S$
Ground current	I_{GND}	−4.0	+3.5	A	
Current Pin 3, 6	$I_{3,6}$	0	5	mA	
Power dissipation at $T_C = 85\,°C$	P_D		20	W	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	125	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−25	85	°C	$P_D = 13$ W
Forward current of free-wheel diode	I_F		3	A	$T_{j\,max} = 125\,°C$
Thermal resistance					
junction – ambient	$R_{th\,jA}$		65	K/W	
junction – case	$R_{th\,jC}$		3	K/W	

Characteristics

$V_S = \pm 15$ V, $T_j = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Open-loop supply current consumption	I_S		20	40	mA	1
Input offset voltage	V_{IO}	−10		10	mV	2
Input offset current	I_{IO}	−100		100	nA	3
Input current	I_I		0.2	1	µA	3
Output voltage						
$R_L = 12\ \Omega$; $f = 1$ kHz	$V_{Q\ pp}$	±13.0	±13.5		V	4
$R_L = 4\ \Omega$; $f = 1$ kHz	$V_{Q\ pp}$	±12.5	±13.0		V	
Input resistance $f = 1$ kHz	R_I	4	5		MΩ	4
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70	80		dB	5
Common-mode input voltage	V_{IC}	+13/−15	+13.5/−15.1		V	6
Common-mode rejection	k_{CMR}	70	80		dB	6
Supply voltage rejection	k_{SVR}	−70	−80		dB	7
Temperature coefficient of V_{IO} ($-25\,°C \le T_C \le +85\,°C$)	α_{VIO}		50		µV/K	2
Temperature coefficient of I_{IO} ($-25\,°C \le T_C \le +85\,°C$)	α_{IIO}		0.4		nA/K	3
Slew rate of V_Q for non-inverting operation	SR		0.5		V/µs	8
Slew rate of V_Q for inverting operation	SR		0.5		V/µs	9
Noise voltage referred to input DIN 45405	V_n		2	5	µV	1
Short-circuit current						
(S1 closed)	I_{SC}		0.75		A	1
(S2 closed)	I_{SC}		−0.75		A	1
Open-loop supply current consumption (S3 open; $V_3 \ge 2$ V[1])	I_S		1.5	3.5	mA	1

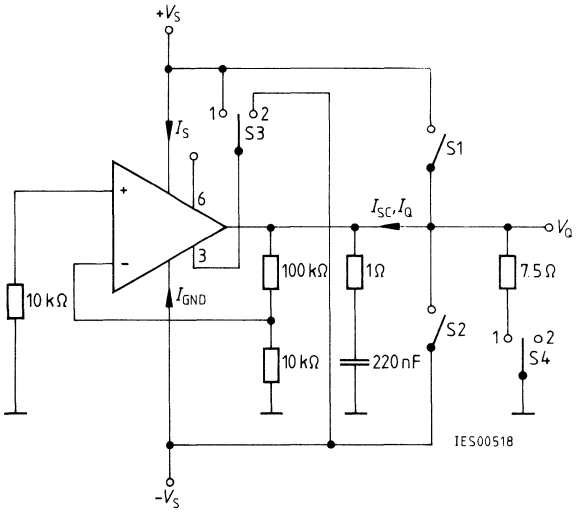
Inhibit Input (pin 3)

V_3 for amp off	$V_{3\ OFF}$	2			V	1
V_3 for amp on[1])	$V_{3\ ON}$			0.5	V	1
Turn-on dead time $I_Q \ge 1$ A[2])	$t_{D\ ON}$		2	5	µs	1
Turn-off dead time $I_Q \le 1$ A[2])	$t_{D\ OFF}$		50	100	µs	1

[1]) referred to $-V_S$
[2]) S4 closed

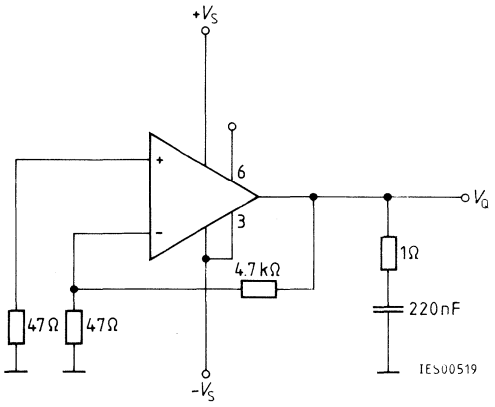
Test and Measurement Circuits

Figure 1
Open-Loop Supply Current Consumption; Noise Voltage



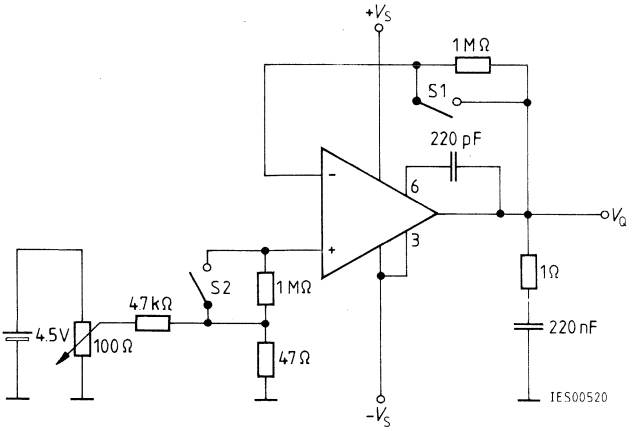
S1 to S4 as shown
unless otherwise specified

Figure 2
Input Offset Voltage, Temperature Coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3
Input Offset Current; Input Current, Temperature Coefficient of I_{IO}



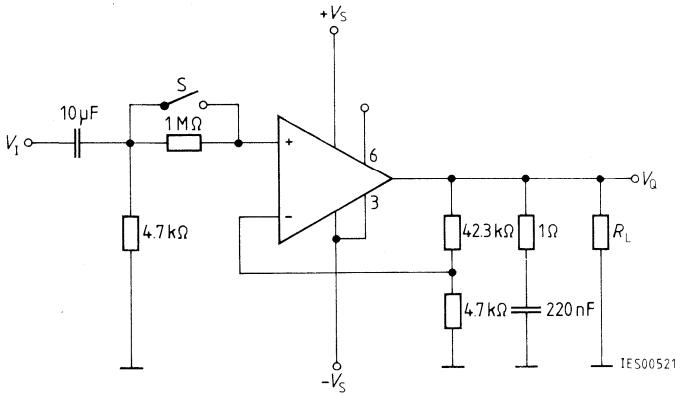
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\ M\Omega}$

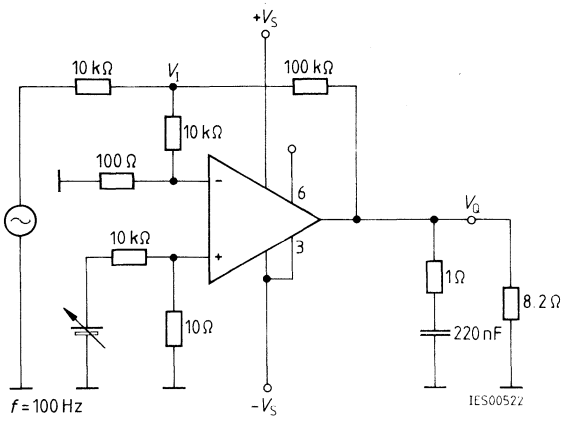
S1 closed – S2 closed: offset alignment

Figure 4
Output Voltage, Input Resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-Loop Voltage Gain



$$G_{V0} = \left| 20 \log 101 \frac{V_Q}{V_I} \right| \text{ [dB]}$$

Figure 6
Common-Mode Voltage Gain G_{VC}
Common-Mode Rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

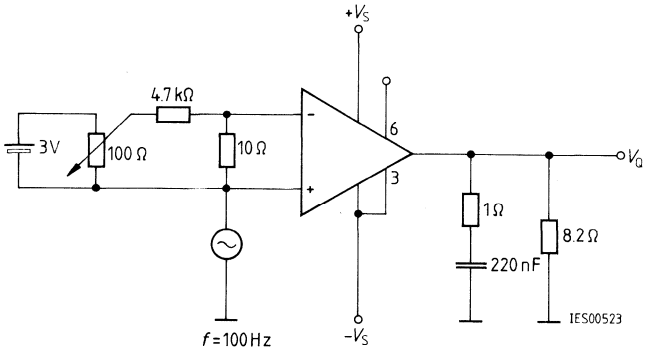
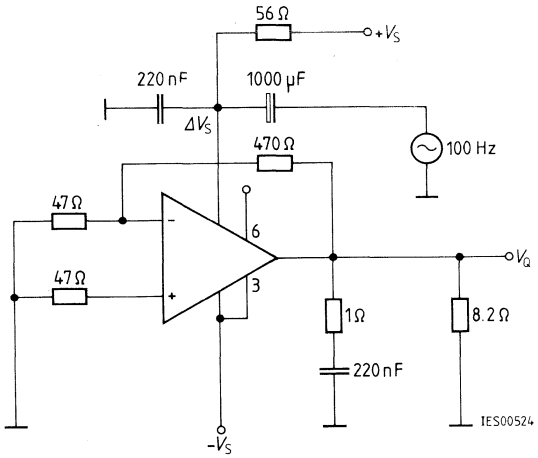


Figure 7
Supply-Voltage Rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ [dB]}$$

Figure 8
Slew Rate for Non-Inverting Operation

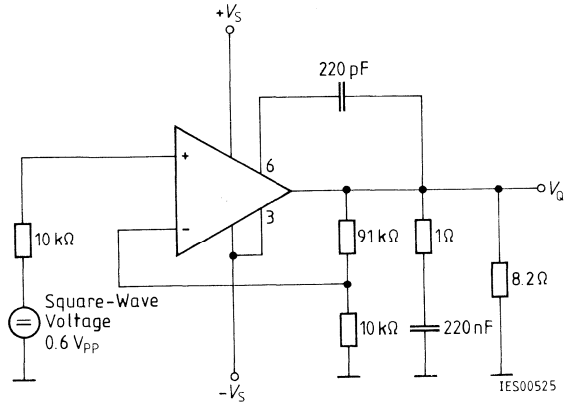
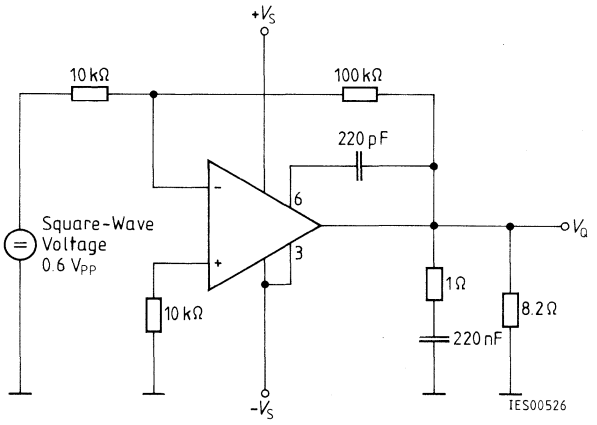
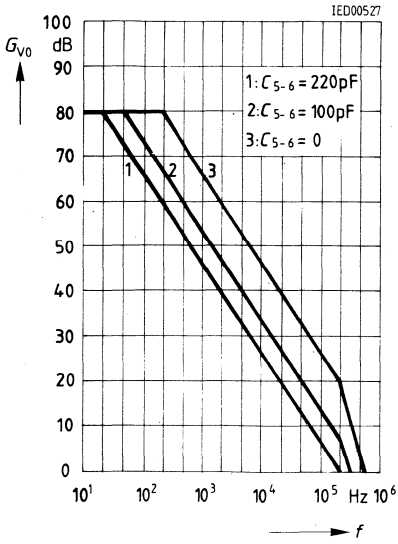


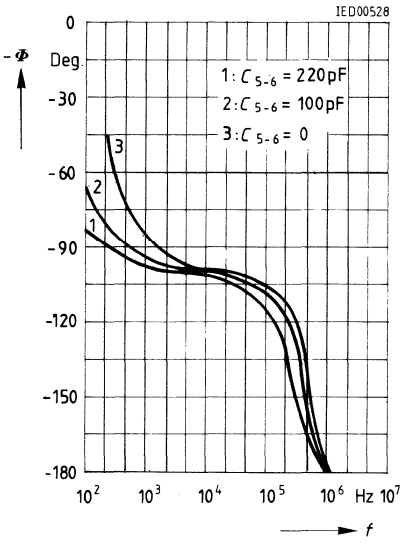
Figure 9
Slew Rate for Inverting Operation



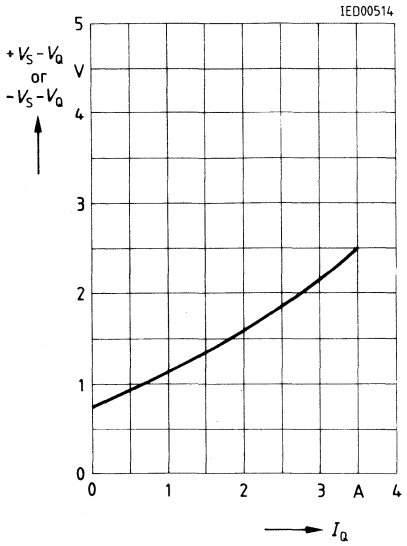
Open-Loop Voltage Gain versus Frequency
$T_j = 25\,°C$; $V_S = \pm 15$ V



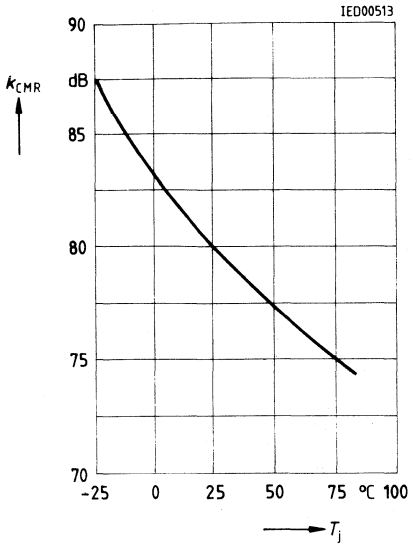
Phase Response versus Frequency
$T_j = 25\,°C$; $V_S = \pm 15$ V



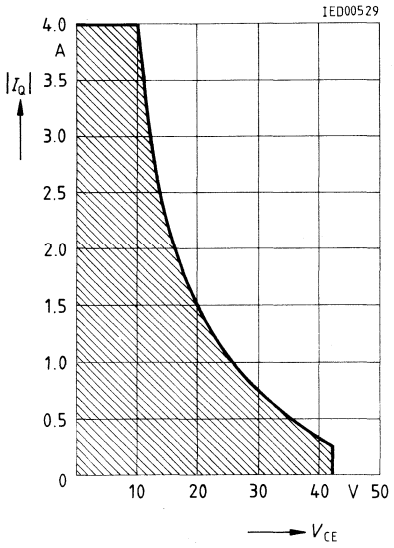
Saturation Voltage versus Output Current
$T_j = 25\,°C$



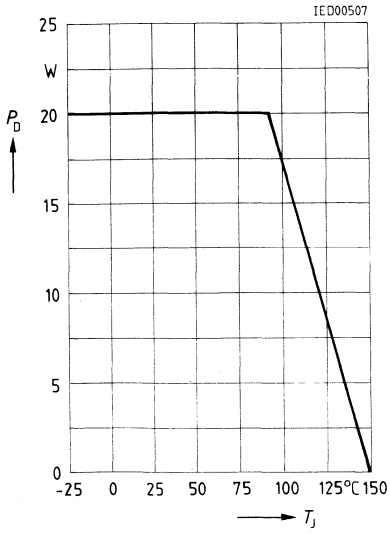
Common-Mode Rejection versus Case Temperature



Safe Operating Area of Output Stage Output Current versus Collector Emitter Voltage
$T_j = 25\,°C$; $V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$

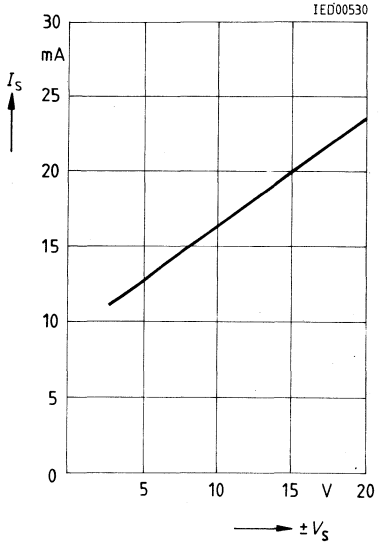


Maximum Permissible Power Dissipation versus Case Temperature

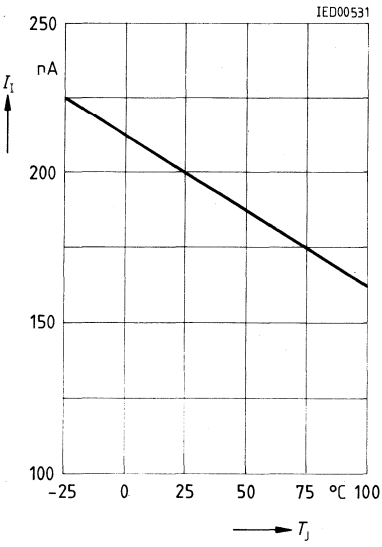


9

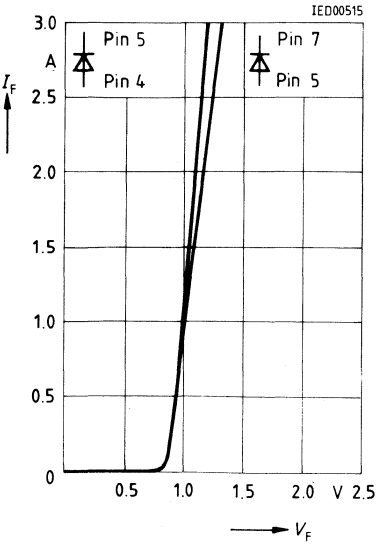
Supply Current versus Supply Voltage
$T_j = 25\,°C$



Input Current versus Junction Temperature
$V_S = \pm 15\,V$



Forward Current versus Forward Voltage
$T_j = 25\,°C$



SIEMENS

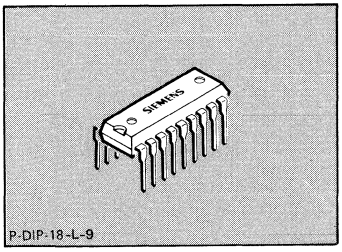
Dual Power Operational Amplifier

TCA 2365

Bipolar IC

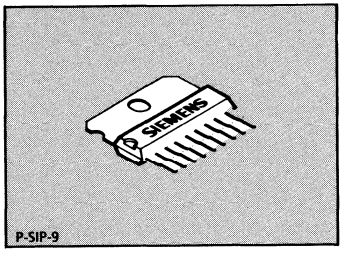
Features

- High output peak current of twice 2.5 A
- Wide supply voltage range, 8 V to 32 V
- High slew rate 4 V/µs
- Outputs entirely protected (DC short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs



Applications

- Power comparator
- Power Schmitt trigger
- Speed control of DC motors



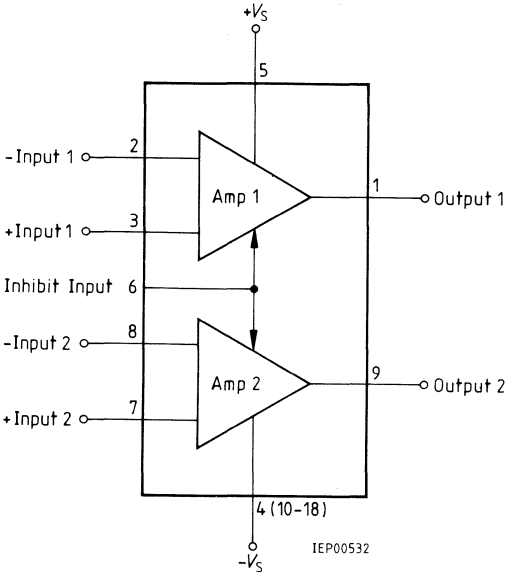
Type	Ordering Code	Package
TCA 2365	Q67000-A1876	P-SIP-9
TCA 2365 A	Q67000-A8017	P-DIP-18-L-9

9

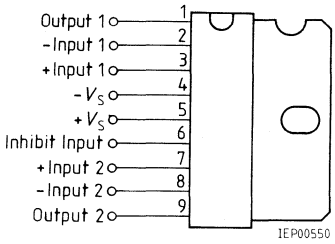
The TCA 2365 is a dual power op amp in a P-SIP-9 or P-DIP-18L-9 package. The IC contains two identical op amps, each supplying a high output peak current of 2.5 A at supply voltages between ±4 V and ±15 V. Both amplifiers can be disconnected simultaneously (tristate; $Z_Q \approx 4$ kΩ) via an inhibit input. Integrated protective circuits protect the outputs against short circuit to $+V_S$ and $-V_S$ and prevent thermal overloading of the IC.

Pin Configuration

TCA 2365A



TCA 2365



Pin 4 is electrically connected to cooling fin.
(Establish external connection between pin 4 and pin 10-18)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		TCA 2365	TCA 2365 A	
Supply voltage	V_S	± 16	± 16	V
t = 50 ms	V_S	± 18	± 18	V
Differential input voltage	V_{ID}	± V_S	± V_S	V
Output voltage range	V_Q	$-V_S$ −1 to $+V_S$ +1		V
Peak output current	I_Q	± 2.5	± 2.5	A
Supply current	I_S	5.5	5.5	A
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−55 to 125	−55 to 125	°C
Thermal resistance				
junction – ambient	$R_{th\ jA}$	65	60	K/W
junction – case	$R_{th\ jC}$	6	10	K/W

Operating Range

Supply voltage	V_S	± 4 to ± 15	± 4 to ± 15	V
Case temperature P_{tot} = 10.0 W	T_C	−25 to 85	−25 to 85	°C
Voltage gain	$G_{V\ min}$	10	10	dB

Characteristics

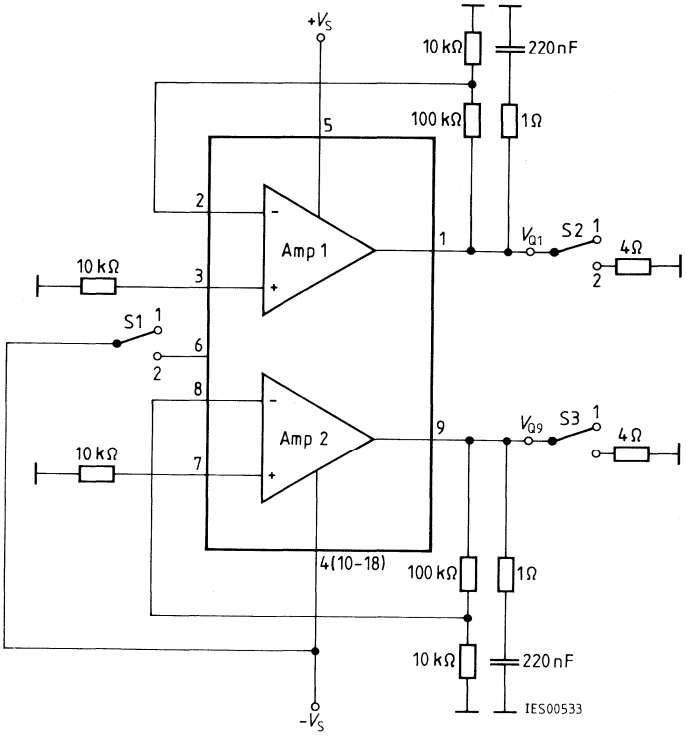
$V_S = \pm 10$ V; $T_j = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Open-loop supply current consumption						
S1 in position 1	I_S		30	50	mA	1
S1 in position 2	I_{SM}		5	8	mA	1
Input offset voltage	V_{IO}	−10		10	mV	2
Input offset current	I_{IO}	−100		100	nA	3
Input current	I_I		0.25	1	µA	3
Output voltage						
($R_L = 12\ \Omega$; $f = 1$ kHz)	$V_{Q\ pp}$	±8.5	±9.0		V	4
($R_L = 4\ \Omega$; $f = 1$ kHz)	$V_{Q\ pp}$	±8.0	±8.5		V	4
($R_L = 470\ \Omega$; $f = 50$ kHz)	$V_{Q\ pp}$		±6.0		V	4
Input resistance ($f = 1$ kHz)	R_I	1	5		MΩ	4
Open-loop voltage gain ($f = 100$ Hz)	G_{VO}	70	80		dB	5
Common-mode input voltage range	V_{IC}	+7/−10	+7.5/−10.5		V	6
Common-mode rejection	k_{CMR}	70	80		dB	6
Supply voltage rejection	k_{SVR}	70	80		dB	7
Temperature coefficient of V_{IO} $-25\ °C \le T_j \le +85\ °C$	α_{VIO}		50		µV/K	2
Temperature coefficient of I_{IO} $-25\ °C \le T_j \le +85\ °C$	α_{IIO}		0.4		nA/K	3
Slew rate of V_q for non-inverting operation[1])	SR		4		V/µs	8
Slew rate of V_q for inverting operation[1])	SR		4		V/µs	9
Noise voltage referred to input	V_n		3		µV	1
Inhibit input (referred to $-V_S$)						
V_6 for IC turned off	$V_{6\ OFF}$	0		1.0	V	1
V_6 for IC turned on	$V_{6\ ON}$	3.0		6	V	1
Turn-on time $\lvert I_{1;9} \rvert > 1$ A	$t_{D\ ON}$		2	5	µs	1
Turn-off time $\lvert I_{1;9} \rvert < 1$ A referred to $V_{6\ OFF/ON}$	$t_{D\ OFF}$		15	30	µs	1
S2 and S3 in position 2						

[1]) For the relationship between power bandwidth and slew rate refer to **"General Information"**

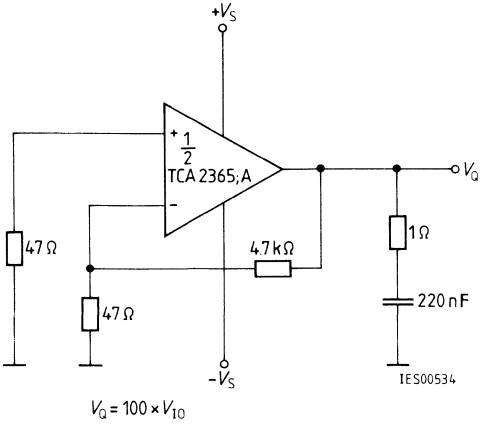
Test Circuits

Figure 1
Open-Loop Supply Current Consumption, Noise Voltage, Turn-Off Voltage



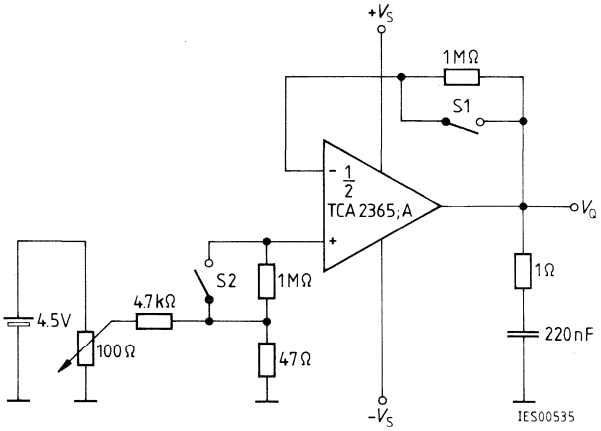
Switch as drawn unless otherwise specified.

Figure 2
Input Offset Voltage, Temperature Coefficient of V_{IO}



$V_Q = 100 \times V_{IO}$

Figure 3
Input Offset Current, Input Current, Temperature Coefficient of I_{IO}



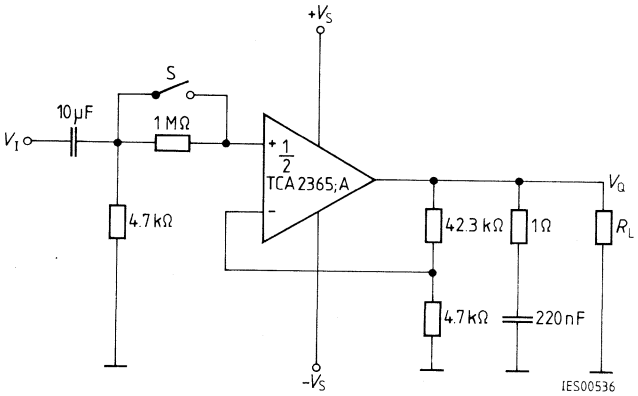
S1 open — S2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

S2 open — S1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$

S1 open — S2 open: $I_{IO} = \frac{V_Q}{1\ M\Omega}$

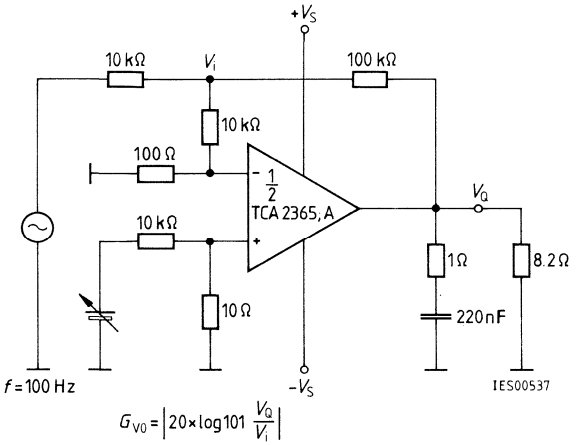
S1 closed — S2 closed: offset alignment

Figure 4
Output Voltage, Input Resistance



S closed: to measure V_{Qpp}
S open / closed: to measure R_I

Figure 5
Open-Loop Voltage Gain



$$G_{V0} = \left| 20 \times \log 101 \frac{V_Q}{V_i} \right|$$

Figure 6
Common-Mode Voltage Gain G_{VC}
Common-Mode Rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

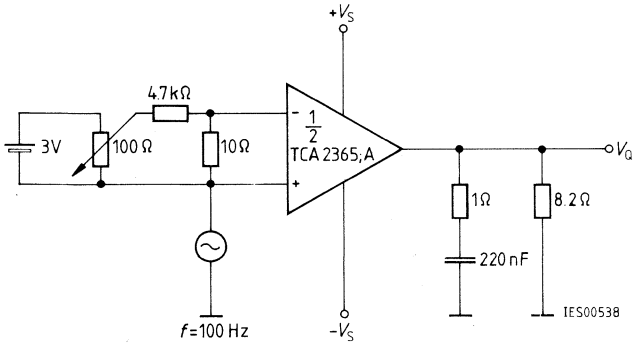
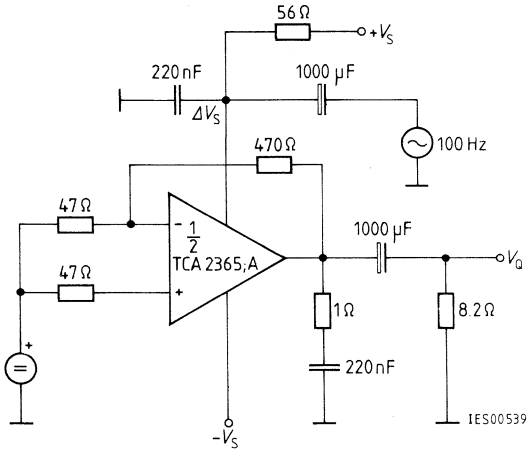


Figure 7
Supply Voltage Rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \cdot \Delta V_S} \text{ [dB]}$$

Figure 8
Slew Rate for Non-Inverting Operation

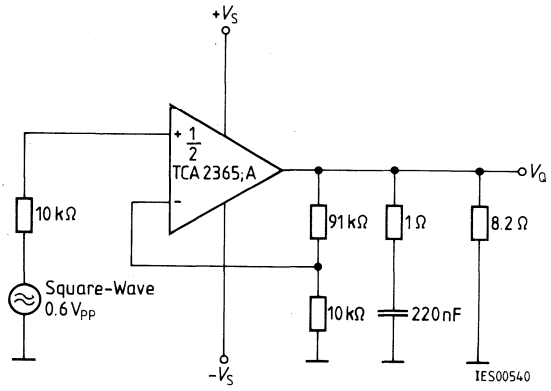
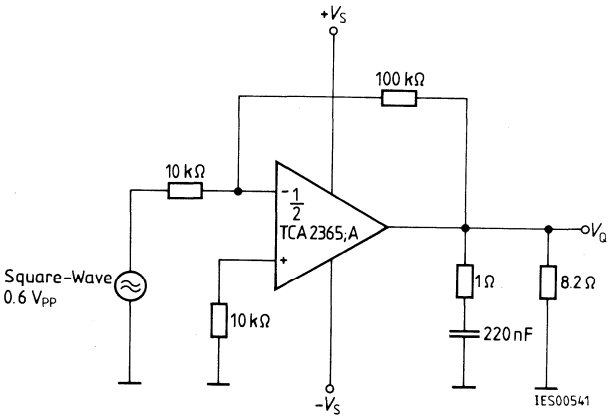
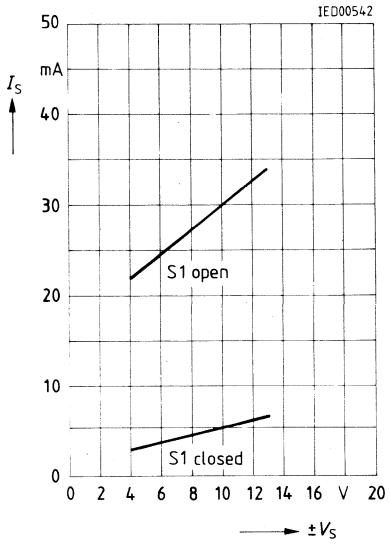


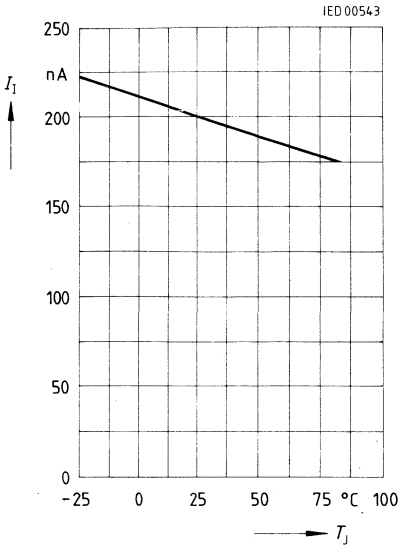
Figure 9
Slew Rate for Inverting Operation



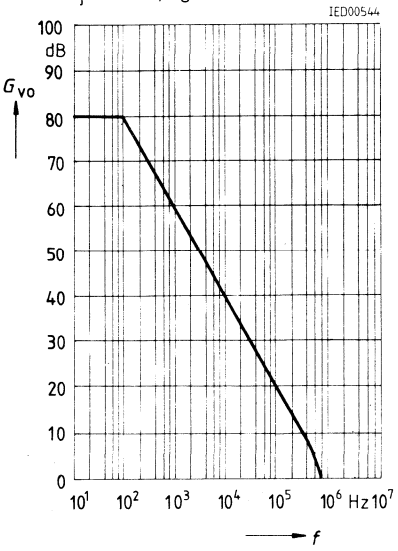
Supply Current I_S and I_{SM} versus Supply Voltage
$T_j = 25\,°C$



Input Current versus Junction Temperature

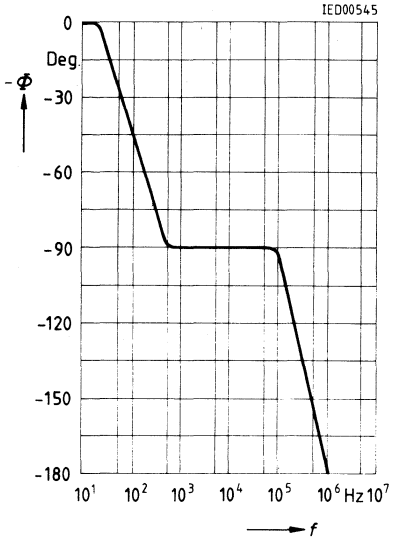


Open-Loop Voltage Gain versus Frequency
$T_j = 25\,°C$; $V_S = \pm 10$ V

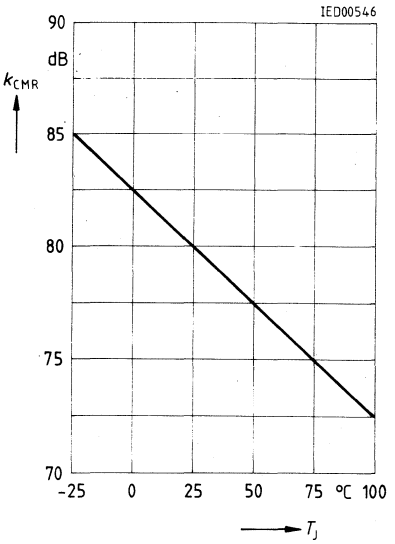


9

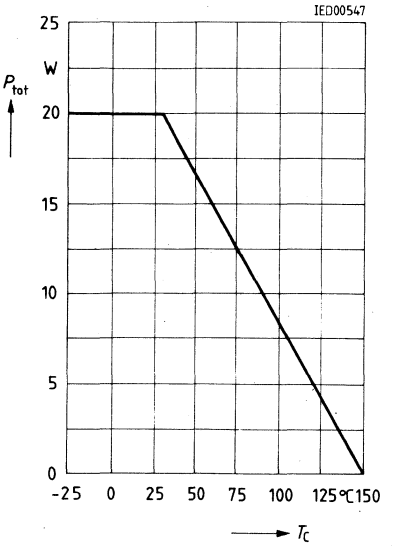
Phase Response versus Frequency
$T_j = 25\,°C$; $V_S = \pm 10$ V



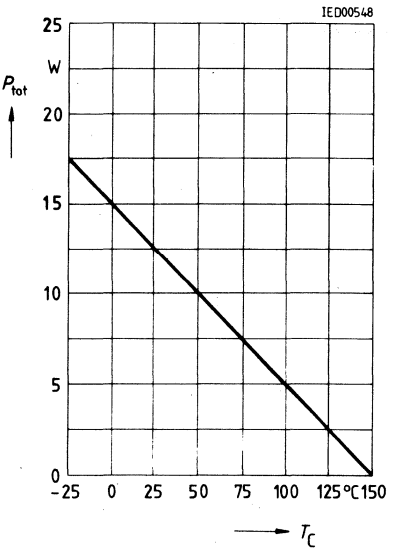
Common-Mode Rejection versus Junction Temperature
$V_S = \pm 10$ V



Max. Permissible Power Dissipation versus Case Temperature



Max. Permissible Power Dissipation versus Case Temperature



SIEMENS

Dual Power Operational Amplifier

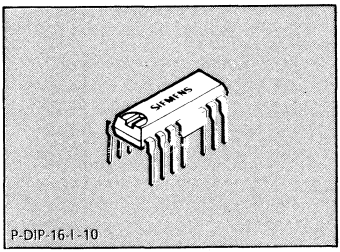
TCA 2465

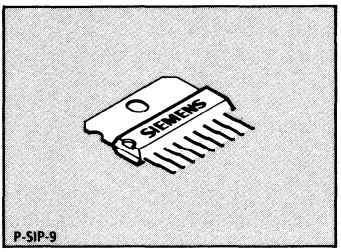
Advance Information: TCA 2465 G

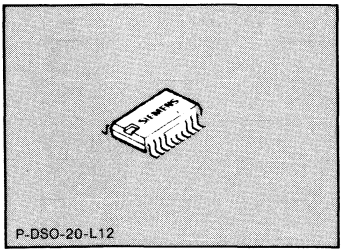
Bipolar IC

Features

- High output peak current of twice 2.5 A
- Twice 2.0 A output peak current for TCA 2465 G
- Large supply voltage range up to 42 V
- High slew rate of 2 V/µs
- Outputs fully protected (DC short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs
- Integrated clamp diodes







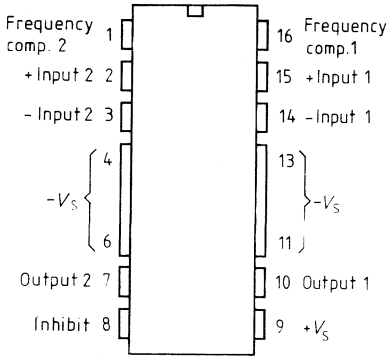
Type	Ordering Code	Package
TCA 2465	Q67000-A8109	P-SIP-9
TCA 2465 A	Q67000-A8110	P-DIP-16-L-10
▼ TCA 2465 G	Q67000-A8334	P-DSO-20-L-12

▼ New type

The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ± 3 V and ± 20 V. Internal compensation permits negative feedback of the amplifiers up to a min. of 20 dB. If a voltage gain of 0 to 20 dB is required, the TCA 2465 A can be compensated with external capacitors from pin 7 to 1 or pin 10 to 16. Both amplifiers can be disconnected at $V_8 \geq 2$ V via an inhibit input. Integrated protective circuits protect the outputs against short-circuit to $+V_S$ and $-V_S$ and prevent thermal overloading of the IC. TCA 2465 G comes in a special surface-mounted power package similar to P-DSO-20 and delivers twice 2.0 A output peak current.

Pin Configuration
(top view)

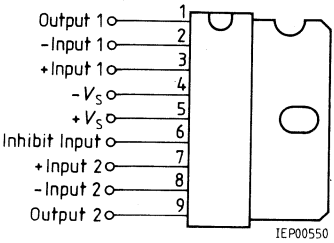
P-DIP-16-L10
(TCA 2465 A)



IEP 00549

Pin Configuration

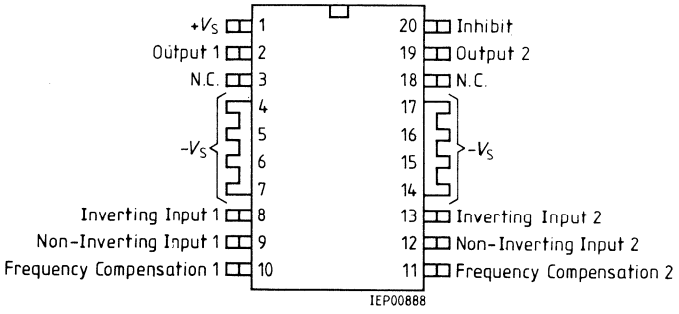
P-SIP-9
(TCA 2465)



IEP00550

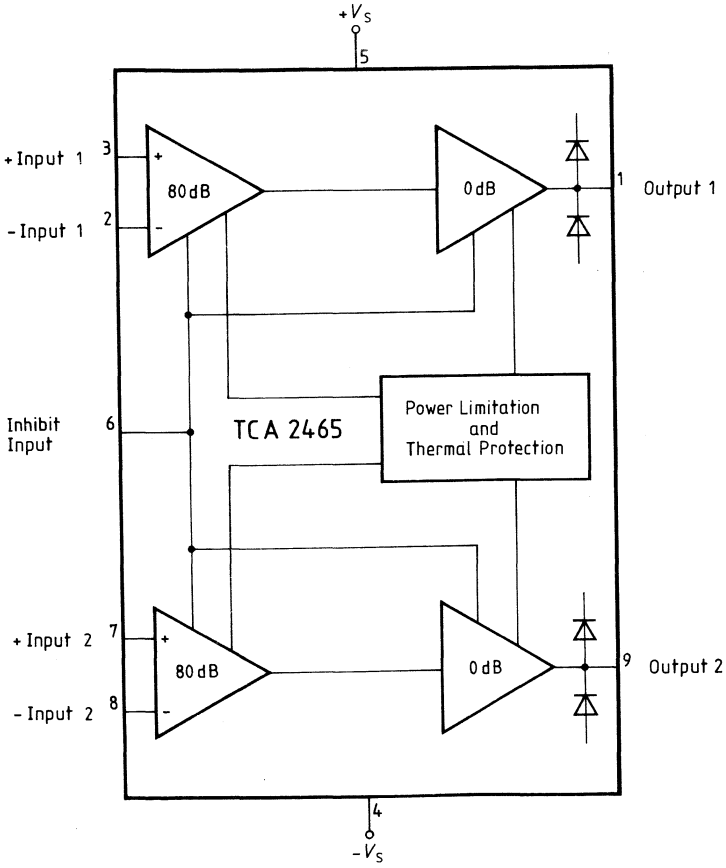
Pin Configuration, Advance Information

P-DSO-20-L12
(TCA 2465 G)

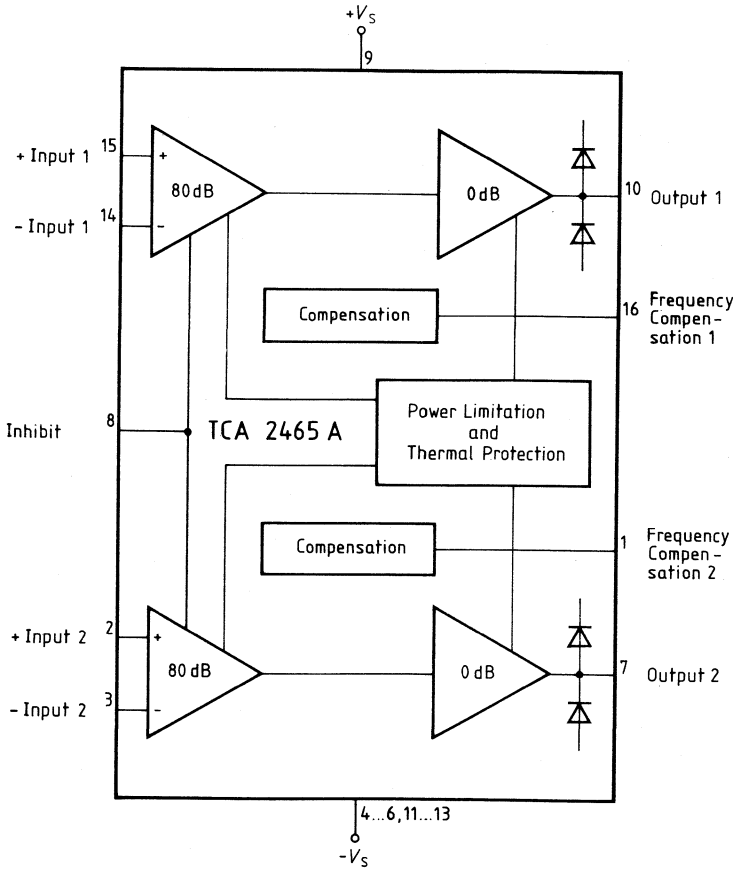


IEP00888

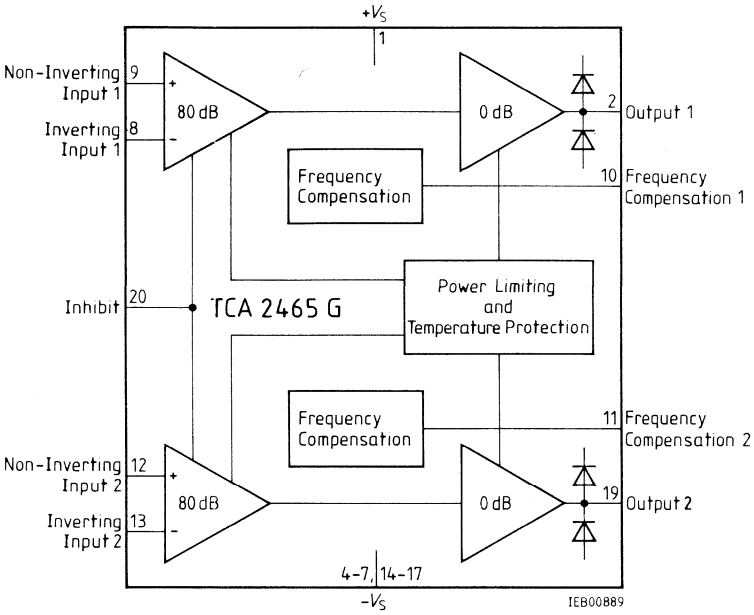
Block Diagram
TCA 2465



Block Diagram
TCA 2465 A



Block Diagram
TCA 2465 G



9

Absolute Maximum Ratings

$T_C = -40\,°C$ to $85\,°C$

Note: Values in brackets refer to TCA 2465G

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Supply voltage	V_S		±21	V	
Differential input voltage	V_{ID}		$(-V_S)+(+V_S)$	V	$\Delta V_{2\text{-}3}$ or $\Delta V_{8\text{-}7}$
Output current	I_Q	−2.5 (−2.0)	2.5 (2.0)	A	I_1 or I_9
Output current	I_Q	−1.5		A	$V_S \geq \pm 15$ V; $V_Q < -V_S$
Supply current	I_S	−5 (−2.0)	5.5 (2.0)	A	I_S
Ground current	I_{GND}	−5.5 (−2.0)	5 (2.0)	A	I_4
Input voltage	V_I	$-V_S$	$+V_S$	V	V_2, V_3, V_7, V_8
Inhibit input	V_6	$-V_S$	$+V_S$	V	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	125	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−40	85	°C	$P_D = 12$ W
Voltage gain	$G_{V\,min}$	20		dB	
Thermal resistance					
junction – ambient	$R_{th\,jA}$		60 (70)	K/W	
junction – case	$R_{th\,jC}$		5 (15)	K/W	

Characteristics

$V_S = \pm 10$ V; $T_j = 25$ °C

Note: Values in brackets refer to TCA 2465A; G

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Open-loop supply current consumption S1 in position 1 and 2	I_S		30	50	mA	1
Input offset voltage	V_{I0}	−10		10	mV	2
Input offset current Input current	I_{I0} I_I	−100	 0.25	100 1	nA µA	3 3
Output voltage R_L = 12 Ω; f = 1 kHz R_L = 4 Ω; f = 1 kHz R_L = 470 Ω; f = 40 kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 ±8.5 ±8.0	 ±9.0 ±8.5 (±9.0) ±8.0		 V V V	 4 4 4
Input resistance f = 1 kHz	R_I	1	5		MΩ	4
Open-loop voltage gain f = 100 kHz	G_{V0}	70	80		dB	5
Common-mode input voltage range	V_{IC}	+7/−10	+7.5/−10.5		V	6
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	70 70	80 −80		dB dB	6 7
Temperature coefficient of V_{I0} −40 °C ≤ T_j ≤ +85 °C Temperature coefficient of I_{I0} −40 °C ≤ T_j ≤ +85 °C	α_{VI0} α_{II0}		50 0.4		µV/K nA/K	2 3
Slew rate of V_Q for non-inverting operation Slew rate of V_Q for inverting operation	SR SR		2 (0.5) 2 (0.5)		V/µs V/µs	8 9
Noise voltage (DIN 45405, referred to input)	V_n		3		µV	1
Inhibit input (referred to $-V_S$) V_6 for IC turned off V_6 for IC turned on	 $V_{6\,OFF}$ $V_{6\,ON}$	 2.0		 0.8	 V V	 1 1
H input current, V_6 = 5 V[1]) L input current, V_6 = 0 V[1])	I_{6H} I_{6L}		0.1 0.5	0.5 3.0	µA µA	1 1
Turn-on dead time $\lvert I_{1;9} \rvert > A^2$) Turn-off dead time $\lvert I_{1;9} \rvert < 1\ A^2$) } referred to $V_{6\,OFF/ON}$	$t_{D\,ON}$ $t_{D\,OFF}$		10 10	20 20	µs µs	1 1
Short-circuit current (switch S3 closed) Short-circuit current (switch S4 closed)	I_{SC} I_{SC}		1 1		A A	1 1

[1]) referred to $-V_S$ [2]) Switch S2 closed

Test Circuits

Figure 1
Open-Loop Supply Current Consumption; Noise Voltage

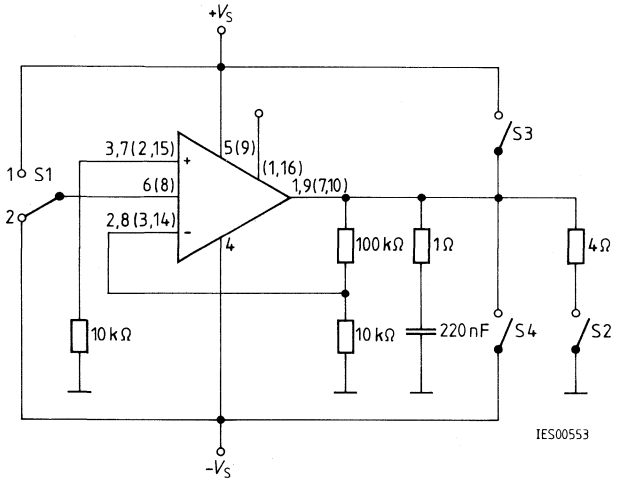
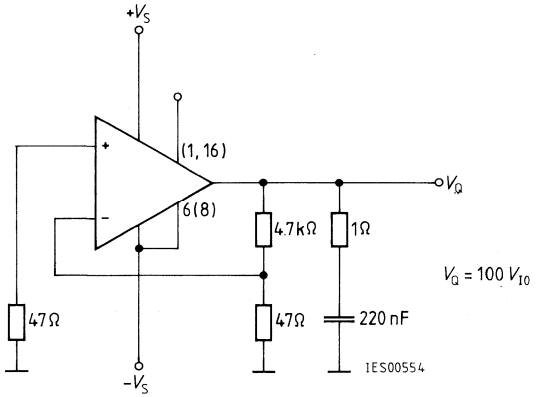


Figure 2
Input Offset Voltage; Temperature Coefficient of V_{IO}



Note: Values in brackets refer to TCA 2465A

Figure 3
Input Offset Current; Input Current; Temperature Coefficient of I_{IO}

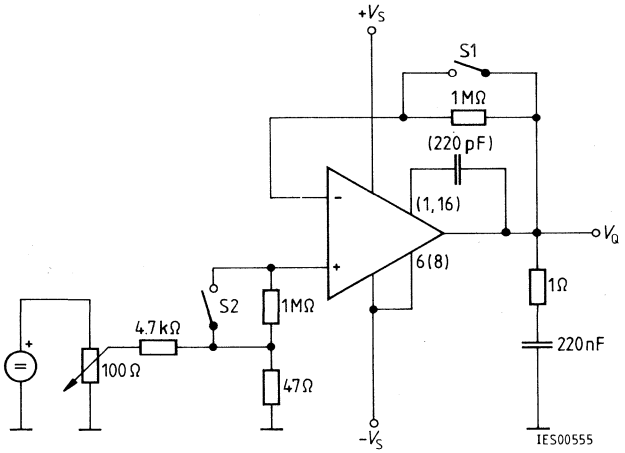
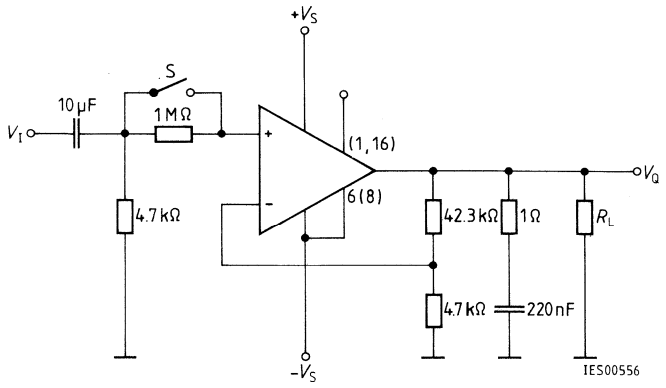


Figure 4
Output Voltage; Input Resistance



Note: Values in brackets refer to TCA 2465A.

Figure 5
Open-Loop Voltage Gain G_{V0}

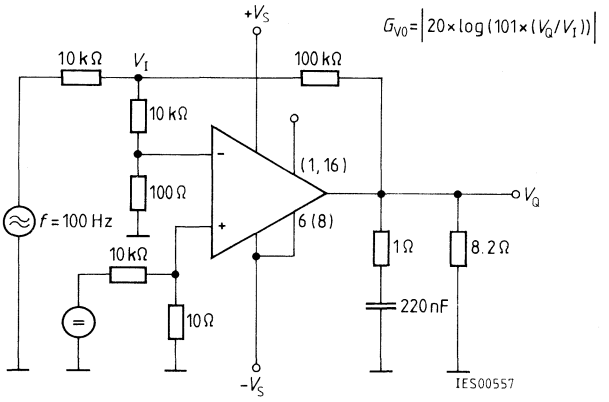
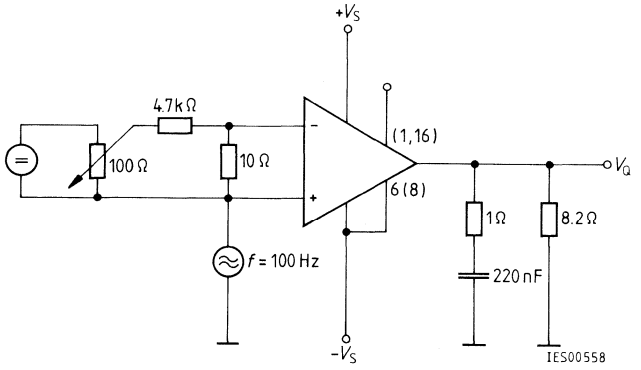


Figure 6
Open-Loop Voltage Gain G_{VC}
Common-Mode Rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)



Note: Values in brackets refer to TCA 2465A.

Figure 7
Supply Voltage Rejection k_{SVR}

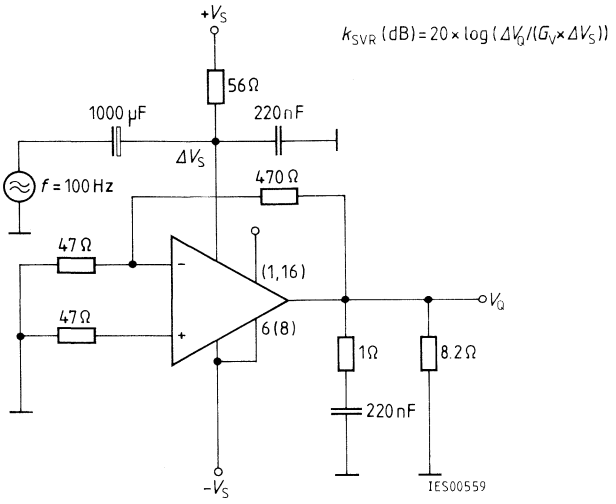
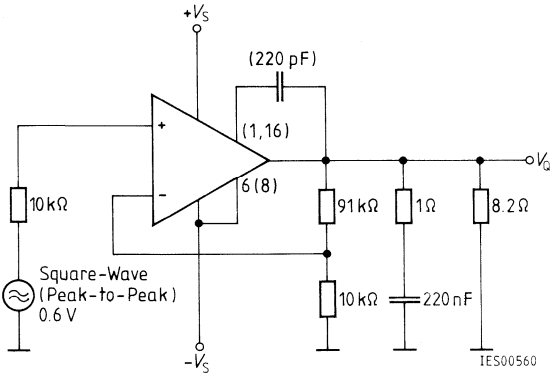
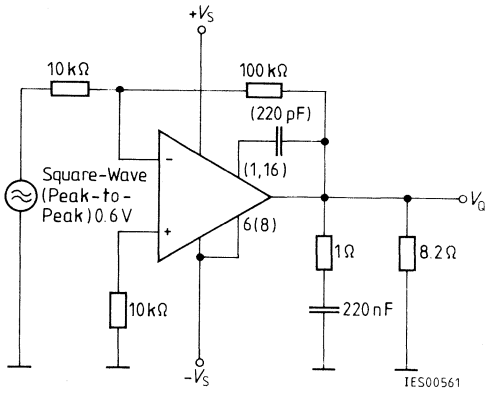


Figure 8
Slew Rate for Non-Inverting Operation



Note: Values in brackets refer to TCA 2465A.

Figure 9
Slew Rate for Inverting Operation

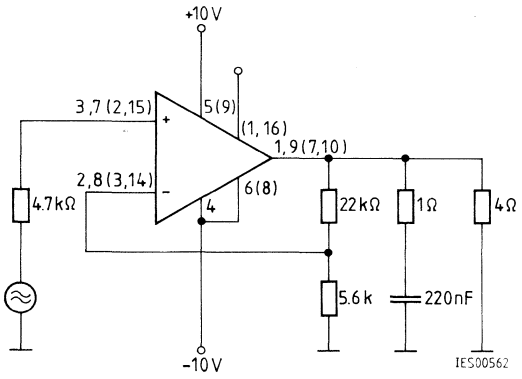


Note: Values in brackets refer to TCA 2465A.

Application Circuits

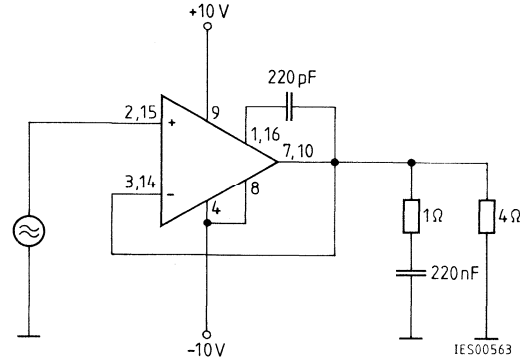
Figure 10
Non-Inverting Operation

a) Amplifier; $G_V = 5$



Note: Values in brackets refer to TCA 2465A.

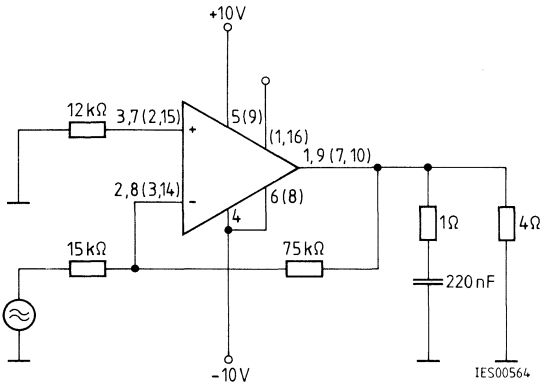
b) Voltage follower TCA 2465A



9

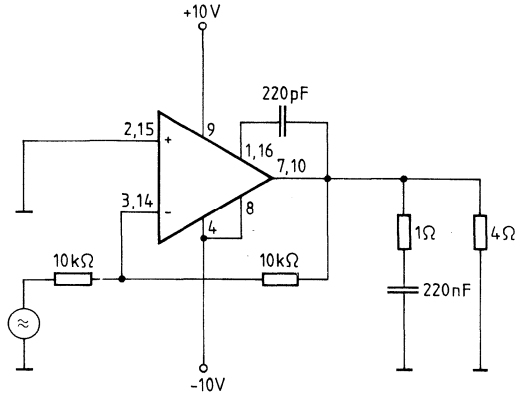
Figure 11
Inverting Operation

a) Amplifier; $G_V = -5$

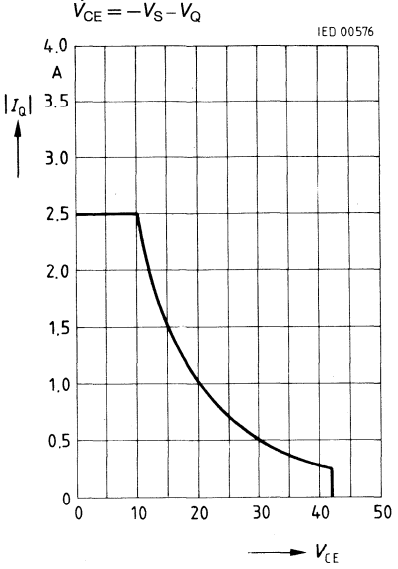


Note: Values in brackets refer to TCA 2465A.

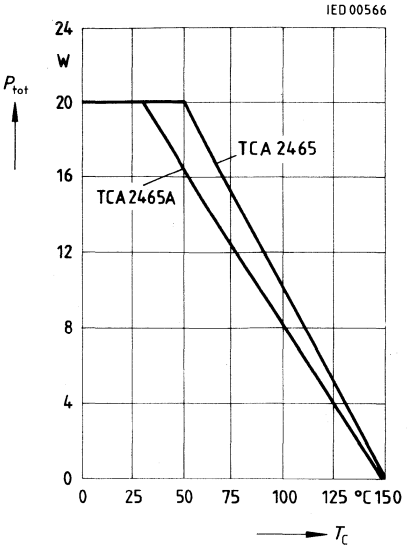
b) Inverter TCA 2465A



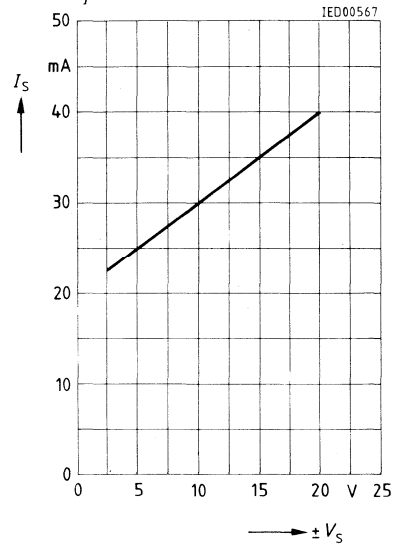
Safe Operating Area (SOA)
Peak Output Current versus
Collector-Emitter Voltage
$T_j = 25\,°C$, $V_{CE} = +V_S - V_Q$ or
$V_{CE} = -V_S - V_Q$



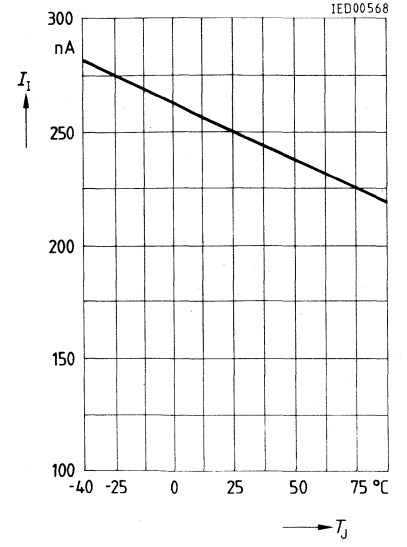
Max. Permissible Power Dissipation
versus Case Temperature



Supply Current versus
Supply Voltage
$T_j = 25\,°C$

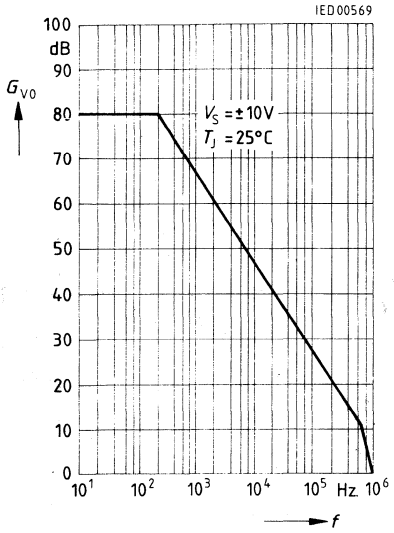


Input Current versus
Junction Temperature
$V_S = \pm 10\,V$

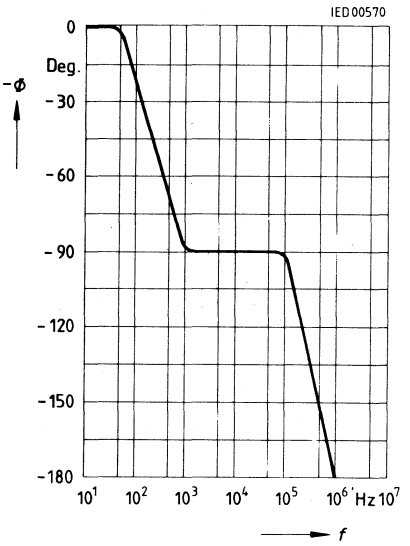


9

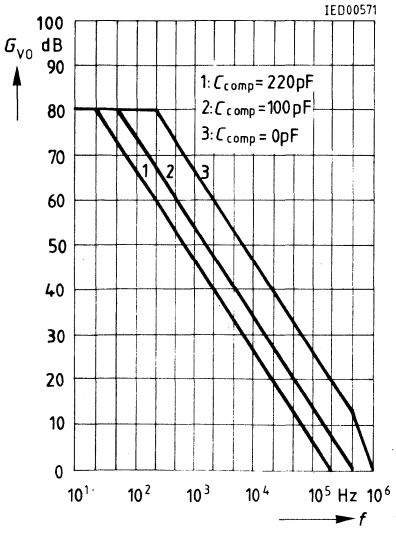
Open-Loop Voltage Gain versus Frequency



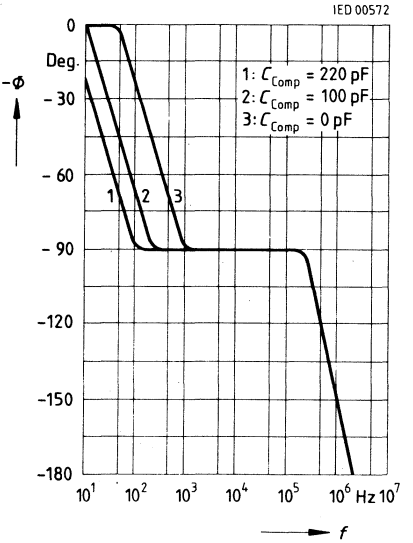
Phase Response versus Frequency
$V_S = \pm 10$ V; $T_C = 25$ °C



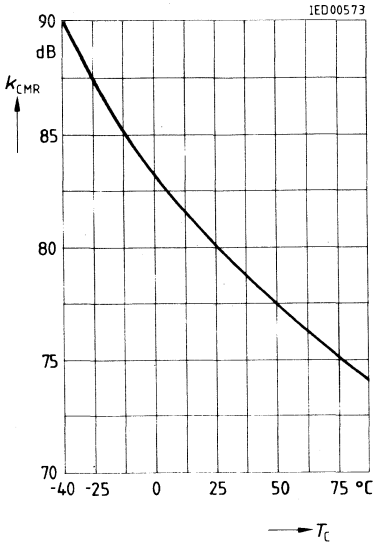
TCA 2465 A, G
Open-Loop Voltage Gain versus Frequency
$V_S = \pm 10$ V, $T_j = 25$ °C



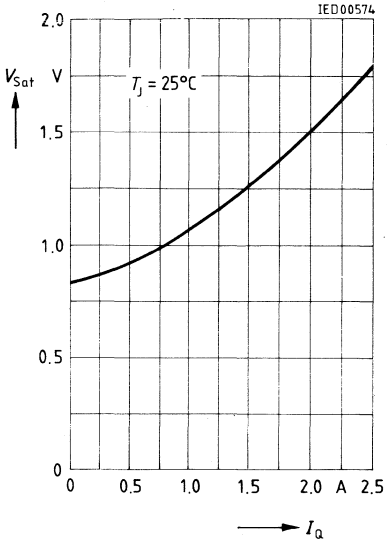
TCA 2465 A, G
Phase Response versus Frequency
$V_S = \pm 10$ V; $T_j = 25$ °C



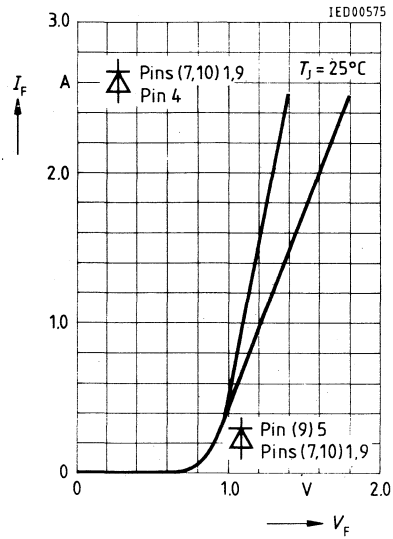
Common-Mode Rejection versus Case Temperature
$V_S = \pm 10$ V



Saturation Voltage versus Peak Output Current
$T_j = 25$ °C



Forward Current versus Forward Voltage



Note: Numbers in brackets refer to TCA 2465 A.

SIEMENS

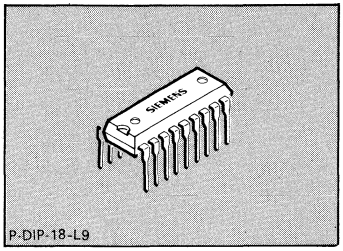
DC Motor Driver

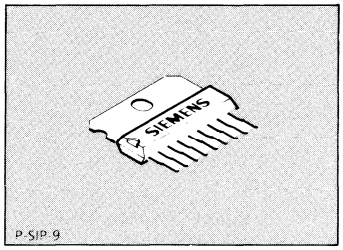
TLE 4201

Features

Bipolar IC

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection





Type	Ordering Code	Package
S TLE 4201 A1	Q67000-A8080	P-DIP-18-L9
S TLE 4201 S1	Q67000-A2285	P-SIP-9

The TLE 4201 IC is a dual comparator that is particularly suitable for driving reversible DC motors and may also be used as a versatile power driver.

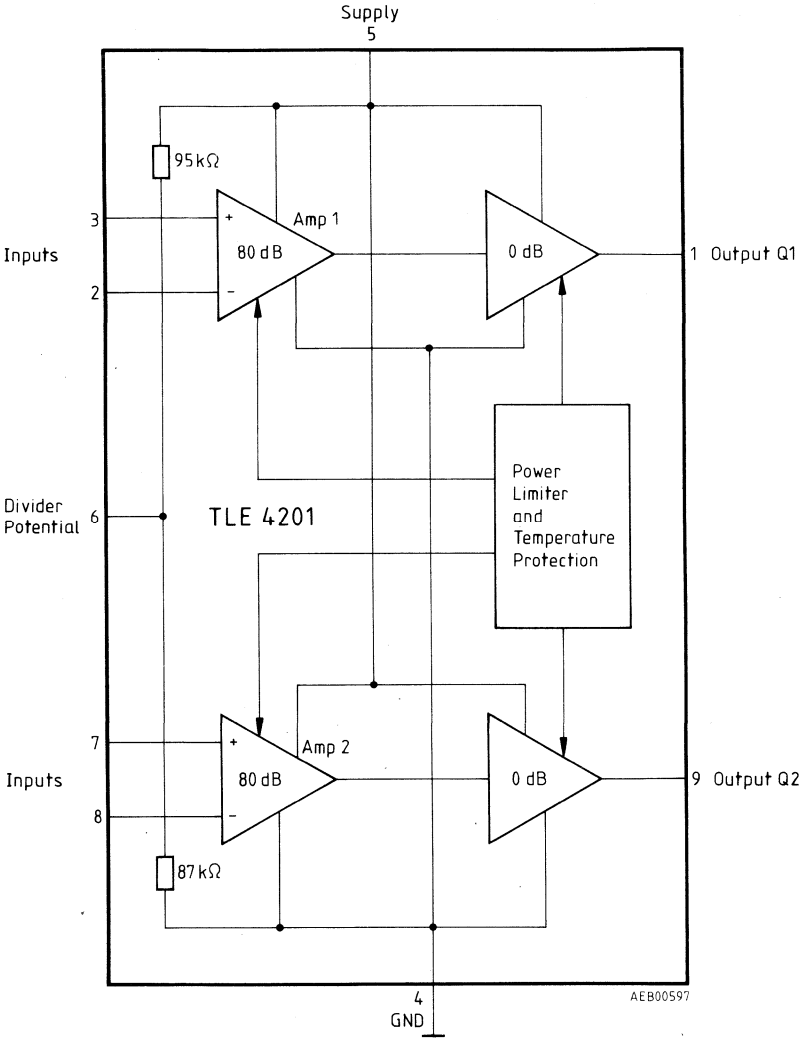
The push-pull power-output stages work in switch mode and can be combined into a full-bridge configuration.

Driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

The TLE 4201 IC comes in two different packages: with the P-SIP-9 package it is possible to remove the heat by way of a cooling fin to a suitable heat sink, whereas with the P-DIP-18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

Figure 1
Block Diagram



Pin Definitions and Functions

TLE 4201 A1 Pin	TLE 4201 S1 Pin	Function
1	1	Output of 1st amplifier
2	2	Inverting input of 1st amplifier
3	3	Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7	7	Non-inverting input of 2nd amplifier
8	8	Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18		Ground; to be connected to pin 4

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SOA protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_s/2$ is available at pin 6 **(see application circuit 2).** This makes the IC particularly suitable as power driver for digital circuits.

Application

Figure 2 shows a window discriminator operation with the control voltage V_I.

The window within which the motor is to stop is set by R_2.

Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application Circuits

Figure 2
Operated as Window Discriminator

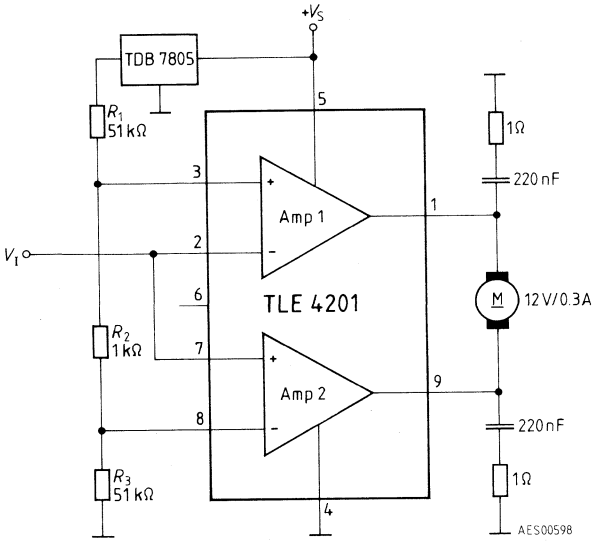
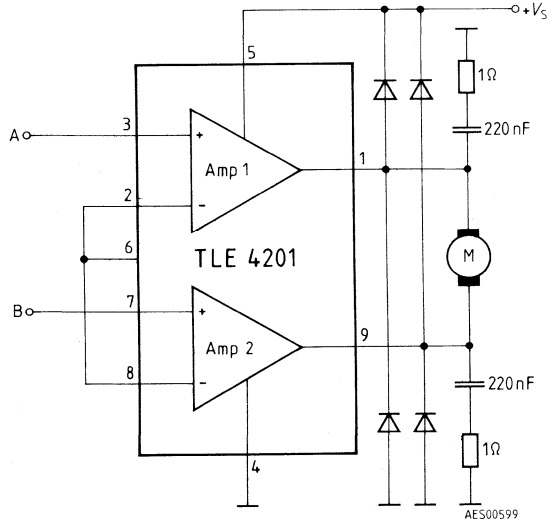


Figure 3
Digital Control
for input signals applies: H ≥ 0.6 V_S
L ≤ 0.3 V_S



Absolute Maximum Ratings

$T_C = -40\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S		25	V
Supply voltage ($t \leq 50$ ms)	V_S		36	V
Output current	I_Q		2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	−0.3	V_S	V
Voltage of pins 1, 9	V	−0.3		V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
TLE 4201 S1 system – air	$R_{th\ JA}$		65	K/W
system – case	$R_{th\ JC}$		8	K/W
TLE 4201 A1 system – air[1])	$R_{th\ JA}$		60	K/W
system – PC board[1])	$R_{th\ JA1}$		44[1])	K/W

Operating Range

Supply voltage	V_S	3.5	17	V
Case temperature	T_C	−40	85	°C
Voltage gain (at negative feedback with external components)	G_V	25		dB

Characteristics

$V_S = 13$ V, $T_C = 25\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions	
Supply current	I_S		20	30	mA	**figure 4:** S = 1	
Open-loop voltage gain	G_{V0}		80		dB	$f = 500$ Hz	
Input resistance	R_I	1	5		MΩ	$f = 1$ kHz	
Saturation voltages						**figure 5:**	S1
Source operation	$V_{Q\ 10}$		1.0	1.1	V	$I_Q = 0.3$ A	1
			1.2	1.6	V	$I_Q = 1.0$ A	1
Sink operation	$V_{Q\ 20}$		0.35	0.5	V	$I_Q = -0.3$ A	2
			0.7	1.0	V	$I_Q = -1.0$ A	2
Rise time of V_Q	t_r		1.5		µs	**figure 4 and 6**	
Fall time of V_Q	t_f		1.5		µs	**figure 4 and 6**	
Turn-on delay time	t_{ON}		3.0		µs	**figure 4 and 6**	
Turn-off delay time	t_{OFF}		1.5		µs	**figure 4 and 6**	
Input current (pins 2, 3, 7, 8)	I_I		1.5	3.0	µA	**figure 5** $V_{2,3,7,8} = 0$	
Input offset voltage	V_{I0}	−5		5	mV	**figure 7**	

[1]) **see figure 8**

Figure 4
Test and Measurement Circuits

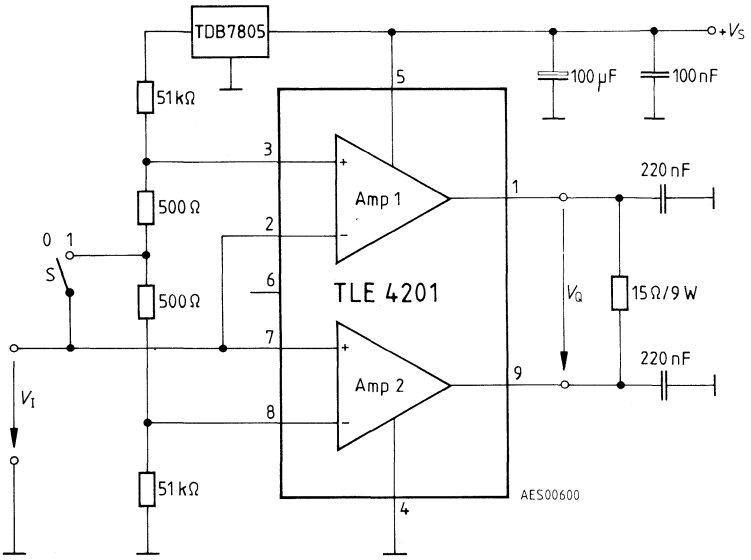


Figure 5

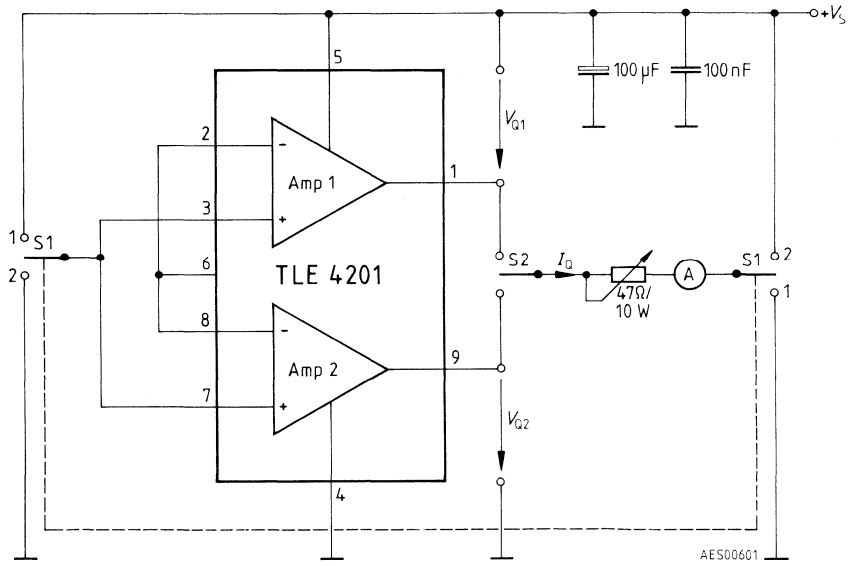


Figure 6
Pulse Diagram

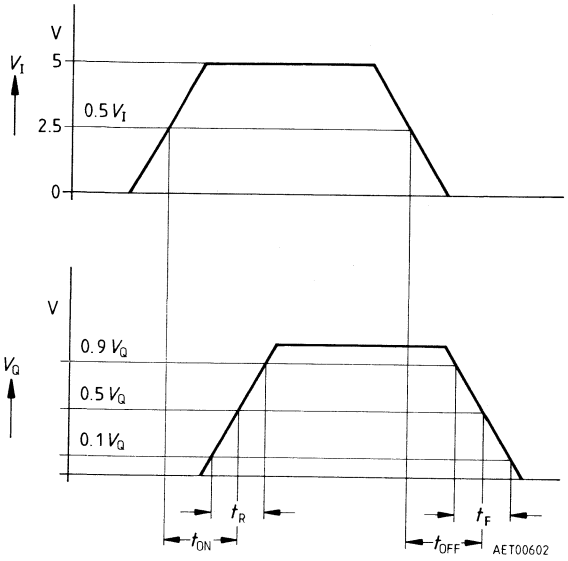
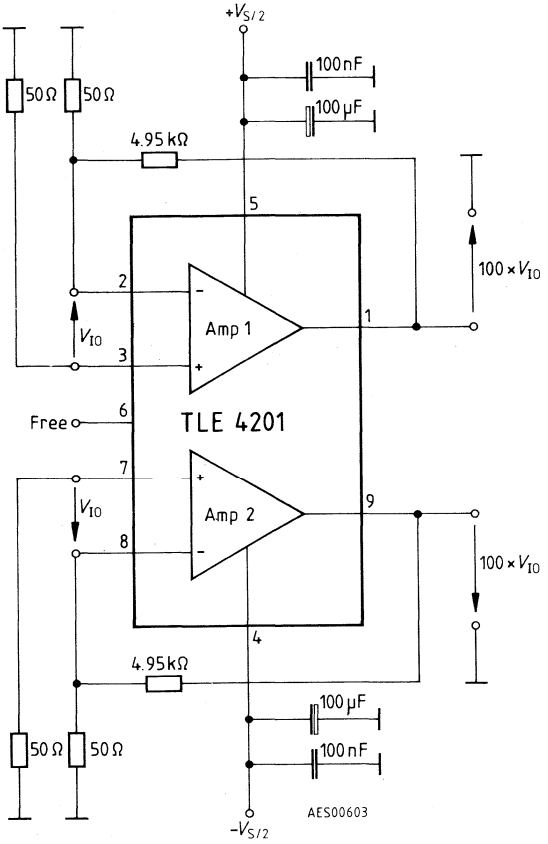


Figure 7
Test and Measurement Circuit

Input Offset Voltages

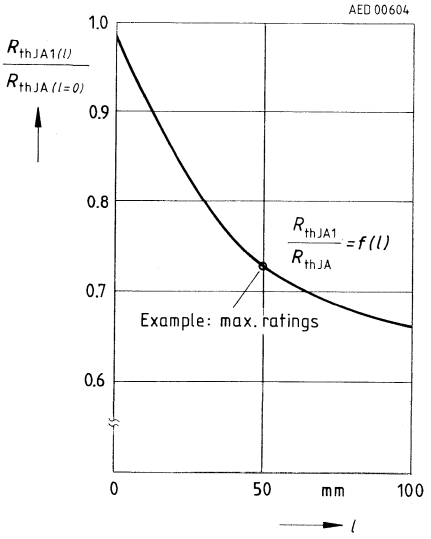


Thermal Resistance of TLE 4201 A1

Thermal resistance, junction-air, $R_{th\ JA\ 1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\ JA}$ $(l = 0) = 60$ K/W
$T_A \leq 70$ °C
$P_V = 1$ W
substrate vertical
circuit vertical
still air

Figure 8



SIEMENS

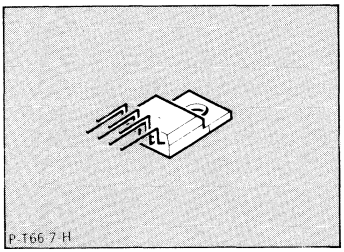
DC Motor Driver

TLE 4202

Bipolar IC

Features

- Max. output current 3.0 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection
- Short-circuit proof to ground
- Suitable for applications in automotive engineering



Type	Ordering Code	Package
S ■ TLE 4202	Q67000-A8007	P-T66-7-H

■ Not for new design

9

The TLE 4202 IC is a dual comparator that is particularly suitable as a driver for reversible DC motors and may also be used as a versatile power driver.

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for applications in motor vehicles. It can be applied at package temperatures between −40 °C and 130 °C.

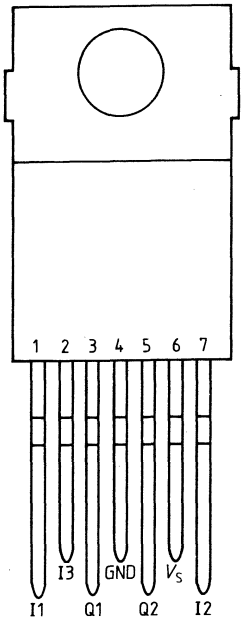
The comparators can be driven analogically in form of a window discriminator or simply by digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanism, etc.

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low residual voltages at the sink transistor, the drive circuit of the sink transistor is connected to the supply voltage. An SOA circuit protects the IC against ground short-circuits.

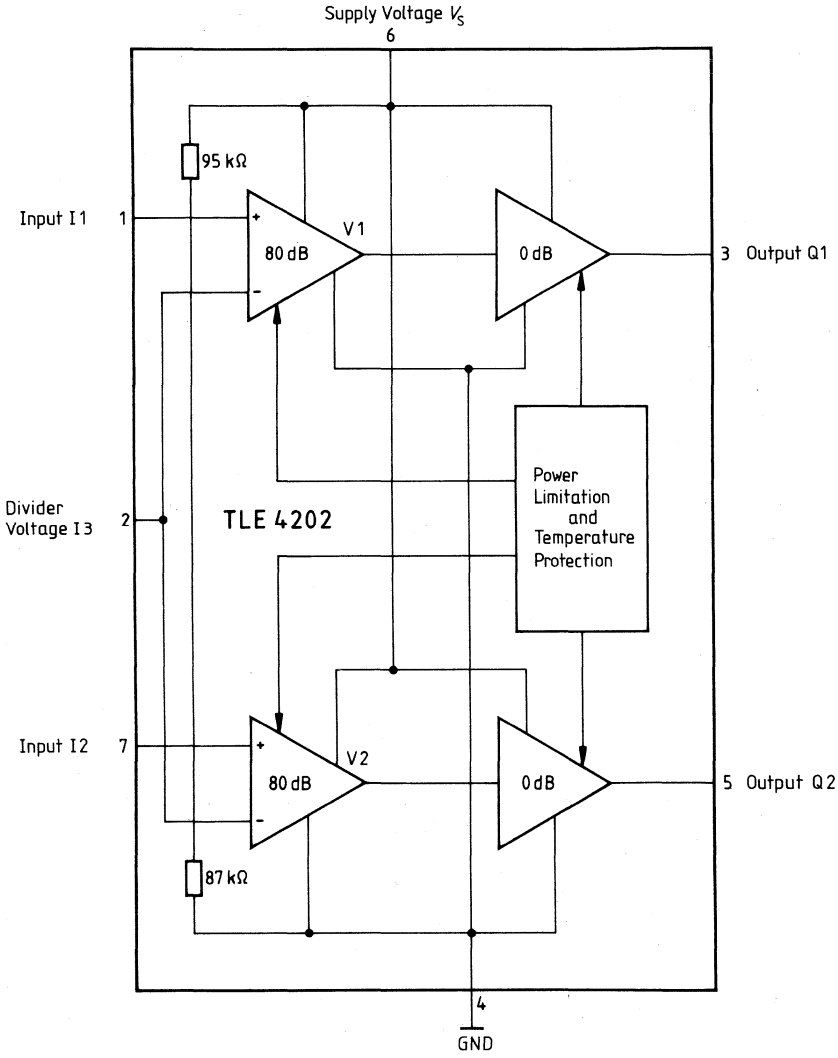
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	I1	**Input** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input** Inverting input of the two comparators, to be connected according to general rules
3	Q1	**Output Q1** Push-pull B output DC-short-circuit proof to ground
4	GND	**Ground**
5	Q2	**Output Q2** see pin 3
6	V_S	**Supply voltage** V_S Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	**Input** Non-inverting input I2, see pin 1

Block Diagram



Absolute Maximum Ratings

$T_C = -40\,°C$ to $130\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage Supply voltage ($t \leq 50$ ms)	V_S V_S		25 36	V V
Output current $T_C \leq 85\,°C$	I_Q	−3.0	3.0	A
Voltage at pins 1, 2, I3 Voltage at the pins Q1, Q2	$V_{1,2,7}$ $V_{3,5}$	−0.3 −0.7	V_S V_S +0.7	V V
Junction temperature Storage temperature	T_j T_{stg}	 −55	150 125	°C °C

Operating Range

Supply voltage	V_S	3.5	17	V
Package temperature during operation $R_L \geq 11\,\Omega$, $V_S = 7...16$ V $R_L \geq 18\,\Omega$, $V_S = 16$ V	T_C	 −40	 130	 °C °C
Voltage gain (at negative feedback with external connection)	G_V	30		dB
Thermal resistance system – case	$R_{th\,SC}$		4.8	K/W

Outputs Q1 and Q2 short-circuit proof to ground
R_L: Resistance between output 1 and output 2

Characteristics

$V_S = 13$ V, $T_C = 25\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions	Test Circuit
General Characteristics							
Quiescent current	I_q		15	25	mA	$S = 1$	1
Open-loop voltage gain	G_{VO}	50	80		dB	$f = 500$ Hz[1])	1
Input Characteristics							
Input current (pins I1, I2)	$I_{I\,1,7}$		1.5	3.0	µA	$V_{I\,1,12} = 0$	2
Input resistance	$R_{I\,1,7}$	1	5		MΩ	$f = 1$ kHz	1
Input offset voltage	V_{I0}	−20		20	mV		3

[1]) $-40\,°C \leq T_C \leq 110\,°C$
$7\,V \leq V_S \leq 16\,V$

Characteristics

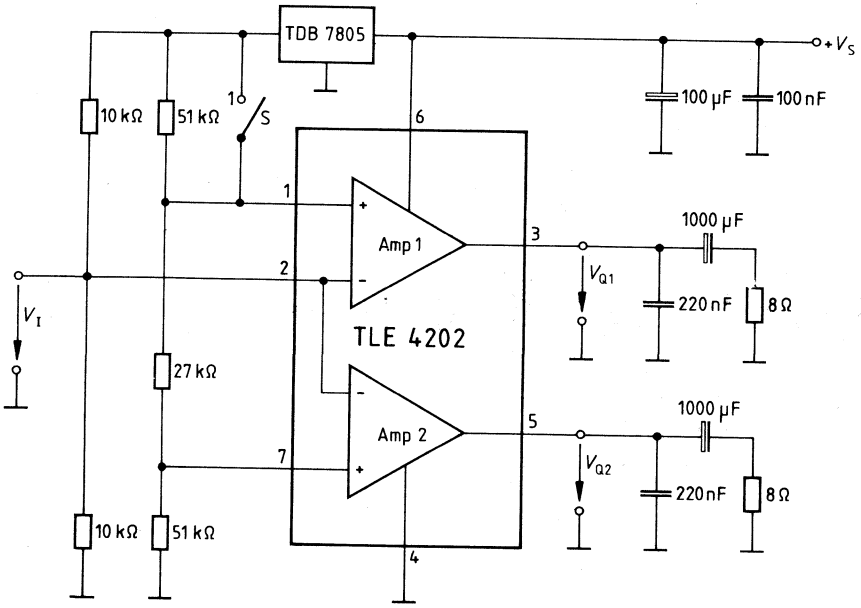
$V_S = 13$ V, $T_C = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
Output Characteristics							
Source operation	V_{Sato}		1.0	1.1	V	$I_Q = -0.3$ A S1 = 1	2
			1.2	1.6	V	$I_Q = -1.0$ A S1 = 1	2
			1.3	2.0	V	$I_Q = -1.5$ A S1 = 1[1]	2
Sink operation	V_{Satu}		0.35	0.5	V	$I_Q = +0.3$ A S1 = 2	2
			0.7	1.0	V	$I_Q = +1.0$ A S1 = 2	2
			0.8	1.5	V	$I_Q = +1.5$ A S1 = 2[1]	2
Short-circuit current	$I_{Q\,max}$		1.25	1.60	A	Source operation[1]	2
Slew-rate (falling edge)	SR	6			V/µs		1
Slew-rate (rising edge)	SR	6			V/µs		1
Switching Times							
Rise time of V_Q	t_r		1.5		µs		1
Falling time of V_Q	t_f		1.5		µs		1
Turn-on delay	t_{ON}		3.0		µs		1
Turn-off delay	t_{OFF}		1.5		µs		1

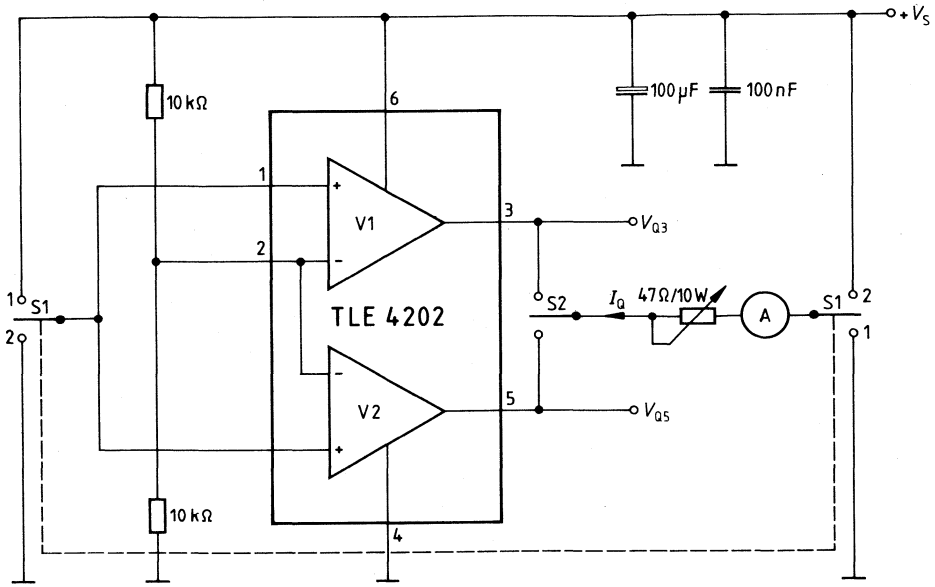
[1] $-40\,°C \le T_C \le 110\,°C$
$7\ V \le V_S \le 16\ V$

9

Test Circuit 1



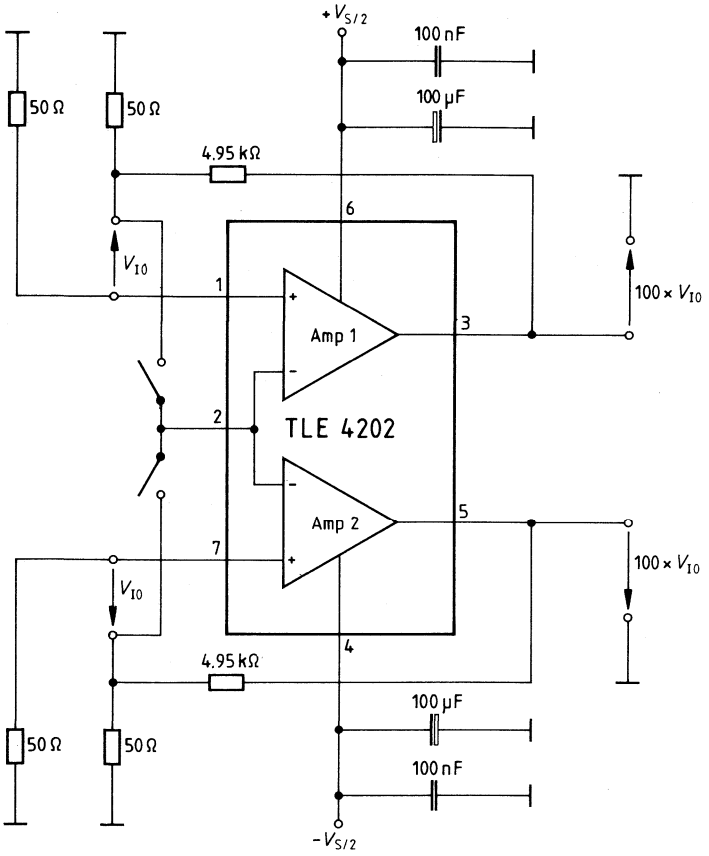
Test Circuit 2



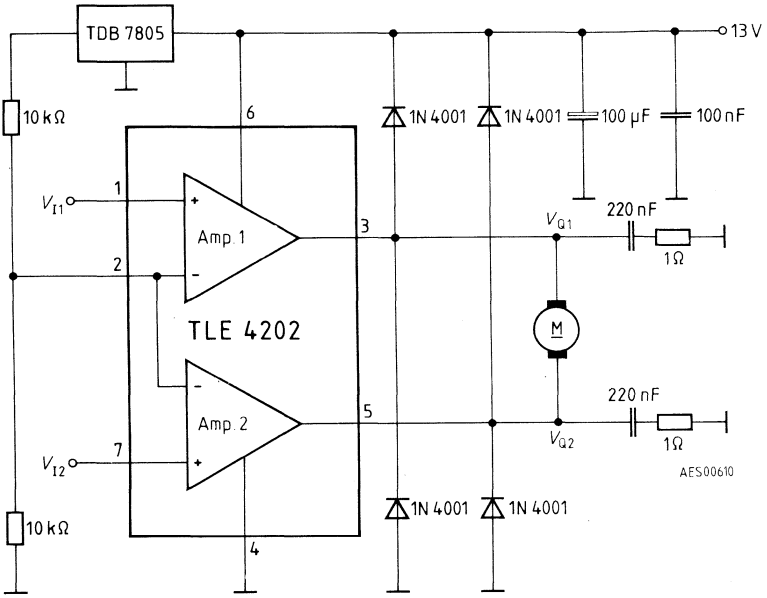
$V_{Sato} = V_S - V_{Q3/5}$
$V_{Satu} = V_{Q3/5}$
$I_{SC} = -I_Q$

9

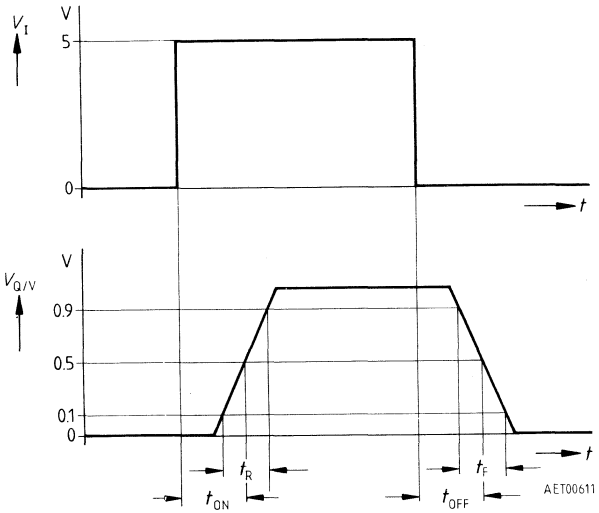
Test Circuit 3



Application Circuit



Diagram



SIEMENS

2 A DC Motor Driver

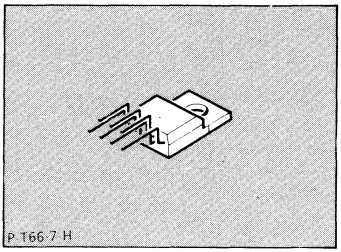
TLE 4202 B

Preliminary Data

Bipolar IC

Features

- Drives motors up to 2 A
- Integrated free-wheeling diodes 2.5 A
- Short-circuit proof to ground
- Overtemperature protection
- Low saturation voltages through bootstrap
- Wide temperature range
- Suitable for applications in automotive engineering



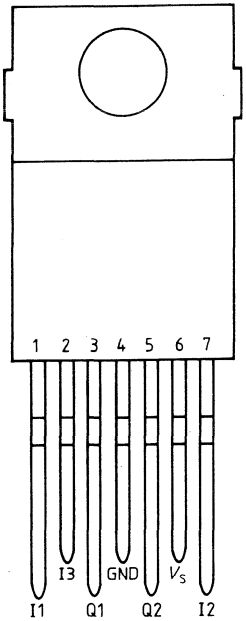
Type	Ordering Code	Package
S TLE 4202 B	Q67000-A8225	P-T66-7-H

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for application in motor vehicles. It can be applied at package temperatures between −40 °C and 130 °C.

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz.

The input stages are PNP differential amplifiers thus resulting in a common-mode input voltage range from 0 V to approx. the value of V_S and in a maximum input differential voltage of V_S. To obtain low saturation voltages at the sink circuit, the drive circuit of the sink transistor is connected to the supply voltage. An SOA protective circuit protects the IC against ground short-circuits. At chip temperatures above approx. 160 °C the source transistors are turned off.

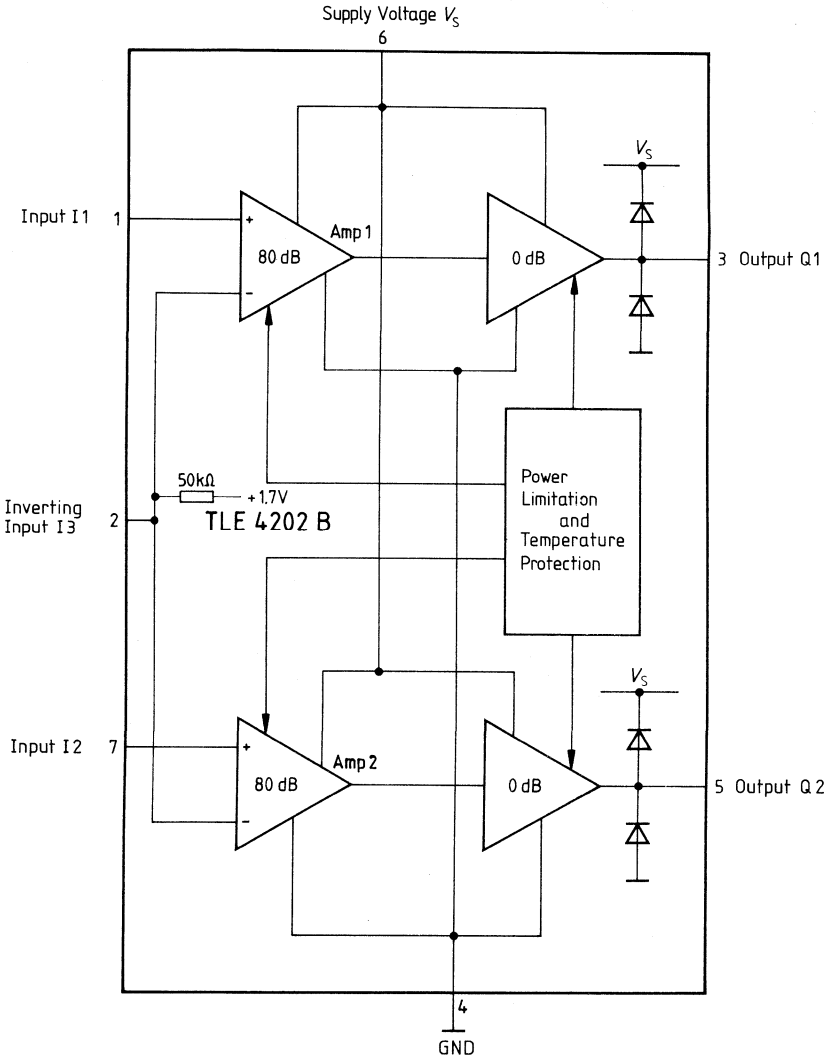
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	I1	**Input 1** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input 3** Inverting inputs of the two comparators; internally connected to reference voltage across 50 kΩ (typ. 1.7 V)
3	Q1	**Output Q1** Push-pull output B DC-short-circuit proof to ground. Integrated free-wheel diodes to ground and to supply voltage
4	GND	**Ground**
5	Q2	**Output Q2,** see pin 3
6	V_S	**Supply voltage** Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	**Input 2** Non-inverting input 2; see pin 1

Block Diagram



Absolute Maximum Ratings

$T_C = -40\,°C$ to $130\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S		40	V
Output current of sink transistors $T_C \leq 85\,°C$	I_Q		2.5	A
Output current of source transistors internally limited	I_Q			
Diode peak currents				
to $+V_S$	I_{F+}		2.5	A
to ground	I_{F-}		2.5	A
Voltage at pins I1, I2, I3	$V_{1,2,7}$	−0.3	V_S	V
Voltage at pins Q1, Q2[1])	$V_{3,5}$			V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C

Operating Range

Supply voltage	V_S	3.5	17	V
Package temperature during operation	T_C			
$R_L \geq 6\,\Omega$, $V_S = 7 \ldots 16$ V		−40		°C
$R_L \geq 9\,\Omega$, $V_S = 16$ V			130	°C
Voltage amplification (at negative feedback with external connection)	V_V	30		dB
Thermal resistance system – case	$R_{th\,SC}$		4	K/W

Outputs Q1 and Q2 short-circuit proof to ground
R_L: Resistance between output 1 and output 2

[1]) The output voltages are kept within a permissible range by free-wheel diodes

Characteristics

$V_S = 13$ V, $T_C = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
General Data							
Quiescent current	I_S		15	25	mA	$S = 1$	1
Open-loop gain	G_{VO}	50	80		dB	$f = 500$ Hz $V_S \leq 7$ V ≤ 16 V $T_C = -40$ °C to +110 °C	1
Input Characteristics							
Input current (pins I1, I2)	$I_{I\,1,\,7}$		1.0	3.0	µA	$V_{I\,1,\,12} = 0$	2
Input current	$I_{I\,2}$		35	70	µA	$V_{I\,2} = 0$; $V_{I\,1,\,7} = V_S$	1
	$-I_{I\,2}$		230	300	µA	$V_{I\,2} \leq V_S$; $V_{I\,1,\,7} = 0$ V	
Input resistance	$R_{I\,1,\,7}$	1	5		MΩ	$f = 1$ kHz	1
Input reference voltage	$V_{I\,2}$	1.4	1.7	2.0	V	$I_{I\,2} = 0$; $V_{I\,1,\,7} = 0$ V	1
Input offset voltage	V_{I0}	−20		20	mV		3
Output Characteristics							
Saturation voltages							
Source operation	V_{Sato}		0.9	1.0	V	$I_Q = -0.3$ A S1 = 1	2
measured to V_S	V_{Sato}		1.2	1.6	V	$I_Q = -1.0$ A S1 = 1	2
	V_{Sato}		1.5	2.1	V	$I_Q = -2$ A S1 = 1	2
Sink operation	V_{Satu}		0.25	0.4	V	$I_Q = +0.3$ A S1 = 2	2
			0.5	0.75	V	$I_Q = +1.0$ A S1 = 2	2
	V_{Satu}		1.0	1.3	V	$I_Q = +2$ A S1 = 2	2
Short-circuit current	I_{SC}		1.25	1.60	A	$V_Q = 0$ V	2
Diode forward voltage							
to $+V_S$	V_{F+}		1.0	1.3	V	$I_F = I_Q = +1$ A	2
to ground	V_{F-}		0.9	1.2	V	$I_F = I_Q = -1$ A	2
Slew rate falling edge	SR		6		V/µs		1
Slew rate rising edge	SR		6		V/µs		1
Switching Times							
Rise time of V_Q	t_r		1.5		µs		1
Fall time of V_Q	t_f		1.5		µs		1
Switch-on delay	t_{ON}		3.0		µs		1
Switch-off delay	t_{OFF}		1.5		µs		1

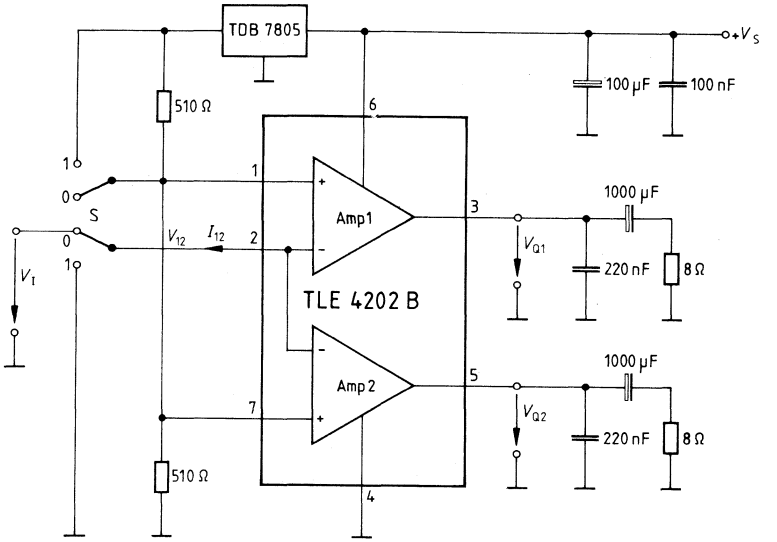
Characteristics

$V_S \leq 7$ V to ≤ 17 V; $T_C = -40$ °C to 110 °C

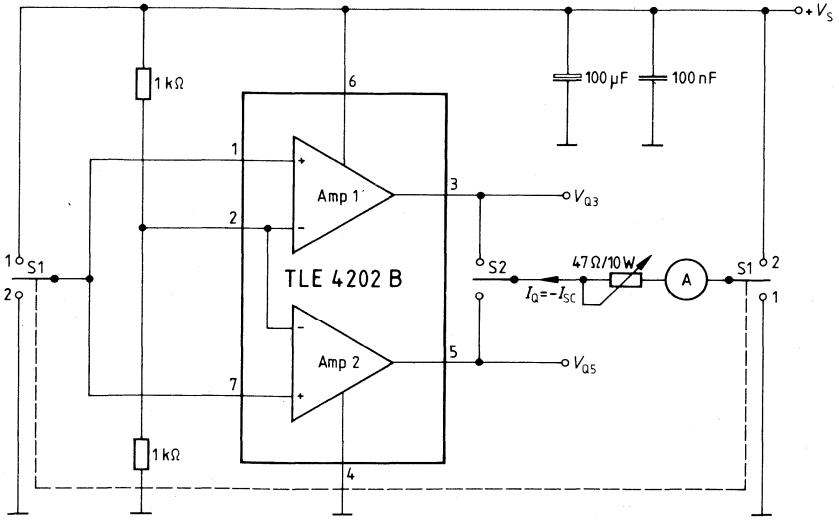
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
Quiescent current	I_S		15	30	mA	S = 1	1
Saturation Voltage							
Source operation measured to V_S	V_{Sato}		0.9	1.2	V	$I_Q = -0.3$ A; S = 1	2
	V_{Sato}		1.2	1.8	V	$I_Q = -1$ A; S = 1	2
	V_{Sato}		1.5	2.4	V	$I_Q = -2$ A; S = 1	2
Sink operation	V_{Satu}		0.25	0.60	V	$I_Q = 0.3$ A; S1 = 2	2
	V_{Satu}		0.5	1.1	V	$I_Q = 1$ A; S1 = 2	2
	V_{Satu}		1.2	2.0	V	$I_Q = 2$ A; S1 = 2	2
Short-circuit current	$-I_{SC}$			3.5	V	$V_Q = 0$ V $T_C = 25$ °C to 110 °C	

9

Test Circuit 1

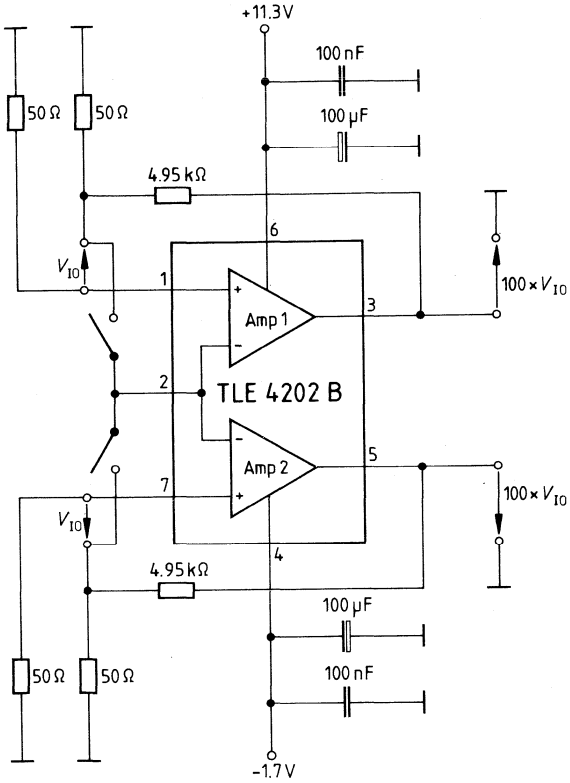


Test Circuit 2



$V_{Sato} = V_S - V_{Q3/5}$
$V_{Satu} = V_{Q3/5}$
$I_{SC} = -I_Q$

Test Circuit 3



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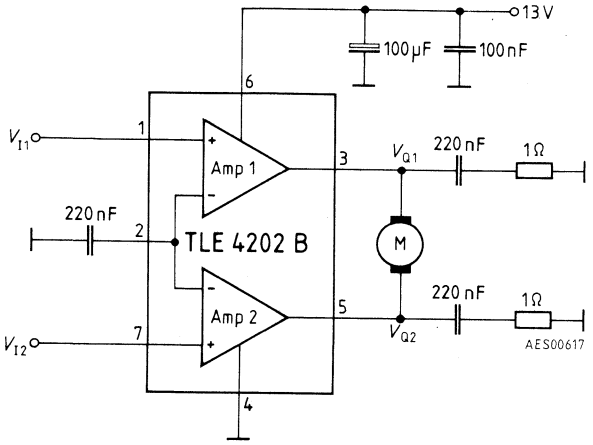
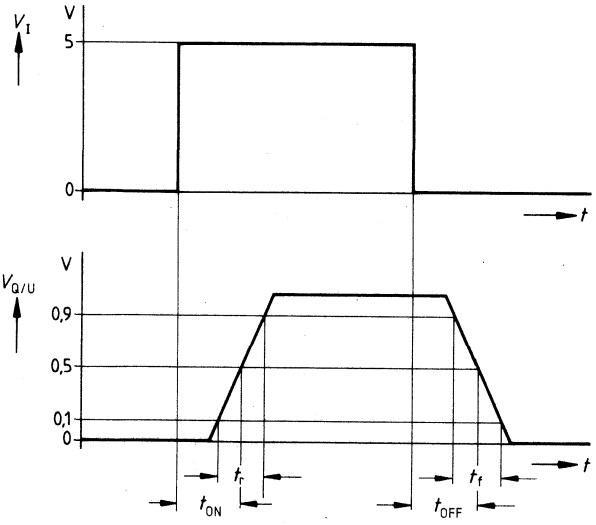
Application Circuit



Diagram



SIEMENS

4 A Motor Driver

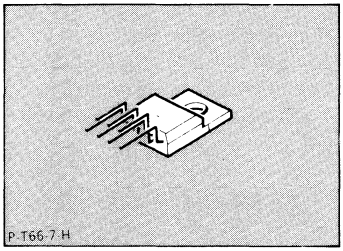
TLE 4203

Preliminary Data

Bipolar IC

Features

- Integrated free-wheeling diodes
- Outputs short-circuit proof to V_S and ground
- Thermal overload protection
- Blocking of the output stages upon undervoltage
- Final push-pull stage free of cross-over



Type	Ordering Code	Package
TLE 4203	Q67000-A8121	P-T66-7-H

The integrated circuit TLE 4203 is a versatile double power driver of up to 4 A output current which is particularly suitable as a driver for DC motors in reversible operation.

The push-pull power output stages operate in the switching mode and can be combined to a full-bridge configuration.

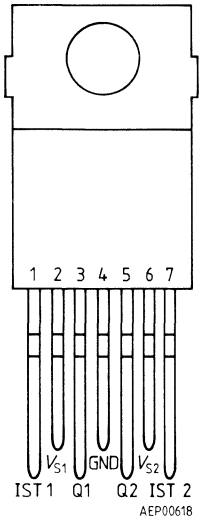
The drive of the input stage is implemented using digital logic.

The device contains a temperature protection logic, output stages protected against short-circuit and integrated free-wheeling diodes.

Typical applications are for follow-up control, servo drives, servo motors, drive mechanisms, etc.

9

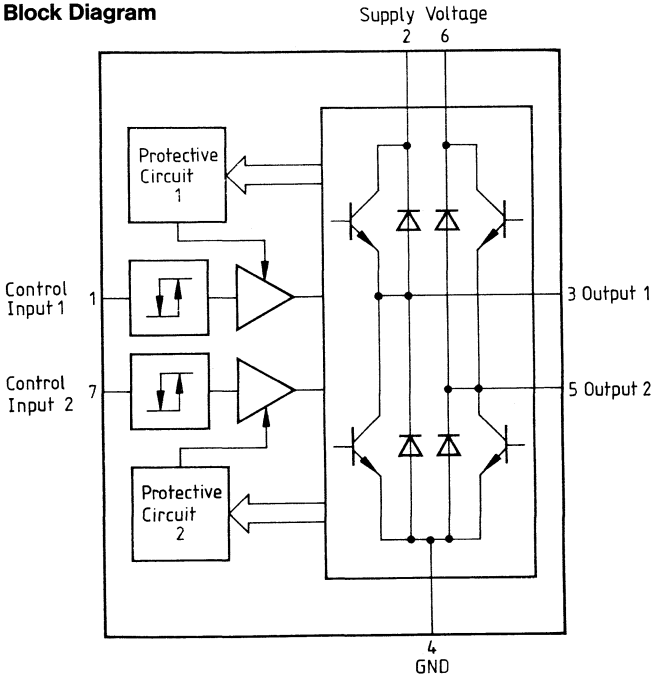
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	IST1	**Control input for channel 1** (TTL/CMOS-compatible), of non-inverting effect on the channel output.
2	V_{S1}	**Channel 1 supply voltage;** externally connected with the supply voltage pin for channel 2 (pin 6).
3	Q1	**Short-circuit protected push-pull C output** channel 1 for currents up to 6 A. Free-wheeling diodes are integrated on chip for inductive loads.
4	GND 1,2	**Ground;** track should be designed for the max. short-circuit current (2 x 6 A).
5	Q2	**Short-circuit protected push-pull C output** channel 2 for currents up to 6 A. Free-wheeling diodes are integrated on chip for inductive loads.
6	V_{S2}	**Channel 2 supply voltage;** externally connected with the supply voltage pin for channel 1 (pin 2).
7	IST2	**Control input for channel 2** (TTL/CMOS-compatible), of non-inverting effect on the channel output.

Block Diagram



Application

In industrial and automotive electronics, power full-bridge DC motor drivers are mostly used for bidirectional motor drives. The two TTL and CMOS-compatible control inputs act on the output as follows:

Status	Input 1	Input 2	Output 1	Output 2
1	L	L	V_{QL}	V_{QL}
2	L	H	V_{QL}	V_{QH}
3	H	L	V_{QH}	V_{QL}
4	H	H	V_{QH}	V_{QH}

V_{QL} means: Lower power unit conducting; upper power unit blocked.

V_{QH} means: Upper power unit conducting; lower power unit blocked.

The following examples illustrate the operation:

Status 1: Motor is slowed down
Status 2: Motor turns right
Status 3: Motor turns left
Status 4: Motor is slowed down

Circuit Description

Input Circuit

The control inputs consist of TTL and CMOS-compatible Schmitt triggers with hysteresis. Buffer amplifiers, controlled from these stages, convert the logic signal into the form required for driving the power output stages.

Output Stages

The output stages consist of two push-pull C stages. Using protective circuits for limiting the power dissipation makes the outputs short-circuit proof to ground and to supply voltage throughout the entire operating range. Positive and negative voltage peaks, which occur when switching inductive loads, are limited by integrated power diodes.

Monitoring and Protecting Functions

The IC is protected against thermal overloads by a temperature protecting circuit.

In addition an internal circuit ensures that all output transistors are blocked for supply voltages below the operating range.

A monitoring stage logic for each output stage transistor detects whether the relevant transistor is active and in this case for sink operation (source operation) prevents the corresponding source transistor (sink transistor) from being turned on. Direct cross-over currents are effectively prevented with this method.

Absolute Maximum Ratings

$T_C = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage	V_S	−0.3	45	V
Logic input voltages	$V_{I\,1,\,2}$	−45	45	V
Currents				
Supply current $T_C \leq +85\,°C$	I_S	−12	12	A
Output current $T_C \leq +85\,°C$	$I_{Q\,1,\,2}$	−6	6	A
Ground current $T_C \leq +85\,°C$	I_{GND}	−12	12	A
Temperatures				
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−50	150	°C
Thermal resistances				
system – case	$R_{th\,SC}$		3	K/W
system – ambient	$R_{th\,SA}$		65	K/W

Maximum Ratings

$T_C = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Operating Range				
Supply voltage	V_S	5.0	20	V
Logic input voltage	$V_{I\,1,\,2}$	−10	40	V
Case temperature $T_j \leq 150\,°C$	T_C	−40	125	°C

Characteristics

$V_S = 8 \ldots 18$ V; $T_C = -25 \ldots 125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
General Characteristics						
Quiescent current	I_q		70	100	mA	$V_{I1} = V_{I2} > V_{IH}$
Quiescent current	I_q		180	230	mA	$V_{I1} = V_{I2} < V_{IL}$
Logic						
Control inputs						
H input voltage	V_{IH}	2.8			V	
L input voltage	V_{IL}			1.2	V	
Hysteresis of input voltage	ΔV_I		0.7		V	
H input current	I_{IH}			10	µA	$V_I = 5$ V
L input current	$-I_{IL}$			10	µA	$V_I = 0.5$ V
Switching Stages						
Saturation voltages						
to $+V_S$	V_{QSato}		1.1	1.3	V	$V_{I1,2} > V_{IH}$; $I_Q = -1$ A[1])
to $+V_S$	V_{QSato}		1.5	1.8	V	$V_{I1,2} > V_{IH}$; $I_Q = -2$ A[1])
to $+V_S$	V_{QSato}		2.5	3.5	V	$V_{I1,2} > V_{IH}$; $I_Q = -4$ A[1])
to ground	V_{QSatu}		0.3	0.6	V	$V_{I1,2} < V_{IL}$; $I_Q = 1$ A
to ground	V_{QSatu}		0.6	1.0	V	$V_{I1,2} < V_{IL}$; $I_Q = 2$ A
to ground	V_{QSatu}		1.6	3.2	V	$V_{I1,2} < V_{IL}$; $I_Q = 4$ A

[1]) measured to $+V_S$

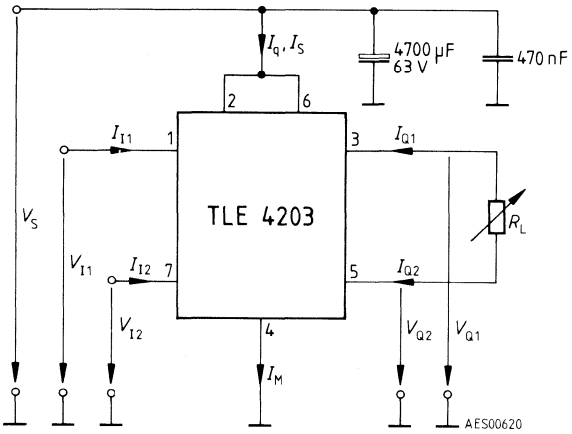
Characteristics

$V_S = 8...18$ V; $T_C = -25...125$ °C

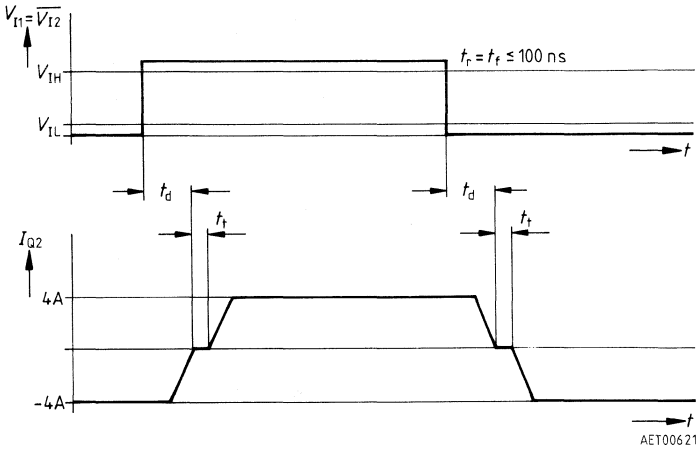
Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Forward Voltages						
Diode to $+V_S$	$-V_{QFo}$		0.95	1.3	V	$V_{I1/2} > V_{IH}$; $I_Q = 1$ A[1])
Diode to $+V_S$	$-V_{QFo}$		1.05	1.5	V	$V_{I1/2} > V_{IH}$; $I_Q = 2$ A[1])
Diode of $+V_S$	$-V_{QFo}$		1.30	1.8	V	$V_{I1/2} > V_{IH}$; $I_Q = 4$ A[1])
Diode to ground	$-V_{QFu}$		0.95	1.3	V	$V_{I1/2} < V_{IL}$; $I_Q = -1$ A
Diode to ground	$-V_{QFu}$		1.00	1.5	V	$V_{I1/2} < V_{IL}$; $I_Q = -2$ A
Diode to ground	$-V_{QFu}$		1.20	1.8	V	$V_{I1/2} < V_{IL}$; $I_Q = -4$ A

[1]) measured to $+V_S$

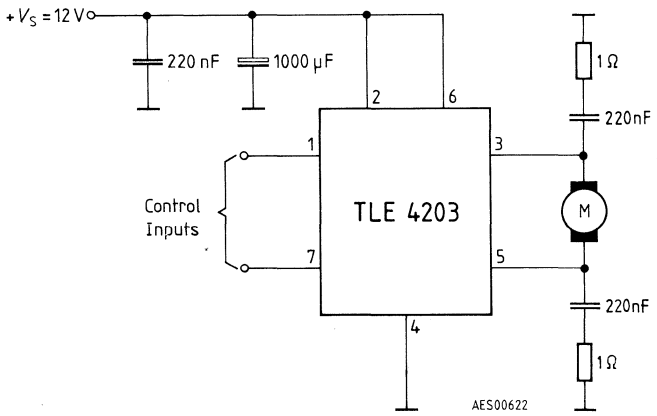
Test Circuit



Timing Diagram

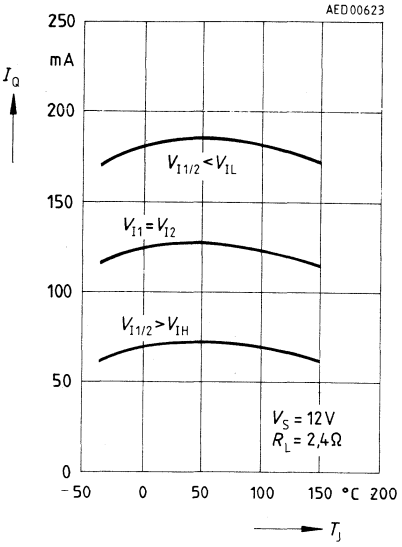


Application Circuit



9

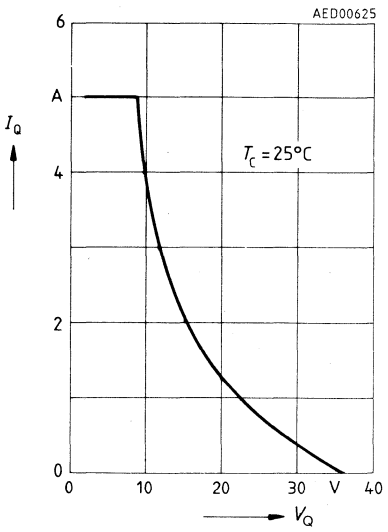
Qiescent Current versus Case Temperature



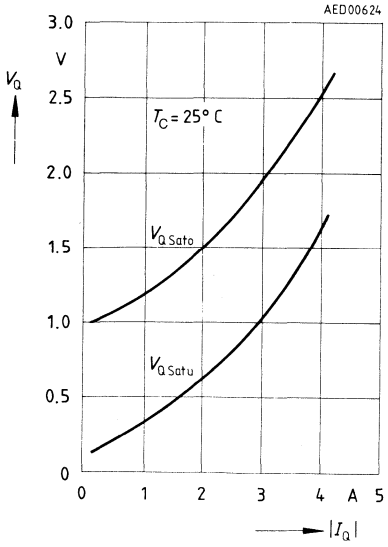
Short-Circuit Current versus Output Voltage

$V_A = V_Q$ for sink operation

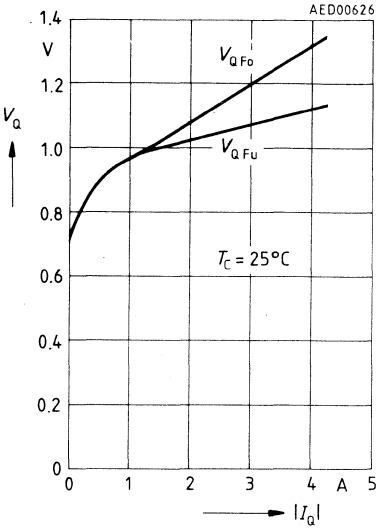
$V_A = V_S - V_Q$ for source operation



Saturation Voltage versus Output Current



Diode Forward Voltage versus Output Current



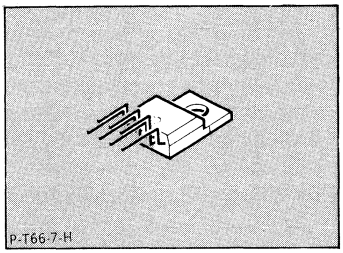
SIEMENS

3 A Motor Driver

TLE 4204

Preliminary Data

Bipolar IC



Features

- Max. output current 4 A
- Outputs short-circuit proof to $\pm V_S$
- Thermal overload protection
- Integrated free-wheeling diodes to $\pm V_S$
- Max. supply voltage 45 V
- Suitable for automotive applications

Type	Ordering Code	Package
S TLE 4204	Q67000–A8182	P-T66-7-H

Integrated 3 A full-bridge DC motor driver with temperature protection, fully protected output stages and integrated free-wheeling diodes. The case temperature range is −40 °C to 125 °C. The IC is also especially suitable for application in automotive electronics.

Application Description

In industrial and automotive electronics full-bridge DC motor drivers are mostly applied in bidirectional motor drives. Both of the differential control inputs act on the outputs as follows:

State	Differential input voltage 1	Differential input voltage 2	Output 1	Output 2
1	<0	<0	V_{QL}	V_{QL}
2	<0	>0	V_{QL}	V_{QH}
3	>0	<0	V_{QH}	V_{QL}
4	>0	>0	V_{QH}	V_{QH}

V_{QL} means: Lower power unit conducts; upper power unit is blocked
V_{QH} means: Upper power unit conducts; lower power unit is blocked

Examples:
State 1: Motor is slowed down
State 2: Motor turns right
State 3: Motor turns left
State 4: Motor is slowed down

9

Circuit Description

Input Circuit

The input stages are designed as differential inputs with an open-loop gain of typ. 80 dB and a common-mode input voltage range to 0 V.

Output Stages

The output stages consist of two push-pull C stages. Using the protective circuits for limiting the power dissipation makes the outputs short-circuit proof to ground and to supply voltage throughout the entire operating range. Positive and negative voltage peaks which occur during switching of inductive loads, are limited by integrated diodes.

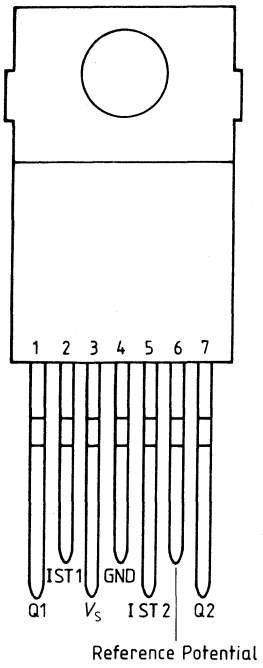
Monitoring and Protecting Functions

The IC is protected against thermal overload by a temperature protecting unit.

The power units are controlled by a protection circuit. At low voltages (up to 8 V) only the current is limited in order to protect the bond leads. At higher voltages the protection circuit controls the power dissipation in the power unit.

Pin Configuration

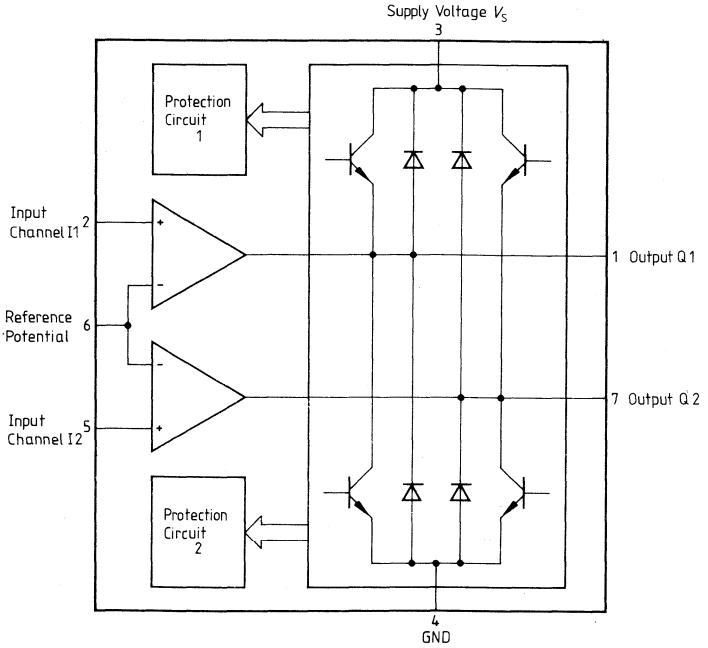
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	**Output of channel 1** Short-circuit proof push-pull C output channel 1 for rated currents up to 3 A. Free-wheeling diodes to $+V_S$ and to ground are integrated.
2	IST1	**Control input for channel 1** Differential input referred to pin 6; of non-inverting effect on output channel 1. The common-mode range is specified from V_S −2.5 V to ground.
3	V_S	**Supply voltage** Block against ground (pin 4) with a ceramic capacitor of 220 nF min. close to pin 3. For longer connections a low-inductance circuit-proof supporting electrolytic capacitor of at least 10 µF between pin 3 and 4 is to be supplied. The connection is to be designed for the maximum short-circuit current (2 x 4 A).
4	GND	**Ground** Design the connection for the maximum short-circuit current (2 x 4 A).
5	IST2	**Control input channel 2** Differential input referred to pin 6; of non-inverting effect on output 2. The common-mode range is specified from V_S −2.5 V to ground.
6	Reference potential	**Input reference potential for channel 1 and 2** The user can individually determine the switching threshold with this input. The common-mode range is specified from V_S −2.5 V to ground.
7	Q2	**Output of channel 2** Short-circuit proof push-pull C output channel 2 for rated currents up to 3 A. Free-wheeling diodes to $+V_S$ and to ground are integrated.

Block Diagram



Absolute Maximum Ratings

$T_C = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Voltages				
Supply voltage	V_S	−0.3	45	V
Input voltages Pin 2, 5 and 6	V_I	−0.3	$+V_S$	V
Currents				
Supply current $T_C \leq 85\,°C$	I_S	−3	8	A
Output current $T_C \leq 85\,°C$	$I_{Q\,1,2}$	−4	4	A
Ground current $T_C \leq 85\,°C$	I_{GND}	−8	8	A
Diode peak currents				
to $+V_S$	I_{F+}		1.5	A
to ground	I_{F-}		4	A

Absolute Maximum Ratings

$T_C = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Temperatures				
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−50	150	°C
Operating Range				
Supply voltage	V_S	8	24	V
Case temperature $T_j \leq 150\,°C$	T_C	−40	125	°C
Thermal resistance				
system – case	$R_{th\ SC}$		4	K/W
system – ambient	$R_{th\ SA}$		65	K/W

Characteristics

$T_C = 25\,°C$; $V_S = 12$ V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
General Ratings						
Quiescent current	I_1		15	30	mA	$V_{2,5} = 12$ V; $V_6 = 0$ V
Control Inputs						
Input offset voltage	V_{I0}	−10		10	mV	
Input offset current	I_{I0}	−100		100	nA	
Input current	$-I_{I\,2,5}$		1	2	µA	$V_{2,5} = 0$ V; $V_6 = 12$ V
Input current	$-I_{I\,6}$		2	4	µA	$V_{2,5} = 12$ V; $V_6 = 0$ V
Common-mode input voltage ranges						
to $+V_S$	V_{IC+}		2.5	3	V	Difference to $+V_S$
to ground	V_{IC-}		−0.5	0	V	to ground
Output Stages						
Saturation voltages						
to $+V_S$	V_{QSato}		1.0	1.3	V	$V_{I6} < V_{I2,5}$; $I_Q = -1$ A[1]
to $+V_S$	V_{QSato}		2.0	2.5	V	$V_{I6} < V_{I2,5}$; $I_Q = -3$ A[1]
to ground	V_{QSatu}		1.0	1.3	V	$V_{I6} > V_{I2,5}$; $I_Q = 1$ A
to ground	V_{QSatu}		2.0	2.5	V	$V_{I6} > V_{I2,5}$; $I_Q = 3$ A

[1]) measured to $+V_S$

Characteristics

$T_C = 25\,°C$; $V_S = 12$ V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Output stages (cont'd)						
Forward voltages						
to $+V_S$	V_{Fo}		1.2	1.4	V	$V_{I6} < V_{I2,5}$; $I_Q = 1$ A[1])
to ground	V_{Fu}		−1	−1.2	V	$V_{I6} > V_{I2,5}$; $I_Q = -1$ A
to ground	V_{Fu}		−1.4	−1.6	V	$V_{I6} > V_{I2,5}$; $I_Q = -3$ A
Short-circuit currents						
at short-circuit to $+V_S$						S 1P, 2P closed
						$V_6 > V_{12,5}$
	$I_{QP1,7}$		2.5	3.5	A	$V_S = 12$ V
	$I_{QP1,7}$		1.0			$V_S = 24$ V
at short-circuit						S 1M, 2M closed
to ground						$V_6 < V_{12,5}$
	$-I_{QM1,7}$		2.5	3.5	A	$V_S = 12$ V
	$-I_{QM1,7}$		1.5		A	$V_S = 24$ V
Switching Times						
Turn-on time	$t_{D\,ON}$		2	4	µs	**see figure 2**
Turn-off time	$t_{D\,OFF}$		3	6	µs	**see figure 2**

[1]) measured to $+V_S$

Figure 1
Test Circuit

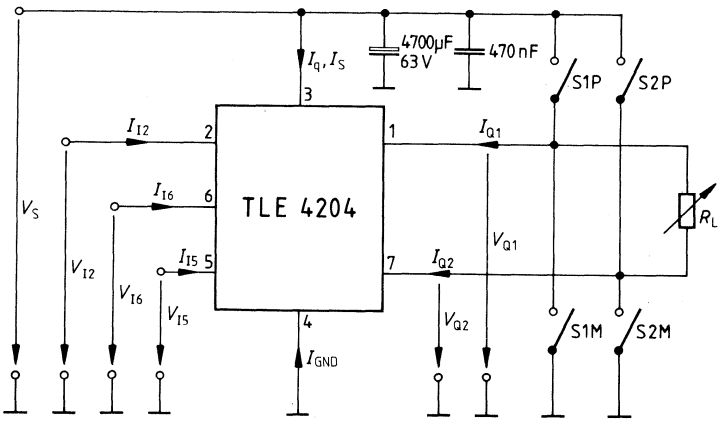


Figure 2
Timing Diagram

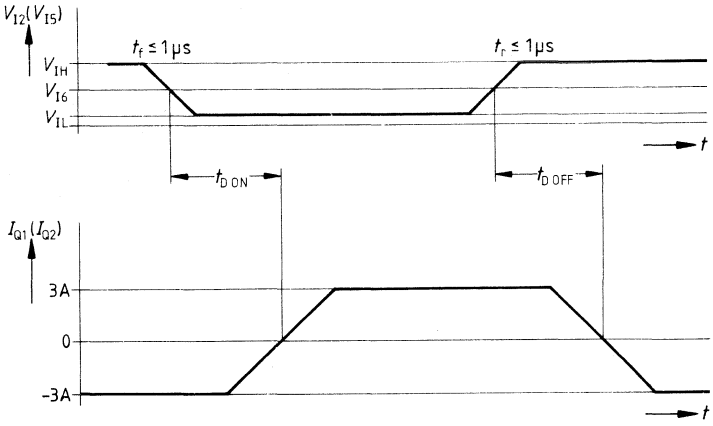
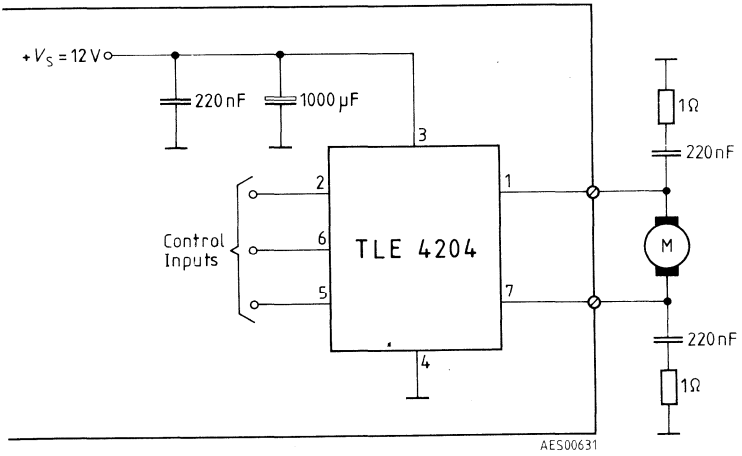
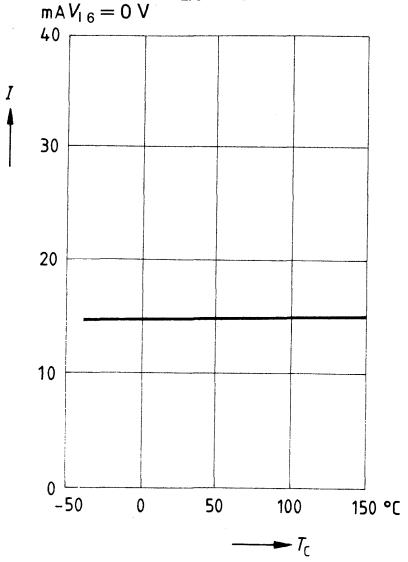


Figure 3
Application Circuit

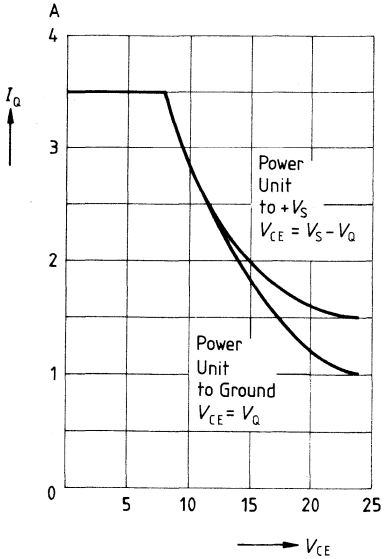


9

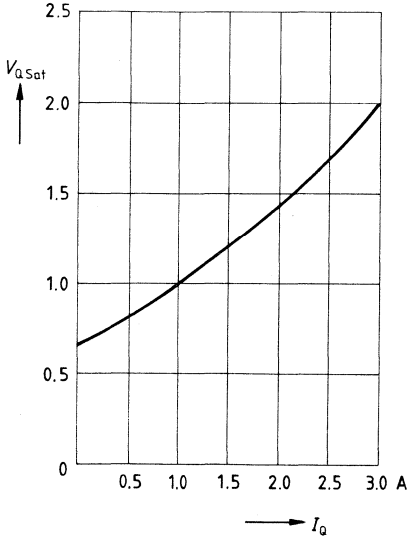
Quiescent Current versus Case Temperature T_C
$V_S = 12$ V; $V_{I\,2/5} = V_S$



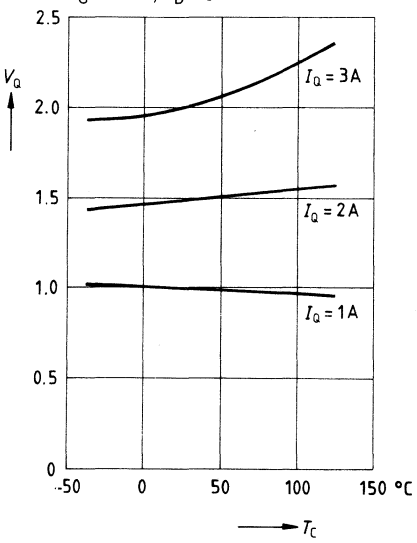
Short-Circuit Current versus Voltage V_{CE} of Power Unit
$T_C = 25$ °C



Saturation Voltage V_{QSat} versus Output Current I_Q
$V_S = 12$ V; $T_C = 25$ °C



Saturation Voltage versus Case Temperature T_C
$V_S = 12$ V; $P_D \leq 6$ W



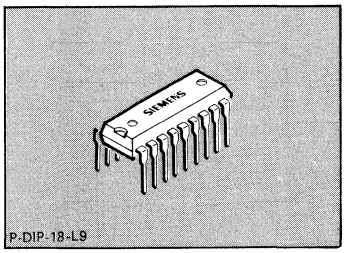
Motor Driver

TLE 4205

Bipolar IC

Features

- Max. driver current 1 A
- Integrated free-wheeling diodes
- Shortcircuit-proof to ground
- Inhibit
- ESD-protected inputs
- Temperature range $-40\,°C \leq T_j \leq 150\,°C$

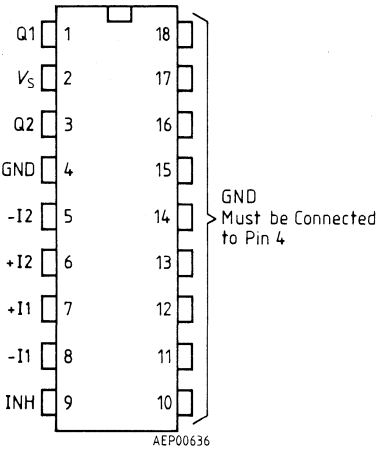


Type	Ordering Code	Package
▼ TLE 4205	Q67000-A9025	P-DIP-18-L9

▼ New type

TLE 4205 is an integrated power full-bridge DC motor driver for a wide temperature range, as required in automotive applications for example. The circuit contains two power comparators that can be combined to a full-bridge circuit. For inductive loads there are integrated free-wheeling diodes to $+V_S$ and ground. The outputs are shortcircuit-proof to ground and turn off when overtemperature occurs. This IC is especially suitable for headlight-beam adjustment in automobiles.

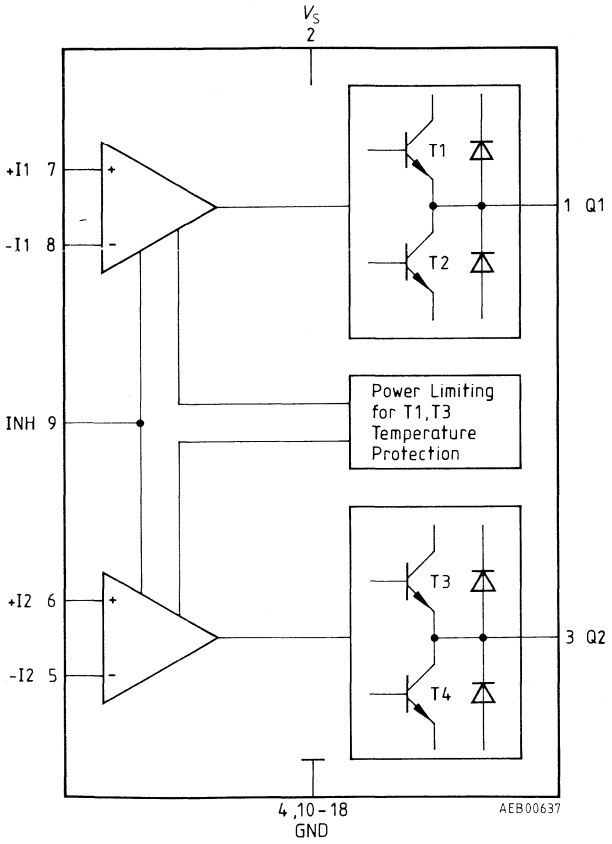
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	**Output Q1 of channel 1;** push-pull B output with DC short-circuit protection to ground. Integrated free-wheeling diodes to ground and the supply voltage.
2	V_S	**Supply voltage V_S;** must be blocked to ground with a ceramic capacitor of at least 100 nF directly on the pins of the IC.
3	Q2	**Output Q2 of channel 2;** see pin 1.
4	GND	**Ground**
5	–I2	**Inverting input channel 2;** to be wired according to general rules.
6	+I2	**Non-inverting input channel 2;** to be wired according to general rules.
7	+I1	**Non-inverting input channel 1;** see pin 6.
8	–I1	**Inverting input channel 1;** see pin 5.
9	INH	**Inhibit;** the IC is passive when this pin is open or connected to ground.
10-18	GND	**Ground;** must be connected to pin 4.

Block Diagram

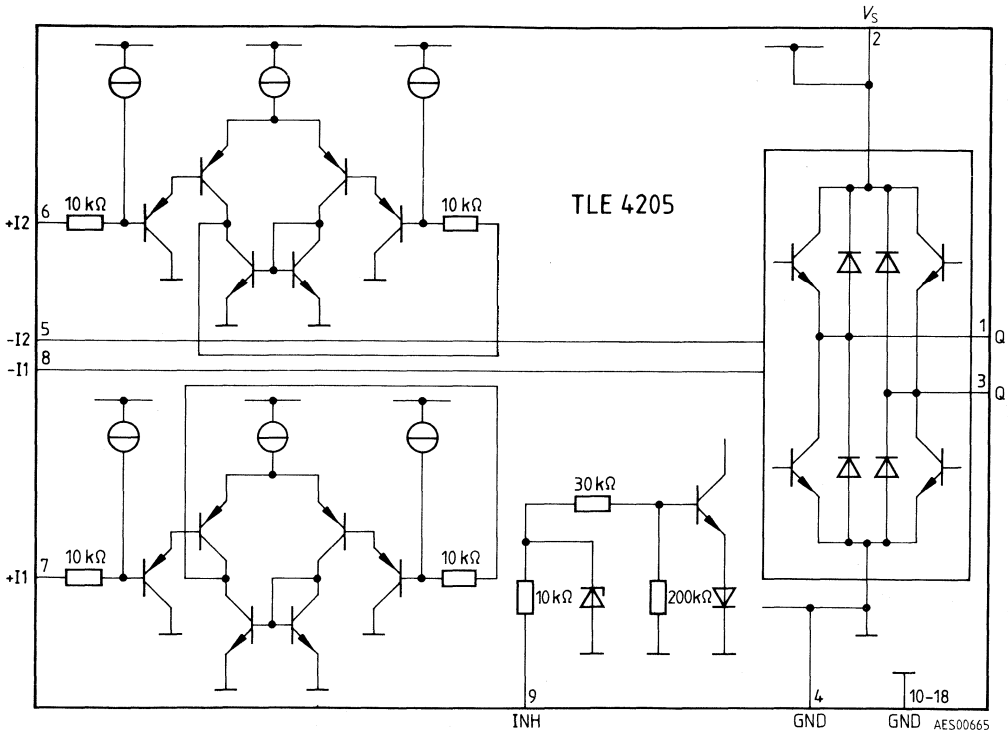


Circuit Description

The IC contains two amplifiers with typical open-loop gain of 80 dB at 500 Hz.

The input stages consist of PNP differential amplifiers. This produces a common-mode input range of 0 V to nearly V_S and a maximum differential input voltage of V_S. The IC is guarded against ground shorts by an SOA protective circuit. The output transistors are turned off if the chip temperature exceeds approx. 160 °C. The IC can be turned off by an inhibit input, which very much reduces current consumption.

Circuit Diagram



Absolute Maximum Ratings

Maximum ratings for junction temperature $T_j = -40$ to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	−0.3	45	V	
Differential input voltage	V_{ID}		$\pm V_S$	V	$\Delta V_{6\text{-}5}$ or $\Delta V_{7\text{-}8}$
Output current	I_Q	−1	1	A	
Supply current	I_S	2.5	3	A	
Ground current	I_{GND}	−3	2.5	A	I2
Input voltage	V_I	−15	$+V_S$	V	V_5; V_6; V_7; V_8
Inhibit input	V_9	−15	$+V_S$	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−50	150	°C	

Operating Range

Supply voltage	V_S	6	32	V	
Case temperature	T_C	−40	105	°C	$P_{Dmax} = 3$ W

Thermal Resistance

junction – ambient	R_{thjA}		70	K/W	
junction – case	R_{thjC}		15	K/W	

Outputs pin 1 and pin 3 shortcircuit-proof to GND at $V_S \leq 18$ V

9

Characteristics

$V_S = 13.5$ V; $T_j = 25$ °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
General						
Open-circuit current consumption	I_S		10	30	mA	active
Open-circuit current consumption	I_S		10	100	µA	inhibit
Turn-on dead time ref. to $V_{9\,Off/On}$	t_{dOn}		10	20	µs	$\mid I_{1,3} \mid < 1$ A
Turn-off dead time ref. to $V_{9\,Off/On}$	t_{dOff}		10	20	µs	$\mid I_{1,3} \mid < 1$ A
Open-loop gain	G_{VO}	50	80		dB	$f = 500$ Hz
Inputs						
Input zero voltage	V_{IO}	−7.5		7.5	mV	$R_S = 10$ kΩ; $-40\,°C \le T_j \le 85\,°C$
Input-voltage drift	$\Delta V_{IO}/\Delta T$		20	30	µV/K	$-40\,°C \le T_j \le 85\,°C$
Input zero current	I_{IO}	−75		75	mA	$-40\,°C \le T_j \le 85\,°C$
Input current	I_I	−300		300	nA	$-40\,°C \le T_j \le 85\,°C$
Input-current drift	$\Delta I_I/\Delta T$			5	nA/K	$-40\,°C \le T_j \le 85\,°C$
Input common-mode range, positive	V_{IC}			$V_S - 2$	V	
Input common-mode range, negative	V_{IC}			−0.5	V	
Power-supply rejection ratio	*PSRR*			200	µV/V	$R_S = 10$ kΩ; $-40\,°C \le T_j \le 85\,°C$
Common-mode rejection ratio	*CMRR*	70	80		dB	

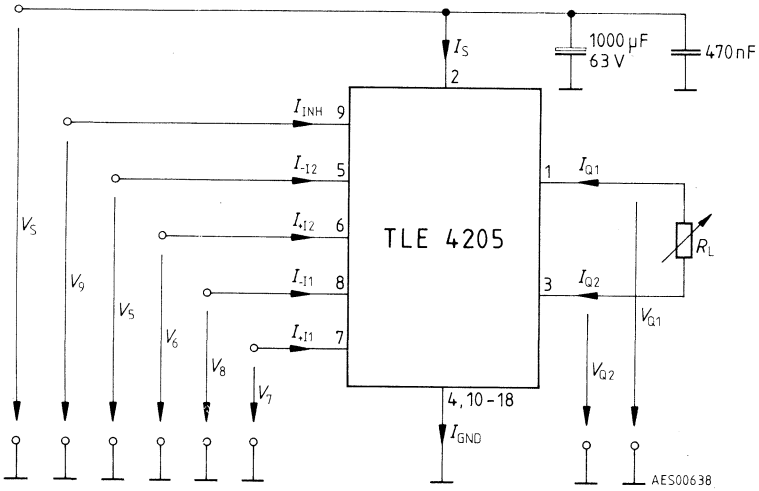
Characteristics

$V_S = 13.5$ V; $T_j = 25$ °C

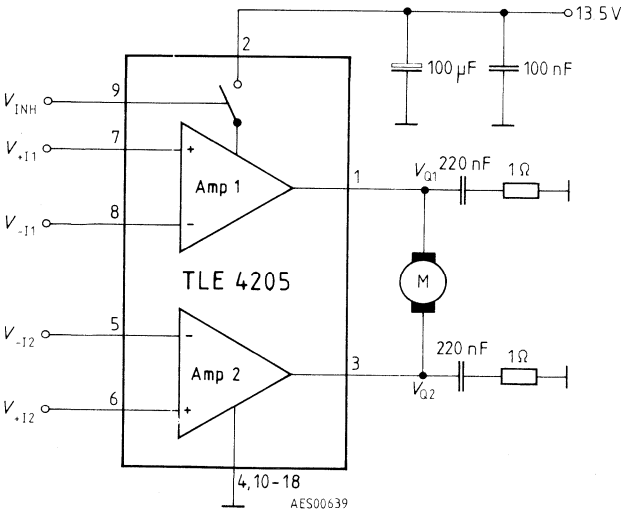
Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Outputs						
Saturation voltage	V_{Satu}		1.0	1.5	V	$I_Q = 0.6$ A; $-40\,°C \le T_j \le 85\,°C$
Saturation voltage	V_{Sat1}		1.0	1.5	V	$I_Q = 0.6$ A; $-40\,°C \le T_j \le 85\,°C$
Forward voltage of free-wheeling diode	V_{Fu}		1.0	1.5	V	$I_Q = 0.6$ A; $-40\,°C \le T_j \le 85\,°C$
Forward voltage of free-wheeling diode	V_{F1}		1.0	1.5	V	$I_Q = 0.6$ A; $-40\,°C \le T_j \le 85\,°C$
Slew rate of	$V_Q\ dV_q/dt_r$		2.0		V/µs	
Inhibit Input						
Switching threshold high	V_{IH}	2			V	
Switching threshold high	V_{IL}			0.8	V	
H-input current	I_{IH}		100		µA	$V_9 = 5$ V
L-input current	I_{IL}		0		µA	$V_9 = 0$ V

9

Test Circuit



Application Circuit



SIEMENS

Stepper Motor Drivers

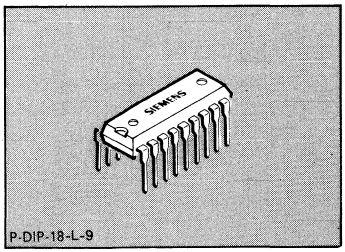
TCA 1561 B
TCA 1560

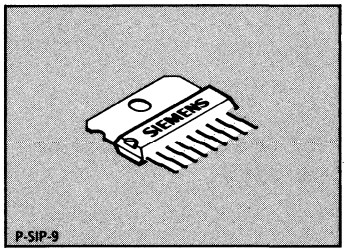
Advance Information: TCA 1560 G

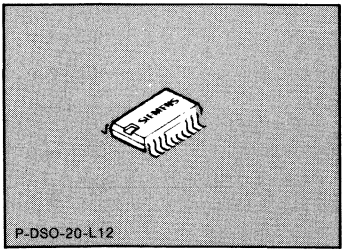
Bipolar IC

Features

- 2.5 A peak current
- High-speed integrated clamp diodes
- Simple drive
- Thermal overload protection with hysteresis







Type	Ordering Code	Package
S TCA 1561 B	Q67000-A8209	P-SIP-9
S TCA 1560 B	Q67000-A8208	P-DIP-18-L9
S ▼ TCA 1560 G	Q67000-A8272	P-DSO-20-L12 (SMD)

▼ New type

The TCA 1561 B is a bipolar monolithic IC designed to control the motor current in one phase of a bipolar stepper motor. It can also be used to drive direct-current motors as well as all inductive loads operated by constant current.

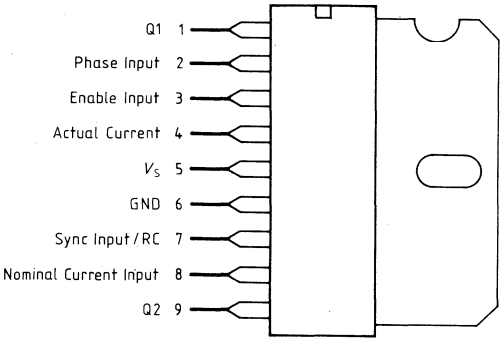
The IC has TTL-compatible logic inputs and contains a full-bridge driver with integrated, high-speed free-wheeling diodes and chopper-operated dynamic motor current limiting. The nominal current is infinitely variable with a control voltage. Using a minimum of external components and a single supply voltage, two TCA 1561 B ICs form a complete and directly MC-drivable system for two-phase bipolar stepper motors with output currents up to 2.5 A per phase.

The functionally identical TCA 1560 B in P-DIP-18-L9 package is designed for output currents up to 1.25 A.

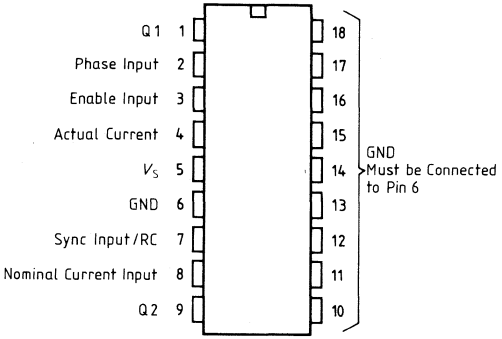
9

Pin Configurations
(top view)

TCA 1561 B



TCA 1560 B



Pin Definitions and Functions

TCA 1561 B

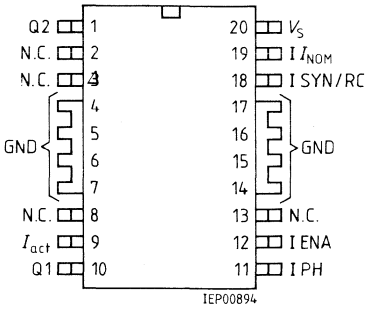
Pin	Symbol	Function
1	Q1	Output Q1
2 3		Phase input Enable input
4		Actual current
5	V_S	Supply voltage
6	GND	Ground
7 8	RC	Sync input/RC Nominal current input
9	Q2	Output Q2

The cooling fin is connected internally to pin 6 (ground).

TCA 1560 B

Pin	Symbol	Function
1	Q1	Output Q1
2 3		Phase input Enable input
4		Actual current
5	V_S	Supply voltage
6	GND	Ground
7 8	RC	Sync input/RC Nominal current input
9	Q2	Output Q2
10-18	GND	Ground (must be connected to pin 6)

Pin Configuration
P-DSO-20-L-12

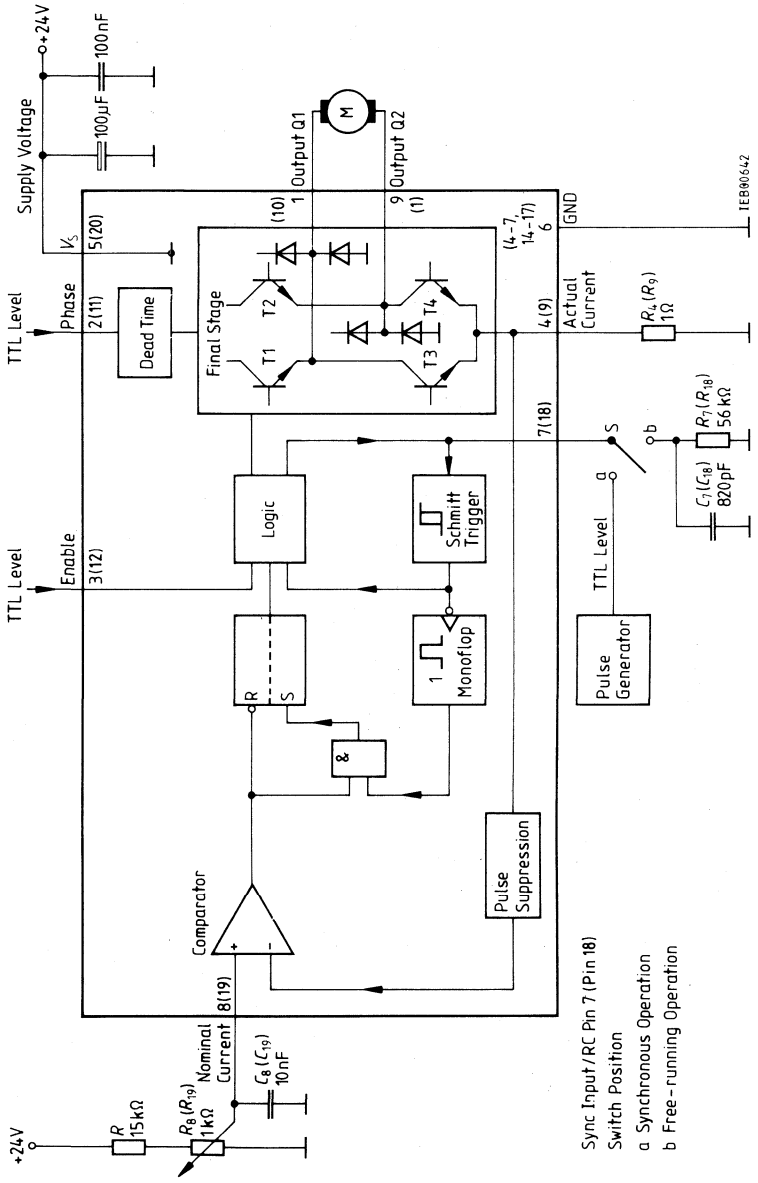


Pin Definitions and Functions

Pin	Symbol	Function
1	Q2	Output
2, 3	N.C.	Not connected
4-7	GND	Ground
8	N.C.	Not connected
9	I_{act}	Actual Current
10	Q1	Output
11	I PH	Phase Input
12	I ENA	Enable Input
13	N.C.	Not connected
14-17	GND	Ground
18	I SYN/RC	Synchron. Input/RC
19	I I_{NOM}	Nominal Current Input
20	V_S	Supply Voltage

Block Diagram

Notes in brackets refer to TCA 1560 G!



Circuit Description

Notes in brackets refer to TCA 1560 G.

Outputs

Outputs Q1, Q2 at pins 1, 9 (pins 1, 10) are fed by push-pull output stages. The two integrated free-wheeling diodes, referred to ground or supply voltage respectively, protect the IC against flyback voltages from an inductive load.

Enable

Outputs Q1 and Q2 are turned off when voltage $V_{I3} \leq 0.8$ V is applied to pin 3 (pin 12). The supply current then decreases maximally to 1 mA. The same occurs if pin 3 is not connected. The sink transistors are turned on when $V_{I3} \geq 2$ V.

Phase

The voltage at pin 2 (pin 11) determines the phase position of the output current. Output Q1 acts as sink for $V_{I2} \leq 0.8$ V and as source for $V_{I2} \geq 2$ V.

Similarly output Q2 acts as

sink when $V_{I2} \geq 2$ V and
source when $V_{I2} \leq 0.8$ V

The sink transistors are current-chopped. An internal circuit avoids undesired cross-over currents at phase change.

Nominal Current Input

The peak current in the motor winding is determined by the voltage at pin 8 (pin 19). A comparator compares this with the voltage drop at the actual current sensor at pin 4. If the nominal current is exceeded, the output sink transistors are turned off by a logic circuit.

Sync Input/RC

Outputs are turned on by a signal at pin 7 (pin 18). Two operating modes are possible: synchronizing by a fed-in TTL signal or free-running with the external RC combination.

Free-Running Operation

When the supply voltage is applied, capacitor C_7 at pin 7 (pin 18) charges to a limiting voltage, typically 2.4 V. With increasing current in the motor winding, the voltage rises at the actual current sensor R_4 at pin 4 (pin 9). After exceeding the predetermined value at the nominal current input (pin 8) the comparator, in conjunction with pulse suppression, resets an RS flipflop. The logic turns off sink transistors T3 and T4. C_7 ceases charging and the parallel resistance R_7 the discharges C_7. The sink transistors remain turned off until the lower threshold voltage of the Schmitt trigger is reached. This off period is thus controlled by the time constant $t_s = R_7 \times C_7$. After the lower trigger threshold has been passed, the monoflop is triggered by the falling edge of the Schmitt trigger output and, provided the voltage at the actual current sensor at pin 4 (pin 9) is lower than the nominal value at pin 8 (pin 19), the RS flipflop is reset. The logic circuit then turns on the sink transistors T3 or T4 and recharges capacitor C_7. If the voltage at pin 4 (pin 9) rises above the comparator value at pin 8 (pin 19), the sink transistors T3 and T4 are turned off again. Turn-on cannot be repeated until capacitor C_7 has discharged to the lower trigger threshold, the discharge time being a function of R_7 and C_7.

Synchronous Operation

Notes in brackets refer to TCA 1560 G

If a TTL level sync signal is fed to pin 7 (pin 18), the negative edge sets the RS flipflop, via the Schmitt trigger/monoflop combination, provided that the voltage at pin 4 (pin 9) is below the nominal value at pin 8 (pin 19). As in the free-running operation mode, the relevant output transistors become conductive. Similarly they are cut off by resetting the RS flipflop once the voltage at pin 4 (pin 9) is higher than the nominal value at pin 8 (pin 19).

Pulse Suppression

In all cases the pulse suppression circuit eliminates positive pulses, typically of 0.5 µs duration, at pin 4 (pin 9). These can result from cross-over currents in chopper operation through the integrated free-wheeling diodes. As a result, the voltage at pin 4 (pin 9) rises well above the nominal value, and without pulse suppression this would lead to dynamic current limiting. The duration of these basically unavoidable cross-over currents is of the same order of magnitude as the reverse-recovery time of the free-wheeling diodes.

Temperature Safeguard

If the temperature of the IC rises to approx. 150 °C, the final stages are turned off. At approx. 130 °C they are turned on again.

Logic Table

Enable		L	L	H	H
Phase		L	H	L	H
Output	Q1	/	/	L	H
Output	Q2	/	/	H	L
Transistor	T1	X	X	X	·
Transistor	T2	X	X	·	X
Transistor	T3	X	X	··	X
Transistor	T4	X	X	X	··

at:
$V_4 > 10$ mV ($V_9 > 10$ mV)*
$R_4 > 0\,\Omega$ ($R_9 > 0\,\Omega$)*

L = Low voltage level, input open
H = High voltage level
X = Transistor turned off
· = Transistor conducting
·· = Transistor conducting with current limiting turned on
/ = Output high-impedance

Absolute Maximum Ratings

$T_C = -40\,°C$ to $85\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage, pin 5	V_S	−0.3	45	V
Supply current, pin 5	I_S	0	2.5	A
Peak current in output transistors, pin 1, 9	I_Q	−2.5	2.5	A
Diode Currents				
Diode to $+V_S$	I_{FH}		2.5	A
Diode to ground	I_{FL}		2.5	A
Input voltage, pins 2, 3, 7, 8	V_I	−0.3	6	V
Output current, pin 4	I_4	−2.5		A
Voltage, pin 4	V_4	−0.3	5	V
Ground current, pin 6	I_6		2.5	A
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance				
system – ambient	$R_{th\,SA}$		70	K/W
system – case	$R_{th\,SC}$		8	K/W
Operating Range				
Supply voltage, pin 5	V_S	8	40	V
Case temperature	T_C	−40	85	°C
Input voltage, pins 2, 3, 7	V_I		5	V
Output current	I_Q	−2	2	A

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Characteristics

$V_S = 24$ V; $T_C = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply current, pin 5	I_S		18	30	mA	$V_{I3} = V_{IH}$
Supply current, pin 5	I_S		0.5	1	mA	$V_{I3} = V_{IL}$
Output, Pins 1, 9						
Output voltage: source	V_{QH}		1.7	1.9	V	$\mid I_Q \mid = 1$ A
Output voltage: source	V_{QH}		1.9	2.1	V	$\mid I_Q \mid = 1.5$ A
Output voltage: sink	V_{QL}		1.2	1.4	V	$\mid I_Q \mid = 1$ A
Output voltage: sink	V_{QL}		1.5	1.7	V	$\mid I_Q \mid = 1.5$ A
Reverse current	$\mid I_{QS} \mid$			300	µA	
Phase dead time	t_T	0.1	0.3	1.0	µs	**figure 1**
Forward voltage of diodes to $+V_S$	V_{FH}		1.0	1.2	V	$I_{FH} = 1$ A
	V_{FH}		1.1	1.3	V	$I_{FH} = 1.5$ A
Forward voltage of diodes to ground	V_{FL}		1.1	1.3	V	$I_{FL} = 1$ A
	V_{FL}		1.3	1.5	V	$I_{FL} = 1.5$ A
Inputs: Enable, Pin 3 and Phase, Pin 2						
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IL}			0.8	V	
H-input current	I_{IH}		50	100	µA	$V_{IH} = 5$ V
L-input current	$-I_{IL}$			100	µA	$V_{IL} = 0$ V
Rise and fall time	t_r, t_f			2	µs	
Nominal Current, Pin 8						
Control range	V_{I8}	0		2	V	
Input current	$-I_{I8}$			5	µA	$V_{I8} = 0$ V
Input offset voltage	$V_{I\,(8\text{-}4)}$		0		mV	**figure 3**
Actual Current, Pin 4						
Control range	V_{I4}	0		2	V	**figure 3**
Turn-off delay	t_D		2	3	µs	**figure 4**
Sync Input/RC, Pin 7						
Sync frequency	f	1		100	kHz	Duty cycle: 0.5
Duty cycle	D	0.1		0.9		$f = 40$ kHz
Rise and fall time	t_r, t_f			2	µs	
Output current, pin 7	$-I_{Q7}$	1.2	1.6	2.0	mA	
Trigger threshold, pin 7	V_{L7}		0.6	0.8	V	**figure 2**
Charging limit C_7	V_{G7}	2.2	2.4		V	
Off period	t_{OFF}		64		µs	**figure 5**
Dynamic input resistance pin 7	R_{I7}		1		kΩ	$V_7 = 1.5$ V

Absolute Maximum Ratings

$T_C = -25$ to 85 °C

Notes in brackets refer to TCA 1560 G

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage, pin 5 (pin 20)*	V_S	−0.3	45	V
Supply current, pin 5 (pin 20)	I_S	0	1.25 (1.0)	A
Peak current in output transistors, pins 1, 9 (pins 1, 10)	I_Q	−1.25 (−1.0)	1.25 (1.0)	A

Diode Currents, Pins 1, 9 (pins 1, 10)

Diode against $+V_S$	I_{FH}		1.25 (1.0)	A
Diode against ground	I_{FL}		1.25 (1.0)	A
Input voltage, pins 2, 3, 7, 8 (pins 11, 12, 18, 19)	V_I	−0.3	6	V
Output current, pin 4 (pin 9)	I_4 (I_9)	−1.25 (−1.0)		A
Voltage, pin 4 (pin 9)	V_4 (V_9)	−0.3	5	V
Ground current, pin 6 (pin 4 to 7)	I_6 ($I_{4\text{-}7}$)		1.25 (1.0)	A
Ground current (pin 14 to 17)	($I_{14\text{-}17}$)		(1.0)	A
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance junction – ambient	$R_{th\ jA}$		70	K/W
junction – case (measured at pin 14) (pin 4 to 7)	$R_{th\ jC}$		15	K/W

Operating Range

Supply voltage, pin 5	V_S	8	40	V
Package temperature measured at pin 14 (pin 4 to 7)	T_C	−25 (−40)	85 (120)	°C
Input voltage, pins 2, 3, 7 (pins 11, 12, 18)	V_I		5	V
Output current, pins 1, 9 (pins 1, 10)	I_Q	−1 (−0.5)	1 (0.5)	A

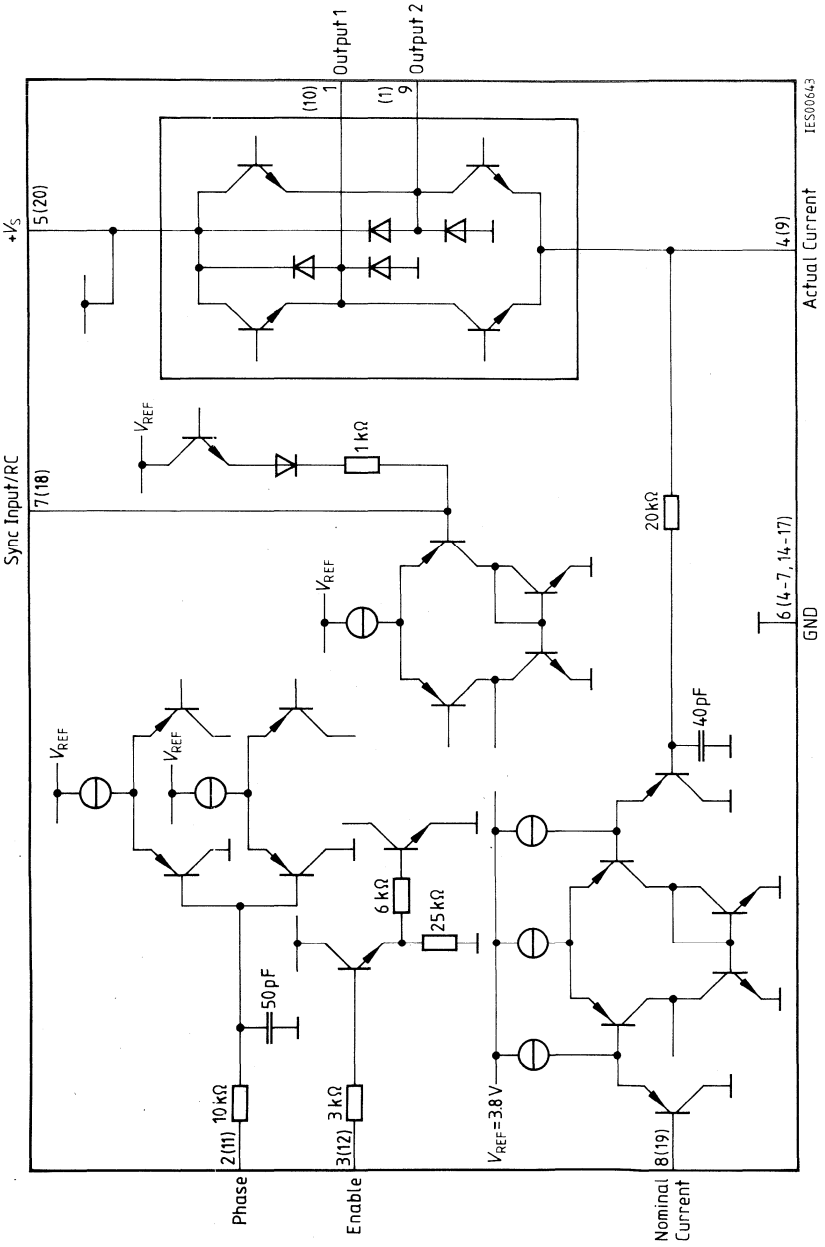
Characteristics

$V_S = 24$ V; $T_C = 25$ °C

Notes in brackets refer to TCA 1560 G.

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply current, pin 5 (pin 20)	I_S		18	30	mA	$V_{I3} = V_{IH}$
Supply current, pin 5 (pin 20)	I_S		0.5	1	mA	$V_{I3} = V_{IL}$
Output, Pins 1, 9 (pins 1, 10)						
Output voltage: source	V_{QH}		1.6	1.8	V	$\lvert I_Q \rvert = 0.5$ A
Output voltage: source	V_{QH}		1.65	1.90	V	$\lvert I_Q \rvert = 0.75$ A
Output voltage: sink	V_{QL}		1.0	1.2	V	$\lvert I_Q \rvert = 0.5$ A
Output voltage: sink	V_{QL}		1.1	1.4	V	$\lvert I_Q \rvert = 0.75$ A
Reverse current	$\lvert I_{QS} \rvert$			300	µA	
Phase dead time	t_T	0.1	0.3	1.0	µs	**figure 1**
Forward voltage of diodes to $+V_S$	V_{FH}		0.9	1.1	V	$I_{FH} = 0.5$ A
	V_{FH}		0.95	1.15	V	$I_{FH} = 0.75$ A
Forward voltage of diodes to ground	V_{FL}		0.95	1.15	V	$I_{FL} = 0.5$ A
	V_{FL}		1.0	1.2	V	$I_{FL} = 0.75$ A
Inputs: Enable, Pin 3 (pin 12) and Phase, Pin 2 (pin 11)						
H-input voltage	V_{IH}	2			V	
L-input voltage	V_{IL}			0.8	V	
H-input current	I_{IH}		50	100	µA	$V_{IH} = 5$ V
L-input current	$-I_{IL}$			100	µA	$V_{IL} = 0$ V
Rise and fall time	t_r, t_f			2	µs	
Nominal Current, Pin 8 (pin 19)						
Control range	V_{I8} (V_{I9})	0		2	V	
Input current	$-I_{I8}$ ($-I_{I9}$)			5	µA	$V_{I8} = 0$ V
Input offset voltage	$V_{I\,(8\text{-}4)}$		0		mV	**figure 3**
Actual Current, Pin 4 (pin 9)						
Regulating range	V_{I4} (V_{I9})	0		2	V	**figure 3**
Turn-off delay	t_D		2	3	µs	**figure 4**
Sync Input/RC, Pin 7 (pin 18)						
Sync frequency	f	1		100	kHz	Duty cycle: 0.5
Duty cycle	D	0.1		0.9		$f = 40$ kHz
Rise and fall time	t_r, t_f			2	µs	
Output current, pin 7 (pin 18)	$-I_{Q7}$ ($-I_{Q18}$)	1.2	1.6	2.0	mA	
Trigger threshold, pin 7 (pin 18)	V_{L7} (V_{L18})		0.6	0.8	V	**figure 2**
Charging limit C_7 (C_{18})	V_{G7} (V_{G18})	2.2	2.4		V	
Off period	t_{OFF}		64		µs	**figure 5**
Dynamic input resistance pin 7 (pin 18)	R_{I7} (R_{I18})		1		kΩ	$V_7 = 1.5$ V $V_{18} = 1.5$ V

Internal Wiring of Pins



9

Figure 1
Phase Dead Time

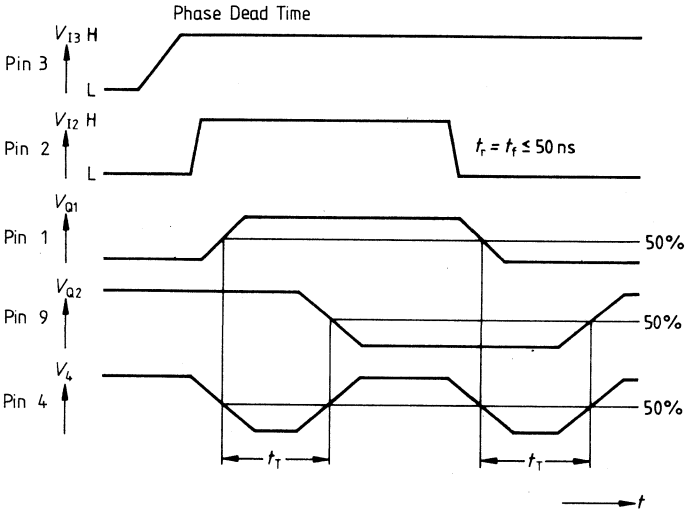


Figure 2
Trigger Threshold

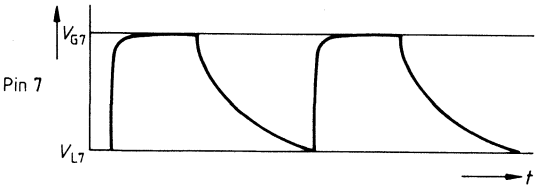


Figure 3
Control Range, Input Offset Voltage

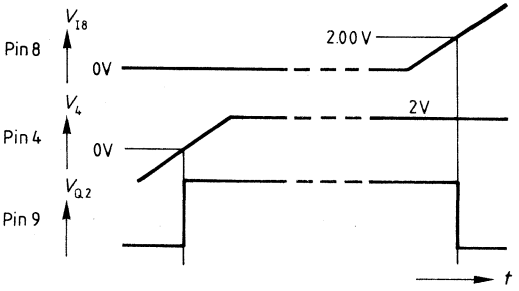


Figure 4
Turn-OFF Delay

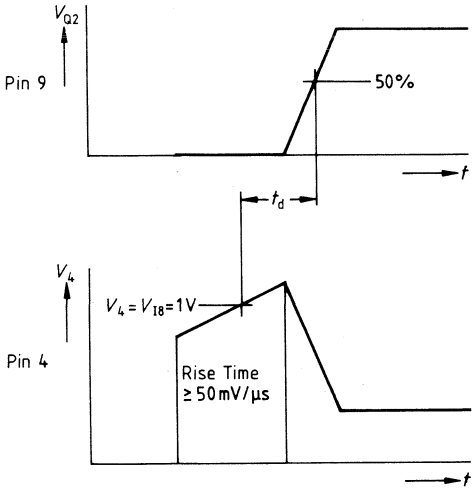
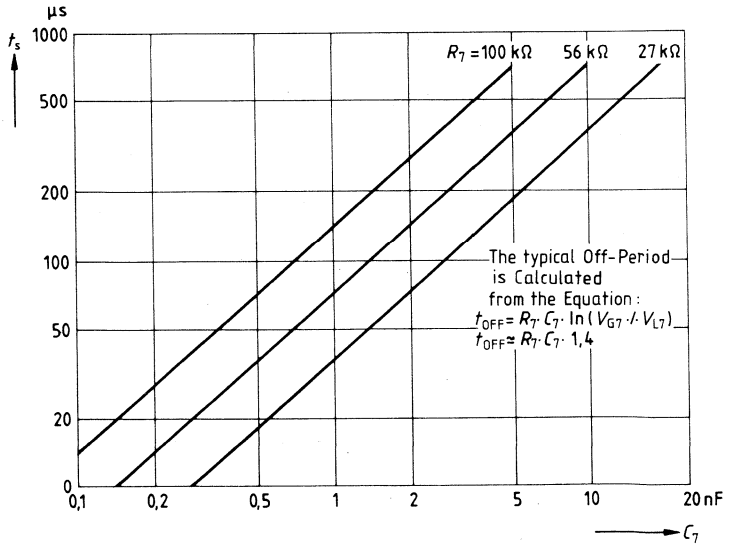


Figure 5
OFF Period versus Capacitance



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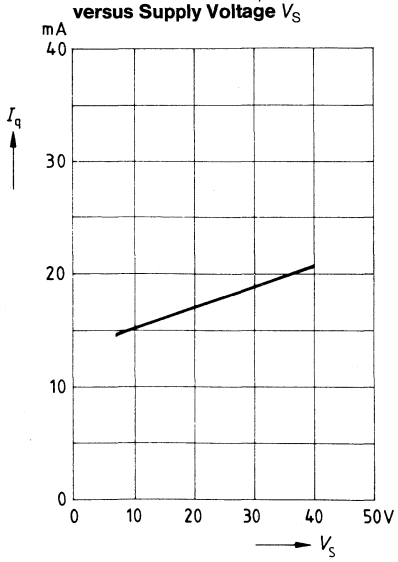
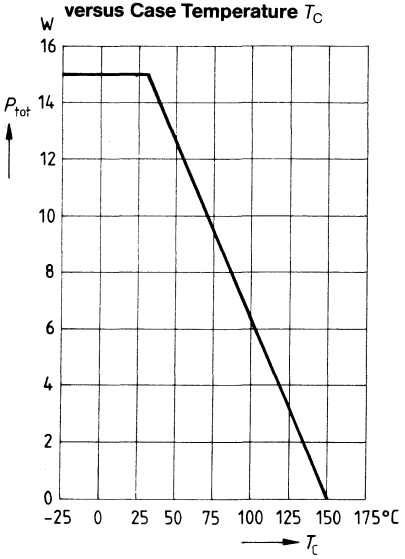
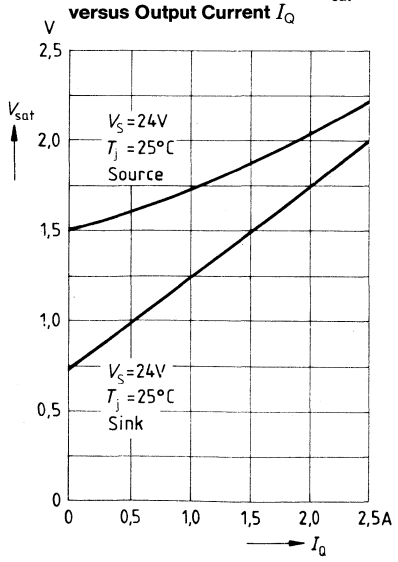
Quiescent Current I_q versus Supply Voltage V_S



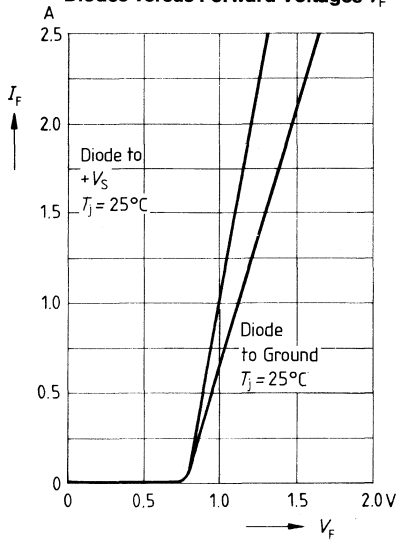
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



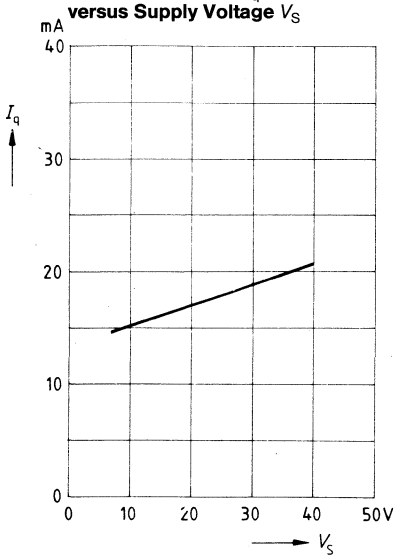
Output Saturation Voltages V_{sat} versus Output Current I_Q



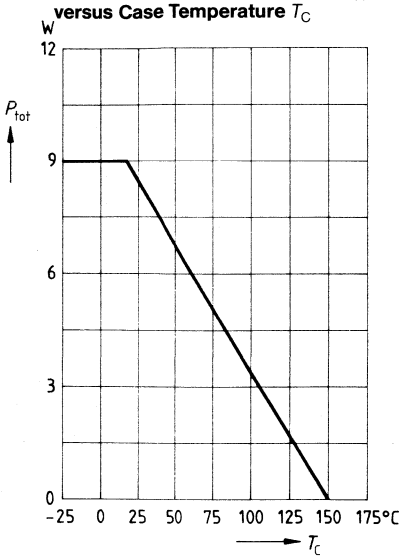
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



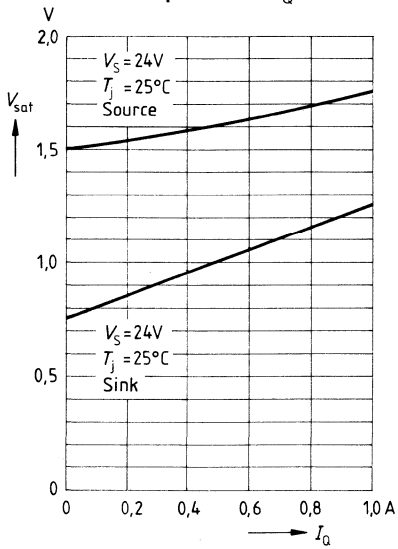
Quiescent Current I_q versus Supply Voltage V_S



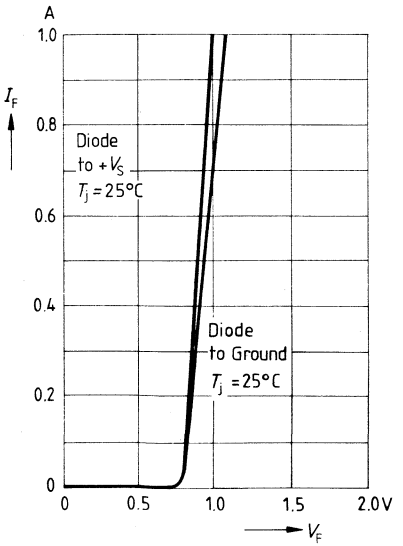
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



Output Saturation Voltages V_{sat} versus Output current I_Q

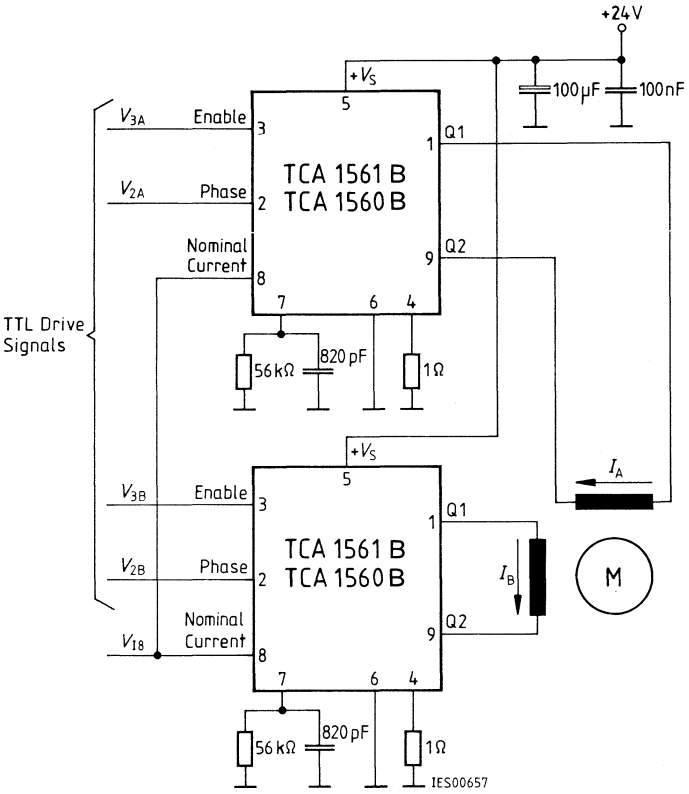


Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F

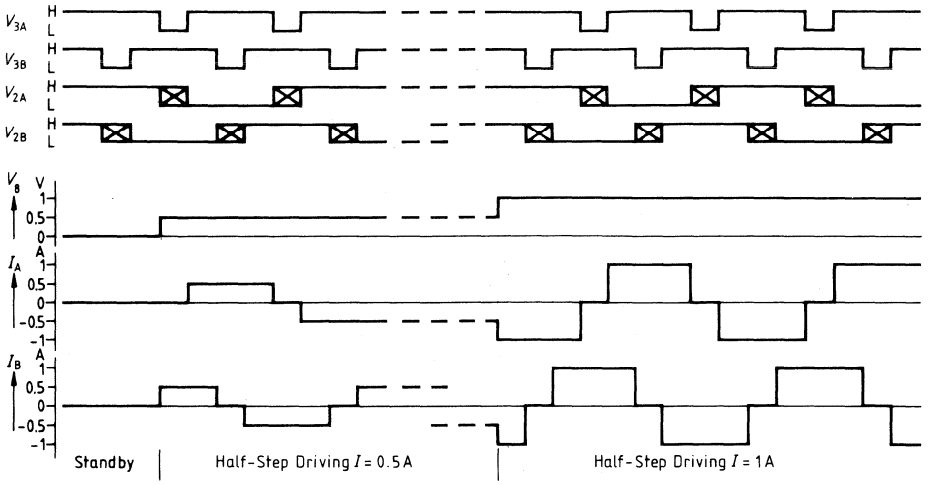


9

Application Circuit



Pulse Diagram for Application Circuit



Calculation of Power Dissipation

The total power dissipation P_{tot} comprises

Saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages)
Quiescent current losses P_q	(quiescent current multiplied by supply voltage)
Switching losses P_s	(turn-on/turn-off operation)

9

The following equations give the power dissipation for chopper operation without phase reversal. This can be regarded as "worst case", as, in addition to the switching losses, full-load current flows for the entire time.

$$P_{tot} = P_{sat} + P_q + P_s$$

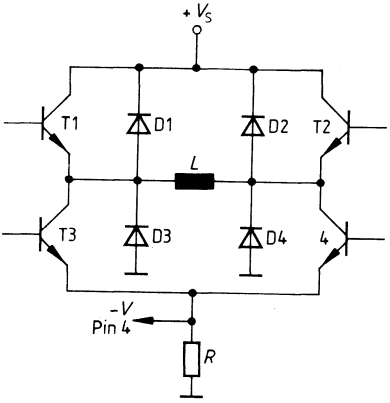
with

$$P_{sat} \simeq I_R \{V_{satu} \cdot D + V_{Fo}(1 - D) + V_{sato}\}$$

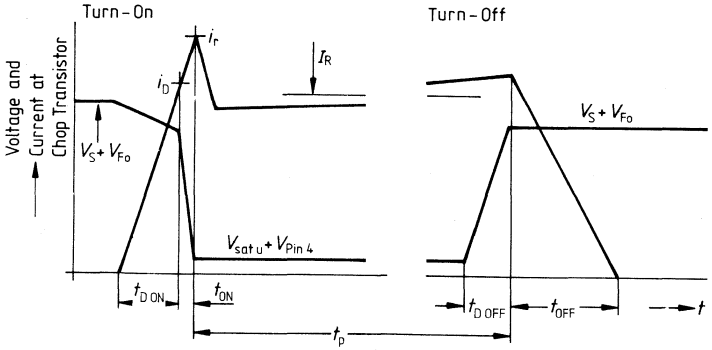
$$P_q = I_q \cdot V_S$$

$$P_s \simeq \frac{V_S}{T} \left\{ \frac{i_D \cdot t_{D\,ON}}{2} + \frac{(i_D + i_r)\, t_{ON}}{4} + \frac{I_R}{2} \left(t_{D\,OFF} + t_{OFF} \right) \right\}$$

I_R = Rated current (mean value)
I_q = Quiescent current
i_D = Reverse current during turn-on delay time
i_r = Peak reverse current
t_p = Conducting time of chop transistor
t_{ON} = Turn-on time
t_{OFF} = Turn-off time
$t_{D\,ON}$ = Turn-on delay time
$t_{D\,OFF}$ = Turn-off delay time
T = Cycle duration
D = Duty cycle t_p/T
V_{satu} = Saturation voltage of sink transistor (T3, 4)
V_{sato} = Saturation voltage of source transistor (T1, 2)
V_{Fo} = Forward voltage of clamp diode (D1, 2)
V_S = Supply voltage

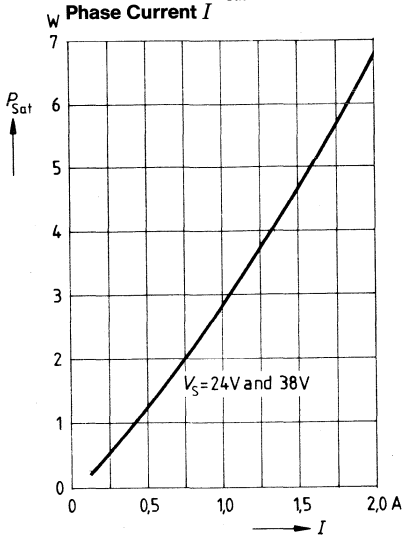


Calculation of Power Dissipation

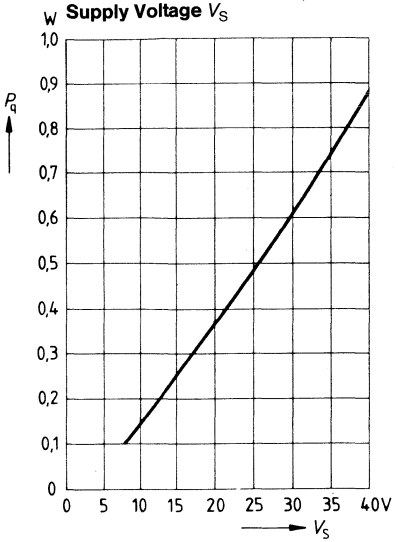


Characteristics for determining the typical power dissipation during chopper operation without phase reversal.
Parameters: $L_{load} = 10$ mH, $C_7 = 820$ pF; $R_7 = 33$ kΩ; $T_C = 25$ °C

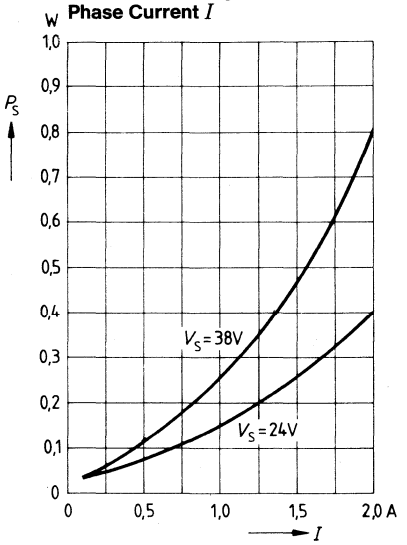
Saturation Loss P_{sat} versus Phase Current I



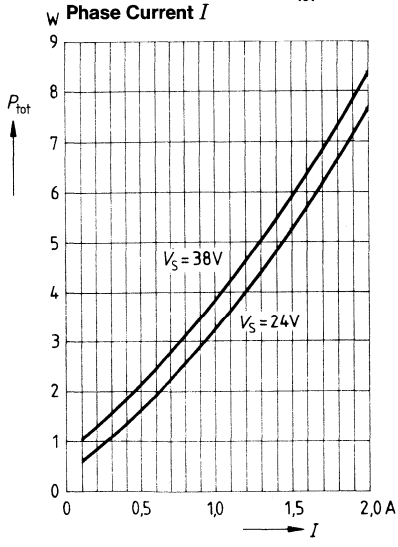
Quiescent Current Loss P_q versus Supply Voltage V_S



Switching Loss P_S versus Phase Current I



Total Power Dissipation P_{tot} versus Phase Current I



9

SIEMENS

2-Phase Stepper-Motor Driver

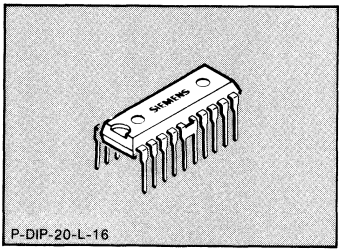
TCA 3727

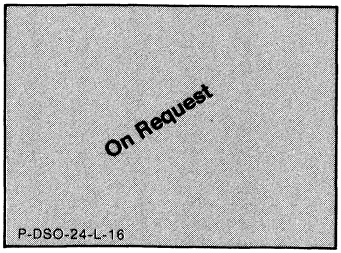
Advance Information

Bipolar IC

Features

- 2 x 1 A outputs 50 V
- Driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Outputs free of crossover current
- Offset-phase turn-on of output stages
- Z-diode for logic supply
- Low standby-current drain
- Full, half, quarter, mini, quasi-sine step





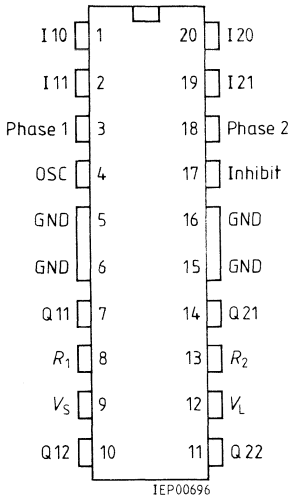
Type	Ordering Code	Package
▼ TCA 3727	Q67000-A8302	P-DIP-20-L-16
▼ TCA 3727 G	on request	P-DSO-24-L-16 (SMD)

▼ New type

TCA 3727 is a bipolar, monolithic IC for driving stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip, which permits switched current control of motors with 1.0 A per phase at operating voltages up to 50 V.

The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration have integrated, fast free-wheeling diodes and are free of crossover current. The logic is supplied either separately with 5 V or taken by the motor supply voltage by way of a series resistor and an integrated Z-diode. The device can be driven directly by a microprocessor with the possibility of all modes from full step through half step to mini step or quasi sine.

Pin Configuration P-DIP-20-L-16
(top view)



Pin Definitions and Functions (P-DIP-20-L-16)

Pin	Symbol	Function
1, 2, 19, 20	I_{10}, I_{11}, I_{21}, I_{20}	Digital control inputs I_{xo}, I_{x1} for the magnitude of the current of the particular phase.

I_{x1}	I_{xo}	Phase current	Example of motor status
H	H	0	No current
H	L	0.25 x I_{set}	Hold
L	H	I_{set}	Normal mode
L	L	1.5 x I_{set}	Accelerate

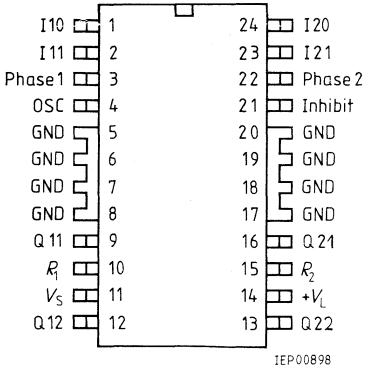
3	Phase 1	**Input phase 1;** controls the current flow through phase winding 1. On H potential the phase current flows from Q11 to Q12, on L potential in the reverse direction.
5, 6, 15, 16	GND	**Ground;** pins 5 and 6 are connected with one another internally and with pins 15 and 16.
13	R_2	Resistor R_2 for sensing the current in phase 2

Pin Definitions and Functions (P-DIP-20-L-16) (cont'd)

Pin	Symbol	Function
4	OSC	**Oscillator;** works at approx. 100 kHz if this pin is wired to ground across 1 nF. A 1/2 divider produces the timing for the current regulators of each phase from this frequency and thus offset-phase turn-on of the two output stages.
7, 10	Q11, Q12	Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes. The outputs are shortcircuit-proof to ground and $+V_S$.
9	$+V_S$	**Supply voltage;** block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 µF in parallel with a ceramic capacitor of 220 nF.
12	$+V_L$	**Logic voltage;** either supply with 5 V or connect to $+V_S$ across a series resistor. A Z diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 µF.
11, 14	Q22, Q21	Push-pull outputs Q21, Q22 for phase 2 with integrated free-wheeling diodes. The outputs are shortcircuit-proof to ground and $+V_S$.
17	Inhibit	**Inhibit input;** the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.
18	Phase 2	**Input phase 2;** controls the current flow through phase winding 2. On H potential the phase current flows from Q21 to Q22, on potential in the reverse direction.
8	R_1	Resistor R_1 for sensing the current in phase 1

The output stages will be turned-on offset-phased at the vertex of the oscillator signal.

Pin Configuration P-DSO-24-L-16
(top view)

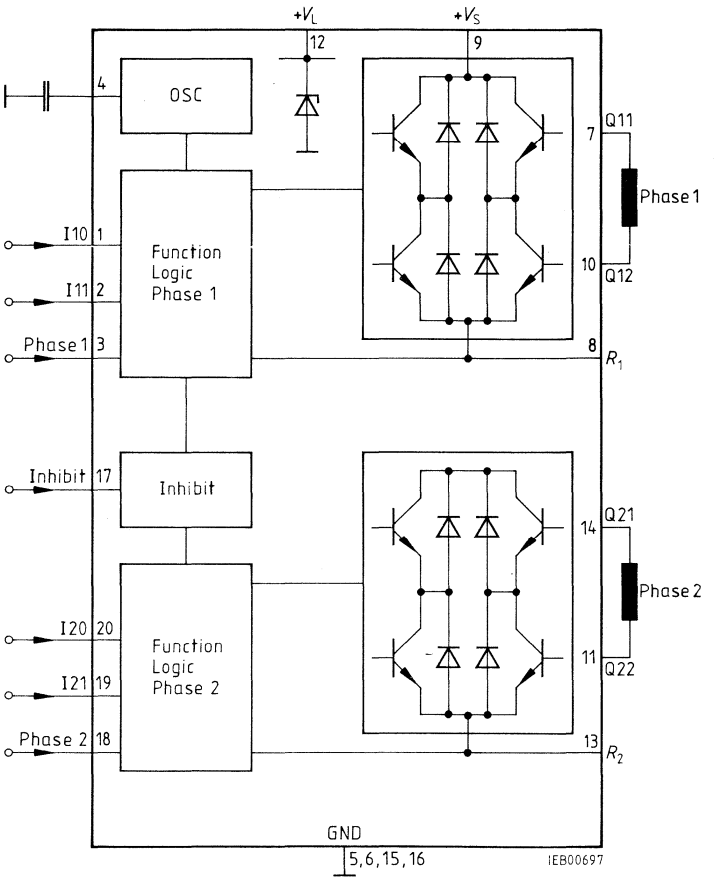


Pin Definitions and Functions (P-DSO-24-L-16)

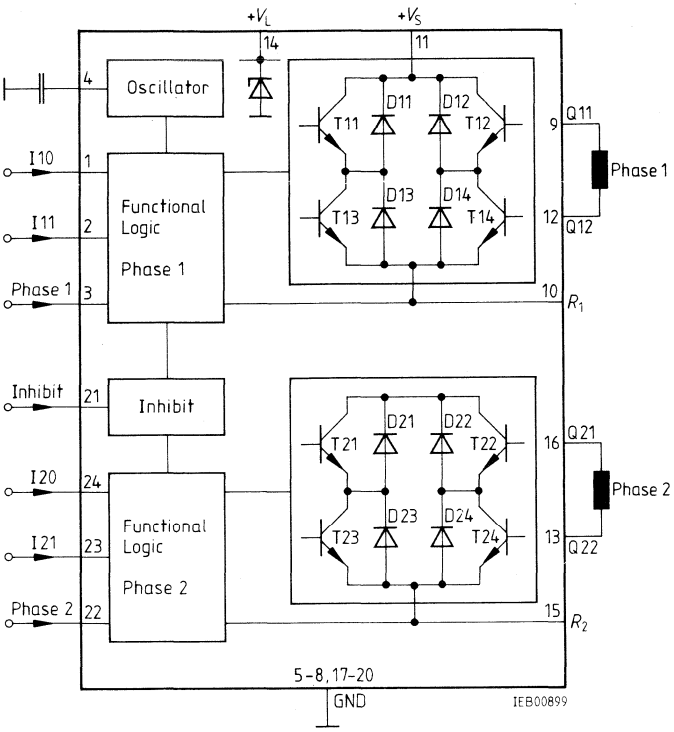
<table>
<tr><th>Pin</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1, 2,
23, 24</td><td>I10, I11,
I21, I20</td><td>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.
<table>
<tr><th>IX1</th><th>IX0</th><th>Phase Current</th><th>Example of motor status</th></tr>
<tr><td>H</td><td>H</td><td>0</td><td>No current</td></tr>
<tr><td>H</td><td>L</td><td>0.5 x I_{set}</td><td>Hold</td></tr>
<tr><td>L</td><td>H</td><td>I_{set}</td><td>Normal mode</td></tr>
<tr><td>L</td><td>L</td><td>1.5 x I_{set}</td><td>Accelerate</td></tr>
</table></td></tr>
<tr><td>3</td><td>Phase 1</td><td>Input phase 1; controls the current flow through phase winding 1. On H potential the phase current flows from Q11 to Q12, on L potential in the reverse direction.</td></tr>
<tr><td>5, 6, 7, 8, 17,
18, 19, 20</td><td>GND</td><td>Ground; pins 5 and 6 are internally connected with one another and with pins 15 and 16.</td></tr>
<tr><td>4</td><td>OSC</td><td>Oscillator; works at approx. 100 kHz, if this pin is wired to ground across 470 nF. A 1/2 divider produces the timing for the current regulators of each phase from this frequency and thus offset-phase turn-on of the two output stages.</td></tr>
<tr><td>10</td><td>R_1</td><td>Resistor 1. For sensing the current of phase 1.</td></tr>
<tr><td>9, 12</td><td>Q11, Q12</td><td>Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.</td></tr>
<tr><td>11</td><td>$+V_S$</td><td>Supply voltage; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 µF in parallel with a ceramic capacitor of 220 nF.</td></tr>
<tr><td>14</td><td>$+V_L$</td><td>Logic voltage; either supply with 5 V or connect to V_S across a series resistor. A Z-diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 µF.</td></tr>
<tr><td>13, 16</td><td>Q22, Q21</td><td>Push-pull outputs Q22, Q 21 for phase 2 with integrated free-wheeling diode.</td></tr>
<tr><td>15</td><td>R_2</td><td>Resistor 2 for sensing the current of phase 2.</td></tr>
<tr><td>21</td><td>Inhibit</td><td>Inhibit input; the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.</td></tr>
<tr><td>22</td><td>Phase 2</td><td>Input phase 2; controls the current flow through phase winding 2. On H potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.</td></tr>
</table>

9

Block Diagram



Block Diagram



Absolute Maximum Ratings

Temperature T_C −40 to 125 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Supply voltage	V_S	0	60	V	
Supply voltage	V_S	0	80	V	$t < 400$ ms
Z-current of V_L	I_L		50	mA	
Output current	I_Q		1	A	Limited internally
Ground current	I_{GND}		2	A	
Logic Inputs	V_{IXX}	−6	V_L+0.5	V	I_{XX} phase 1, 2; Inhibit
Diode currents					
to $+V_S$	I_{F+}		1	A	
to ground	I_{F-}		1	A	
Junction temperature	T_J		150	°C	
Storage temperature	T_{Stg}	−50	125	°C	

Operating Range

Supply voltage	V_S	5	50	V	
Logic voltage	V_L	4.5	6.5	V	
Case temperature	T_C	−40	125	°C	Measured on pin 5 $P_{diss} = 2$ W
Output current	I_Q		750	mA	
Logic Inputs	V_{IXX}	−5	V_L	V	I_{XX} phase 1, 2; Inhibit
Thermal resistance					
system – air	R_{thSA}		56	K/W	(P-DIP-20-L-16)
system – air	R_{thSA}		40	K/W	Soldered on a 35 µm thick 20 m² PC board copper area (P-DIP-20-L-16)
system – case	R_{thSC}		10	K/W	Measured on pin 5 (P-DIP-20-L-16)
system – air	R_{thSA}		75	K/W	(P-DSO-24-L-12)
system – air	R_{thSA}		35	K/W	Soldered on a 35 µm thick 20 m² PC board copper area (P-DSO-24-L-12)
system – case	R_{thSC}		6	K/W	Measured on pin 5 (P-DSO-24-L-12)

Characteristics

$V_S = 40$ V; $V_L = 5$ V; $T_C = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Current Consumption						
from $+V_S$	I_S		1		mA	$V_{inh} = V_{IL}$
from $+V_S$	I_S		5		mA	$V_{inh} = V_{iH}$; $I_{Q1/2} = 0$
from $+V_L$	I_L		1		mA	$V_{inh} = V_{IL}$
from $+V_L$	I_L		30		mA	$V_{inh} = V_{IH}$
Oscillator						
Output charging current	I_{OSC}		95		µA	
Charging threshold	$V_{OSC\,L}$		1.4		V	
Discharging threshold	$V_{OSC\,H}$		2.4		V	
Frequency	f_{OSC}		100		kHz	$C_{ext} = 1$ nF
Phase-Current Selection						
No current	I_Q		0		mA	$I_{x0} = H$; $I_{x1} = H$
Hold	I_Q		250		mA	$V_{REF\,1/2} = 5$ V; $I_{xo} = L$; $I_{x1} = H$
Setpoint	I_Q		500		mA	$V_{REF\,1/2} = 5$ V; $I_{xo} = H$; $I_{x1} = L$
Accelerate	I_Q		750		mA	$V_{REF\,1/2} = 5$ V; $I_{xo} = L$; $I_{x1} = L$
Logic Inputs (I_{x1}; I_{xo}; Phase x; Inhibit)						
Threshold voltage	V_I	1.4	1.7	2.0	V	
Input current low	I_{IL}	−10			µA	$V_I = 1.4$ V
L-input current	I_{IL}	−100			µA	$V_I = 0$ V
H-input current	I_{IH}			10	µA	$V_I = 5$ V
Standby						
Threshold	$V_{Inhibit\,E}$		2.9		V	
Hysteresis	$V_{Inhibit\,Hy}$		0.7		V	
Overvoltage Cutout						
Overvoltage threshold	V_{TO}		55		V	
Overvoltage hysteresis	V_{HO}		1		V	
Internal Logic						
Z-Voltage	V_{LZ}		7.4		V	$I_L = 50$ mA

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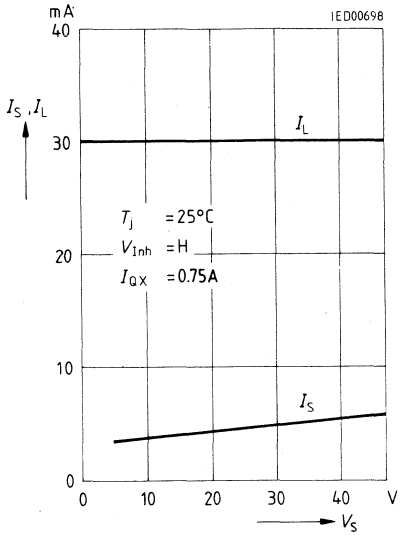
Characteristics

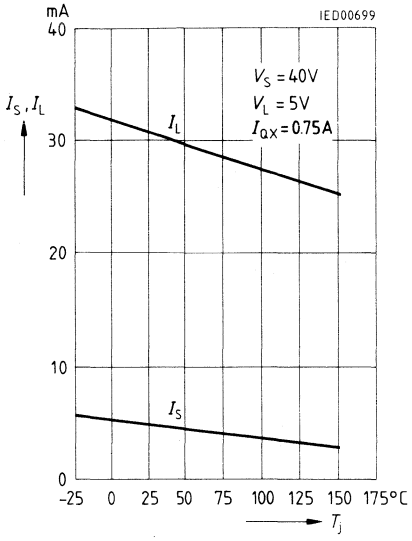
Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair						
Saturation voltage	V_{sat1}		0.4		V	$I_Q = -0.3$ A
Saturation voltage	V_{sat1}		1.0		V	$I_Q = -0.5$ A
Reverse current	I_{R1}		300		µA	$V_Q = 40$ V
Forward voltage	V_{F1}		0.9		V	$I_Q = 0.3$ A
Forward voltage	V_{F1}		1.0		V	$I_Q = 0.5$ A
Diode Transistor Source Pair						
Saturation voltage	V_{satuC}		1.0		V	$I_Q = 0.3$ A; charge
Saturation voltage	V_{satuD}		0.4		V	$I_Q = 0.3$ A; discharge
Saturation voltage	V_{satuC}		1.3		V	$I_Q = 0.5$ A; charge
Saturation voltage	V_{satuD}		0.8		V	$I_Q = 0.5$ A; discharge
Reverse current	I_{Ru}		300		µA	$V_Q = 0$ V
Forward voltage	V_{Fu}		1.0		V	$I_Q = -0.3$ A
Forward voltage	V_{Fu}		1.2		V	$I_Q = -0.5$ A
Diode leakage current	I_{SL}		1		mA	$I_F = -0.5$ A

Diagrams

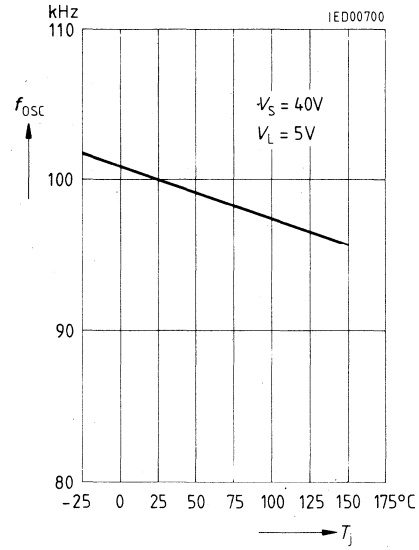
Quiescent current I_S, I_L versus supply voltage V_S



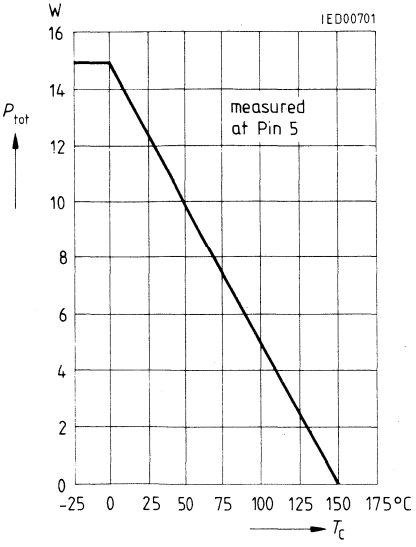
Quiescent current I_S, I_L versus junction temperature T_j



Oscillator frequency f_{OSC} versus junction temperature T_j



Permissible power dissipation P_{tot} versus case temperature T_C



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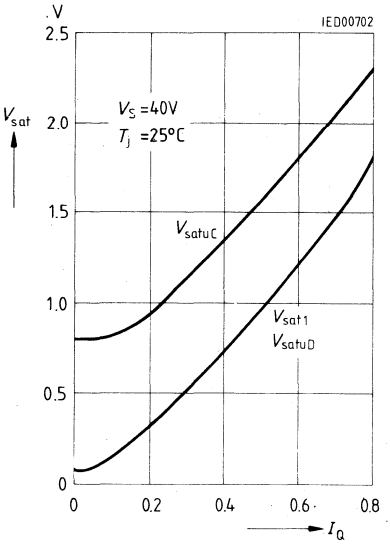
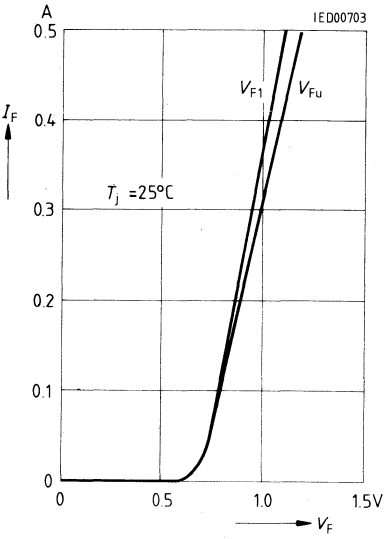
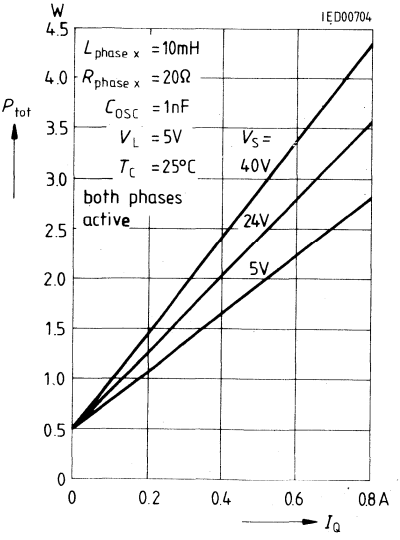
Output saturation voltages V_{sat} versus output current I_Q



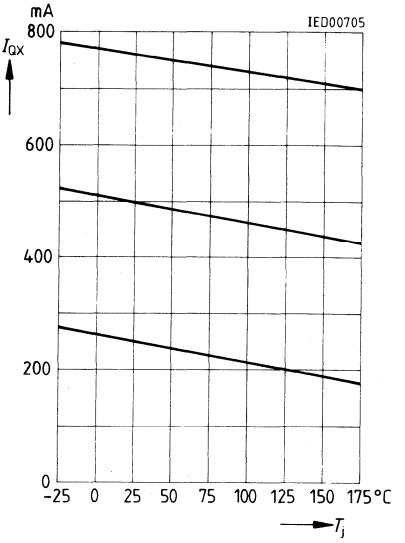
Forward current I_F of free-wheeling diodes versus forward voltages V_F



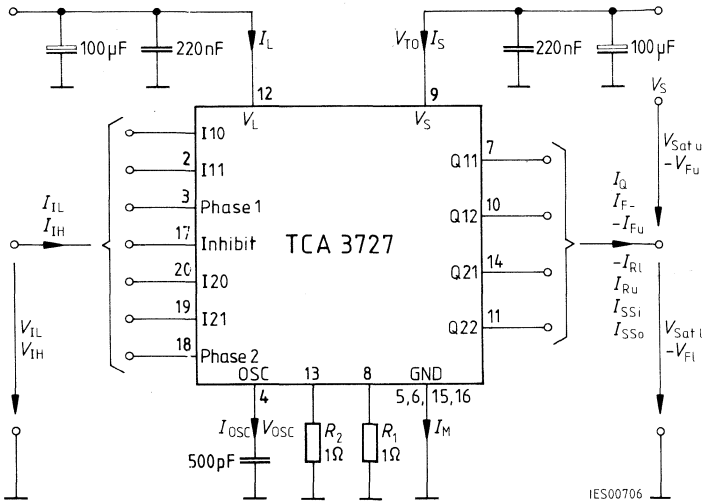
Permissible power dissipation P_{tot} versus output current I_Q



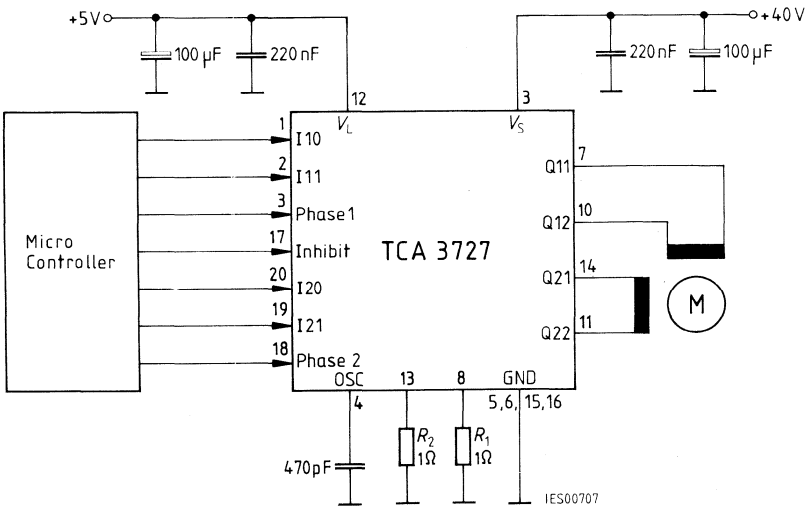
Output current I_{QX} versus junction temperature T_j



Test Circuit

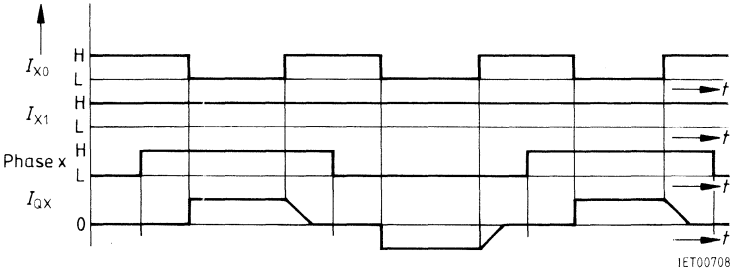


Application Circuit

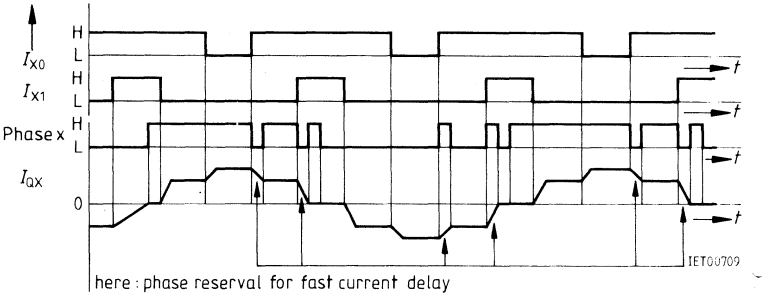


Diagrams

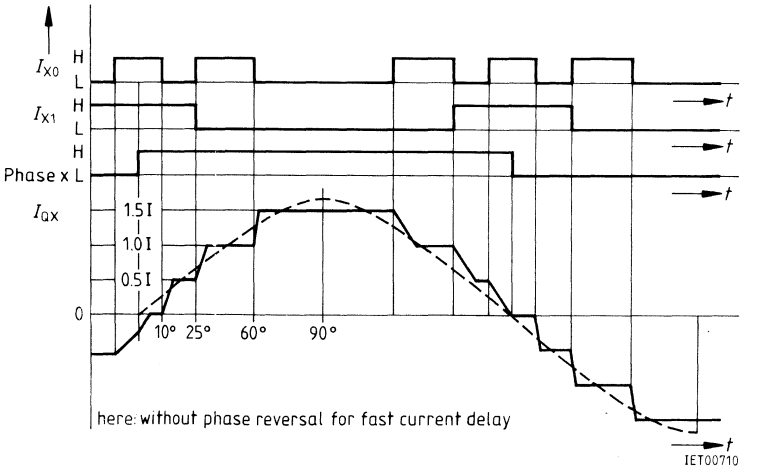
Half-Step Operation



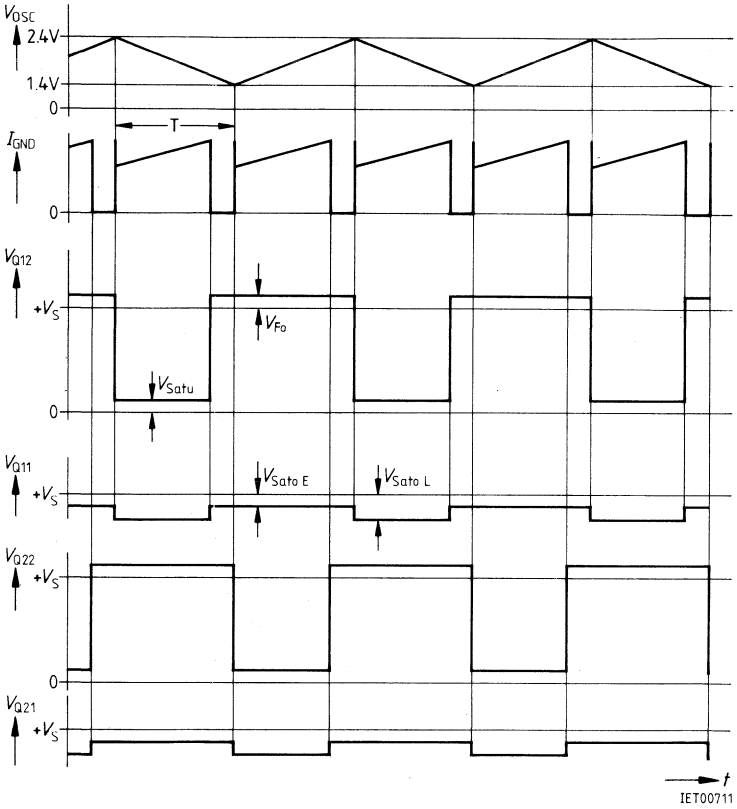
Quarter-Step Operation



Quasi-Sine Operation



Current Control



Operating conditions:

V_S	= 40 V	$V_{phase\ x}$	= H
V_L	= $V_{REF\ x}$ = 5 V	$V_{Inhibit}$	= H
$L_{phase\ x}$	= 10 mH	V_{xx}	= L
$R_{phase\ x}$	= 20 Ω		

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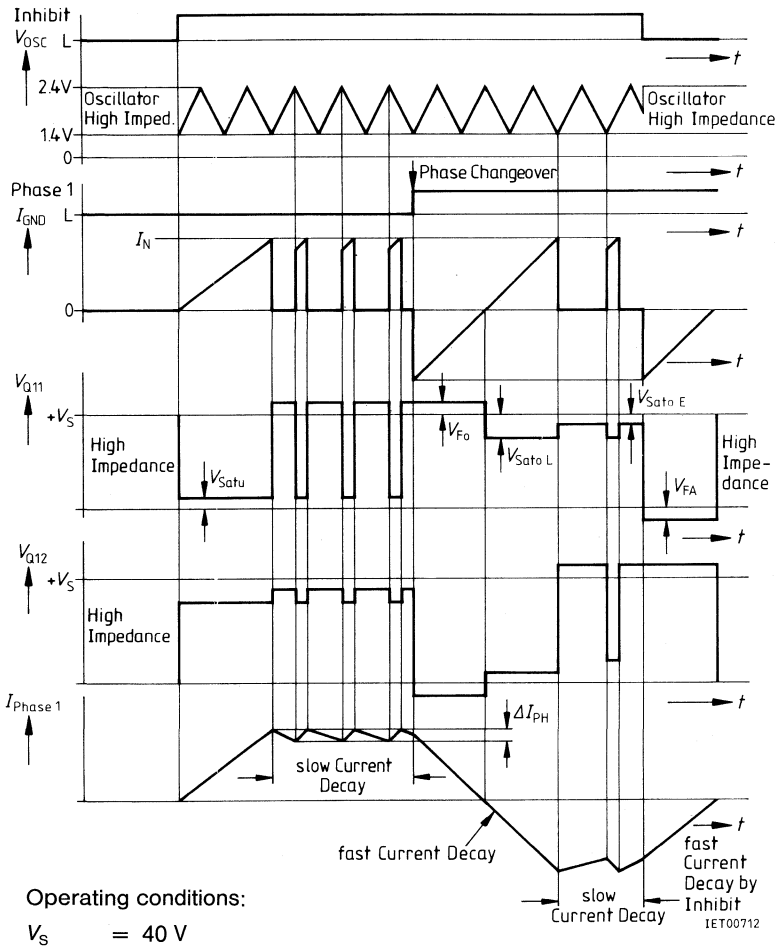
Phase Reversal and Inhibit



Operating conditions:

V_S = 40 V
V_L = $V_{REF\,x}$ = 5 V
$L_{phase\ 1}$ = 10 mH
$R_{phase\ 1}$ = 20 Ω
I_{1x} = L; I_{2x} = H

$$\Delta I_{PH} = T \frac{V_O + V_I}{V_O + V_I}$$

$V_O = V_S - V_{satu} - V_{sat1}$
$V_I = V_{Fu} + V_{satu} + I_{phase} \times R_{phase}$

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat} (transistor saturation voltage and diode forward voltages),

quiescent losses P_q (quiescent current times supply voltage) and

switching losses P_s (turn-on/turn-off operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = P_{sat} + P_q + P_s + I_L \times V_L$$

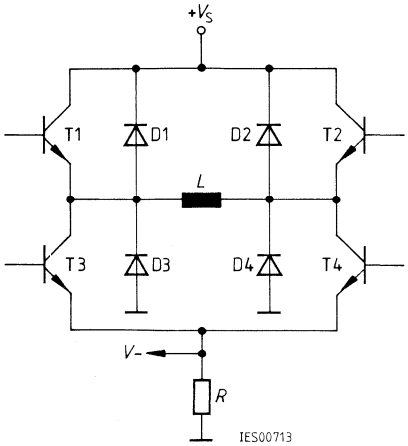
where

$$P_{sat} = I_N \{V_{sat1} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d)\}$$

$$P_q = I_q \times V_S + I_L \times V_L$$

$$P_s = \frac{V_S}{T} \left\{ \frac{i_D \times t_{Don}}{2} + \frac{(i_D + i_R)\, t_{On}}{4} + \frac{I_N}{2} (t_{Doff} + t_{Off}) \right\}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_P = conducting time of chopper transistor
t_{On} = turn-on time
t_{Off} = turn-off time
t_{Don} = turn-on delay
t_{Doff} = turn-off delay
T = cycle duration
d = duty cycle t_P/T
V_{sat1} = saturation voltage of sink transistor (T3.4)
V_{satuC} = saturation voltage of source transistor (T1.2) during charge cycle
V_{satuD} = saturation voltage of source transistor (T1.2) during discharge cycle
V_{Fu} = forward voltage or free-wheeling diode (D1.2)
V_S = supply voltage



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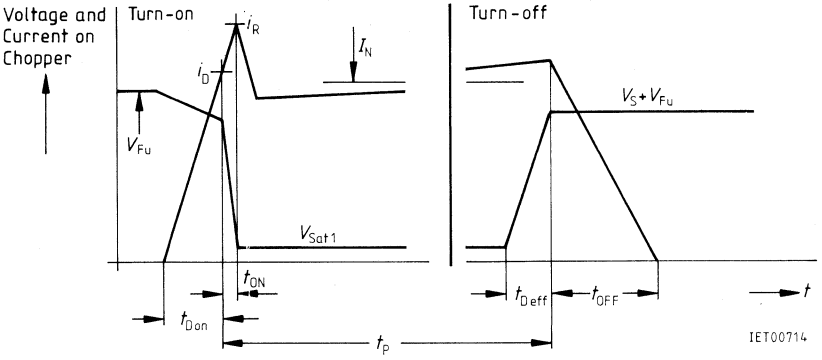
Voltage and Current on Chopper Transistor



SIEMENS

Pulse-Width Modulator

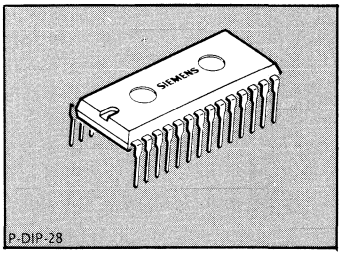
SLE 4520

Preliminary Data

MOS IC

Features

- Digital sine synthesis for controlling the speed and torque of three-phase motors
- 2-chip solution (e.g. SAB 8051 with SLE 4520) for easy configuration of a powerful frequency converter.
- Motor frequencies from 0 to 3 kHz selectable at a switching frequency up to 23.4 kHz
- Adaptation to different output stages through programmable dead time.
- Functional and performance features determined by dedicated software.



Type	Ordering Code	Package
SLE 4520	Q671000-H8271	P-DIP-28

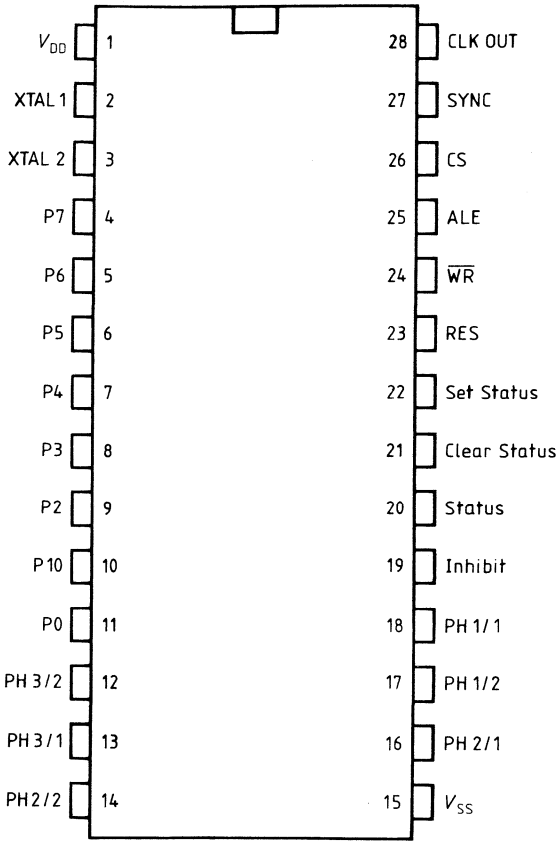
Application

The new pulse-width modulator (PWM) converts an 8-bit data word into a rectangular signal of corresponding width.

Three independently operating channels consisting of a latch, loadable counter and zero detector are used for this purpose. Together with a microcontroller (e.g. SAB 8051) and suitable software, pulses are generated to drive AC converters and inverters (three-phase) with an almost unlimited range of waveforms (sinusoidal, triangular) and phase relationships. An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program dead times are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage the *V/f* ratio of which is kept almost constant with variable frequency. For the generation of this three-phase voltage a frequency converter is required, which rectifies and filters the AC supply voltage and, subsequently, reconverts it into an AC voltage of another frequency the aid of a drive circuit and three power half-bridges. In order to avoid high losses the output stages operate in switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulses with a repetition frequency (switching frequency) up to and above the audible range, a drive block consisting of the SAB 8051 microcontroller and the SLE 4520 PWM as a minimum configuration has proved to be best suited to do the job.

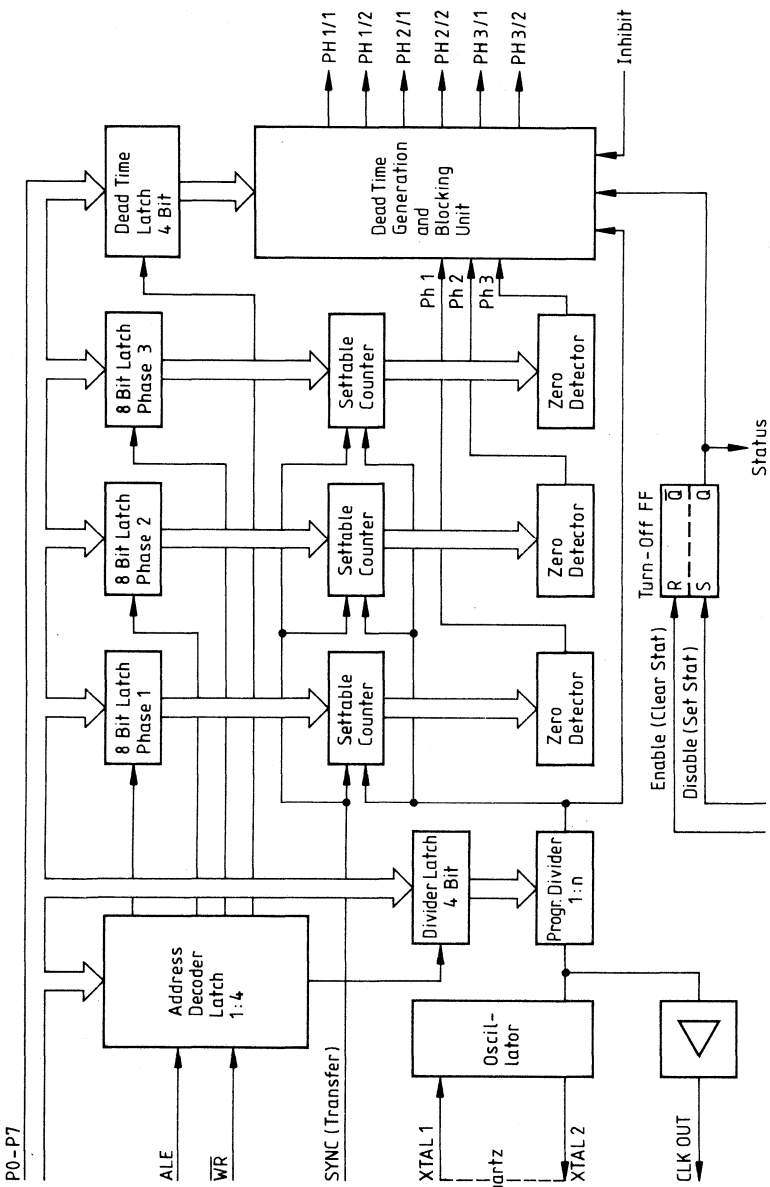
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	+5 V pin
2	XTAL1	Crystal pin
3	XTAL2	Crystal pin
4	P7	Data bus pins (inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P10	
11	P0	
12	PH 3/2	Output phase 3 inverted
13	PH3/1	Output phase 3 normal (active low)
14	PH2/2	Output phase 2 inverted
15	V_{SS}	Ground
16	PH2/1	Output phase 2 normal (active low)
17	PH1/2	Output phase 1 inverted
18	PH1/1	Output phase 1 normal (active low)
19	INHIBIT	Inhibit (active high) sets all phase outputs to high
20	STATUS	Output of status flipflop
21	CLEAR STATUS	Resets status flipflop
22	SET STATUS	Sets status flipflop
23	RES	Chip reset
24	$\overline{WR}$	Input for $\overline{WR}$ pulse from microcontroller
25	ALE	Input for ALE clock from microcontroller
26	CS	Chip select
27	SYNC	Input for trigger pulse from microcontroller
28	CLK OUT	Output crystal frequency for microcontroller

Block Diagram



Functional Description

The following description deals with the combination of the SAB 8051 microcontroller and the SLE 4520 PWM and a program developed by Siemens. Other hardware combinations are possible as well.

An on-chip oscillator directly feeds the programmable prescaler and has a buffered output for the connected microcontroller. The interface to the microcontroller has a width of 8 bits.

Data from the SAB 8051 microcontroller to the SLE 4520 PWM are transferred via the data bus P0 using the control signals $\overline{ALE}$ and $\overline{WR}$. In the PWM component three 8-bit registers for the three phases and two 4-bit registers for dead time and divider ratio respectively as well as an address decoder latch to buffer the relevant addresses are connected to the internal data bus of the SLE 4520 **(see block diagram)**.

Addresses are as follows:

Address	Register
00	8-bit register for phase 1
01	8-bit register for phase 2
02	8-bit register for phase 3
03	dead time control register
04	divider control register

The last two registers have to be written only once when being initialized. In the case of a controller output the above-mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse-width modulator.

The required divider ratio for the production of low switching frequencies at a simultaneously high operating frequency of the microcontroller is set by the divider control register. The divider control register is best loaded with an adequate value in the starting routine.

Allocation of value and divider ratio is shown in table 1:

Table 1

Allocation of value in the divider register to the divider ratio by which the SLE 4520 operating frequency is selected

Value	Divider ratio Counter	Divider ratio Delay clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

After the ratio has been determined, the length of the switching frequency cycle should be selected in such a way that the maximum pulse width is just reached. This means that with a PWM counter clock of, e.g. 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 µs (switching frequency cycle 128 µs).

Table 2 gives a number of useful allocations of counter frequency and switching frequency for the SAB 8051 (12 MHz clock).

Table 2

Allocation of counter frequency and switching frequency of SAB 8051

Divider ratio	Counter frequency	Operating time Timer 0	Switching frequency	Resolution
1:6	2 MHz	64 µs	15.6 kHz	7 bit
1:6	2 MHz	128 µs	7.8 kHz	8 bit
1:12	1 MHz	128 µs	7.8 kHz	7 bit
1:12	1 MHz	256 µs	3.9 kHz	8 bit
1:24	500 kHz	256 µs	3.9 kHz	7 bit
1:24	500 kHz	2 x 256 µs	1.95 kHz	8 bit
1:48	250 kHz	2 x 256 µs	1.95 kHz	7 bit
1:48	250 kHz	4 x 256 µs	975 Hz	8 bit

Converting a data word into a pulse width

Pulse generation in the three processing channels is done by a presettable 8-bit down-counter and a zero detector (NOR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width 1 instruction cycle), whose repetition rate determines the length of the switching frequency, the presettable counter is loaded with the contents of the appropriate register and 0 appears at the zero detector's output (provided the register does not contain 00H).

This 0 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio serves as clock frequency for the PWM counter.

Functional Description

Dead-time control register and dead-time setting in order to avoid overlapping switching operations

The dead time between the drive pulses for the two transistors of a half-bridge must consider the storage times of the bipolar driver and the power transistors, otherwise dangerous overlapping switching operations might occur. In the pulse-width modulator the dead time is obtained by linking the pulse-width modulated signal source with a delay signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs.

The shift pulse is either $f_{\frac{CRYSTAL}{6}}$ or $f_{\frac{CRYSTAL}{4}}$, depending on the values in the divider control register.

By writing a value between 0 and 0FH into the appropriate control register 16 dead times are presettable (incl. zero dead time)

The dead time depends on the crystal frequency and the preset divider ratio. Programmable dead times for a 12-MHz crystal frequency are shown in **table 3.**

Table 3

Dead times presettable in the dead time control register using divider ratios of 1:4 and 1:6

Word in dead time memory	Divider ratio 1:4 dead time (µs)	Divider ratio 1:6 dead time (µs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

Functional Description

The interface to the power circuit is provided by outputs PH1/1 to PH3/2

Without dead time PH1/2 is inverted to PH1/1, PH2/2 to PH2/1 and PH3/2 to PH3/1. The active switching state is Low.

With a programmed dead time the negative edges of the output signal are shifted to the right by the dead time.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive block and power circuit with a current up to 20 mA.

Static or dynamic interlocking of outputs is possible

Within the duration of the inhibit signal (pin 19) all six outputs can be set to high level. In case the outputs are connected to optocouplers the light emitting diodes are currentless and all six individual transistors of the power circuit are blocked. This option is particularly necessary when switching on the drive block, as proper pulses at the pulse-width modulator output are only available after the oscillator output has been built up and the initilization routine has been executed.

As the SAB 8051 sets the port outputs to high when switched on, only one port pin of the microcontroller has to be connected to inhibit. At the end of the initialization routine this port pin is set to low.

Another way of inhibiting the outputs (hold function) is to apply a high pulse to the "Set" input (pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (pin 20) and can be used to indicate or inform the microcontroller (active high; used, for example, in the event of power failure, short circuit, overtemperature etc.).

The status flipflop is cleared by a high pulse at the "Clear Status" input (pin 21).

Features

- Generation of three pairs of pulse-width modulated rectangular pulses (phase angle between one phase and the next is, for example, 120°) to drive six individual transistors of an inverter power block.
- Programmable dead time to reliably drive both power switches of a half-bridge from

  0 to 15 x $\frac{6}{f_{crystal}}$ or 15 x $\frac{4}{f_{crystal}}$ in 15 steps.

  It is the negative edge which is in each case delayed because the output signal is active low.
- Programmable divider in the pulse-width modulator to obtain low switching frequencies (for output stages with thyristors, GTOs, and bipolar transistors) and to simultaneously operate the microcontroller at higher crystal frequencies.
- Direct drive of an optocoupler interface to isolate control and load circuits (I_{sink} = 20 mA maximum).
- All six outputs of the SLE 4520 are set to high level either dynamically by an inhibit signal (INHIBIT) or statically by an R-S flipflop (SET STATUS). Thus blocking of all six individual transistors of the power circuit is possible.
- DC braking by selecting different, fixed duty cycles in the three output pairs.
- Direction of rotation is software-reversed by changing between two phases.
- Sine-wave frequency range about 0 to > 2600 Hz.
- Switching frequency range < 1 to > 20 kHz.
- 8-bit resolution of the desired sine-wave function with a switching frequency of $\frac{f_{crystal}}{6 \times 2^8}$ or 7 bits with a switching frequency of $\frac{f_{crystal}}{6 \times 2^7}$ ($f_{crystal}$ = 12 MHz and resolution = 7 bits result in a 15.6 kHz switching frequency).
- Smallest increment of the pulse-width is 333 ns with $f_{crystal}$ = 12 MHz and divider ratio 1:4.
- Changing the switching frequency cycle in 1-µs steps allows the transition from one sine-wave frequency stage to the next quasi continuously (virtually analog).
- Evaluating the bit pattern at one port of the microcontroller enables many (256) different speed-control programs to be selected.
- Low current consumption of the pulse-width modulator due to ACMOS technology.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_I	−0.3		V_{DD} +0.3	V
Storage temperature	T_{stg}	−50		125	°C
Total power dissipation	P_{tot}			500	mW
Power dissipation per output	P_Q			50	mW

Operating Range

Supply voltage	V_{CC}	4.5	5	5.5	V
Supply current (outputs not connected)	I_{DD}			15	mA
Operating frequency	f_{CLK}			12	MHz
Ambient temperature	T_A	−40		85	°C

DC Characteristics

$T_A = 25\,°C$

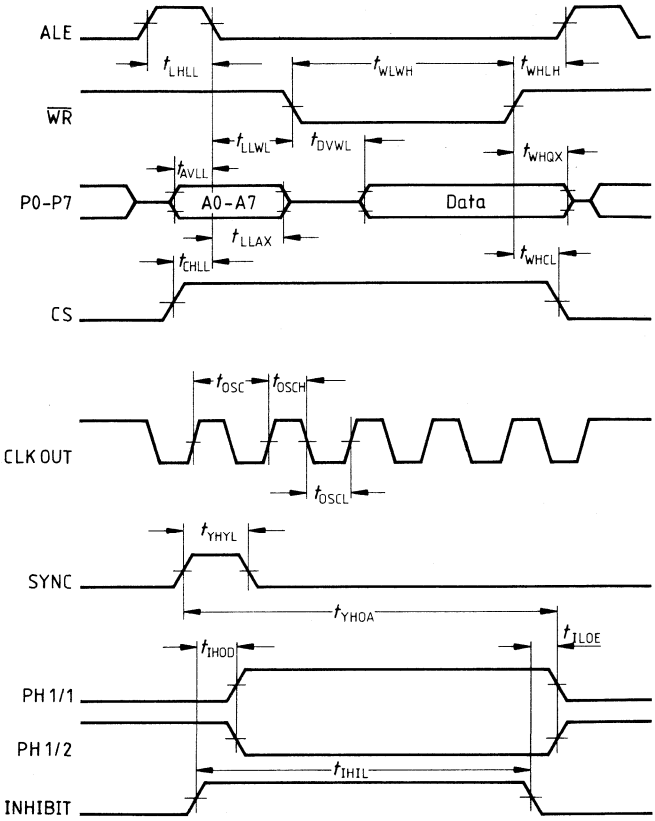
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
All Input Signals Except XTAL2						
H-input voltage	V_{IH}	2.2		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Input Signal XTAL2 for External Clock						
H-input voltage	V_{IH}	4.0			V	
L-input voltage	V_{IL}	0		0.3	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Output Signals STATUS, CLK OUT						
H-output voltage	V_{QH}	V_{DD}−0.8			V	$I_Q = 0.5$ mA
L-output voltage	V_{QL}			0.4	V	$I_Q = 1.6$ mA
Output Signals PH 1/1, PH 1/2, PH 2/2, PH 3/1, PH 3/2						
L-output voltage	V_{QL}			1	V	$I_Q = 20$ mA
H-output voltage	V_{QH}	V_{DD}−0.8 V			V	$I_Q = 1$ mA

AC Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LHLL}	100		ns
Address setup to ALE	t_{AVLL}	30		ns
Address hold after ALE	t_{LLAX}	30		ns
WRN pulse width	t_{WLWH}	200		ns
WRN high to ALE high	t_{WHLH}	50		ns
Data setup after WRN low	t_{DVWL}		20	ns
ALE low to WRN low	t_{LLWL}	100		ns
Data hold after WRN[1)]	t_{WHQX}	30		ns
Oscillator period	t_{OSC}	83		ns
High time	t_{OSCH}	35		ns
Low time	t_{OSCL}	35		ns
SYNC pulse width	t_{YHYL}	200		ns
INHIBIT low to output enable	t_{ILOE}		100	ns
Delay between SYNC high to output active	t_{YHOA}	4 t_{OSC}	97 t_{OSC} +20	ns
Chip select setup to ALE low	t_{CHLL}	20		ns
Chip select hold after WRN high	t_{WHCL}	30		ns
Reset pulse width	t_{RHRL}	12 t_{OSC}		ns
Set Status pulse width	t_{SHSL}	200		ns
Clear Status pulse width	t_{CHCL}	200		ns
INHIBIT high to output disable	t_{IHOD}		100	ns
Set Status high to output disable	t_{SHOD}		100	ns
Clear Status high to output enable	t_{CHOD}		100	ns
Set Status pulse length	t_{SHTH}	100		ns
Clear Status pulse length	t_{CHTL}	100		ns
Inhibit pulse length	t_{IHIL}	100		ns

[1)] If t_{WLWH} is less than 2 t_{OSC} +20 ns, then t_{WHQX} is 50 ns

Pulse Diagrams



SIEMENS

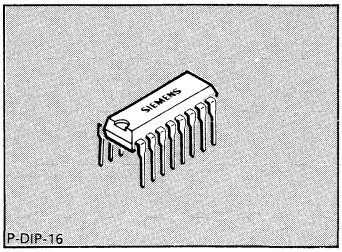
Speed Controller

TCA 955

Bipolar IC

Features

- High control accuracy
- Large supply voltage range



Typical Applications

Speed control in

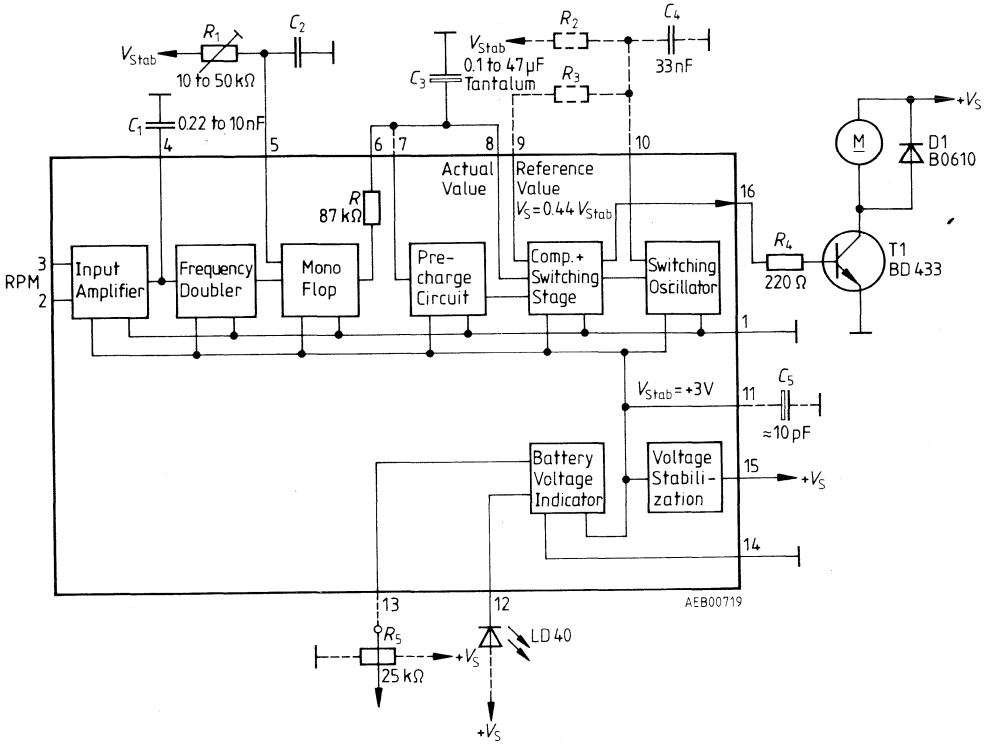
- Tape recorders
- Cassette recorders
- Record players
- Movie Cameras
- Control system drivers

Type	Ordering Code	Package
■ TCA 955	Q67000-A983	P-DIP-16

■ Not for new design

The TCA 955 is suited for the speed control of DC motors. The principle corresponds to a clocked control. Outstanding features are its high control accuracy, its large supply voltage range, and the possible current saving. Additionally, the IC features a battery voltage indicator.

Block Diagram for Speed Control with TCA 955



Dimensioning Notes

- The internal voltage stabilization offers the following advantages:
  - operation with highly varying supply voltage,
  - wide range of supply voltage.
- In order to receive pulses with a steady duty cycle at the output, symmetrical pulses must be applied to the input.
- It is recommended to use multipole tachometer generators as this improves the accuracy of control and possibly the power consumption.
- The power consumption can considerably be reduced by means of the switching frequency oscillator at low electric motor time constants.
- Higher accuracy can be obtained by using a second-order filter instead of C_3.
- When using rapidly starting motors, the precharge circuitry reduces overshoots.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage Supply voltage (pin 11 and pin 15 connected)	V_S V_S	16 6	V V
Output current pin 16 Output current pin 12 (LED output)	I_Q $I_{Q\ LED}$	200 15	mA mA
Power dissipation, LED output	$P_{Q\ LED}$	150	mW
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	85	K/W

Operating Range

With internal short-circuit stabilization (pin 11 and pin 15 connected)	V_S	2 to 6	V
With internal stabilization (V_S to pin 15)	V_S	4.8 to 16.0	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 2.2$ V to 16.0 V; $T_A = 25$ °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Controller					
Current consumption $V_S = 4.8$ V $V_S = 16$ V	I_S I_S		8.3 15.5	12.0 24.0	mA mA
Stabilized voltage $V_S = 4.8$ to 16 V	V_{stab}	2.75	3.00	3.30	V
Input threshold (pin 3) to ground Hysteresis of input threshold Offset voltage (pin 3 to pin 2)	 V_I ΔV_I V_{offset}	 0.46 x V_{11}	 0.485 x V_{11} 0.015 x V_{11} 11	 0.51 x V_{11} 0.03 x V_{11} 20	 V V mV
Input current (pin 3)	I_I			1	µA
Output transistor saturation voltage $I_Q =$ 50 mA $I_Q = 100$ mA	 $V_{Q\ sat}$ $V_{Q\ sat}$		 0.84 0.92	 1.00 1.25	 V V
Output transistor cutoff current	$I_{Q\ H}$			30	µA
Duty cycle – control range[1])	D	0		1	

Characteristics

$V_S = 2.2$ V to 16.0 V; $T_A = 25$ °C

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Controller					
Rated rpm[2]	n	$\frac{12.55}{p \cdot R_1 \cdot C_2}$	$\frac{14.85}{p \cdot R_1 \cdot C_2}$	$\frac{17.64}{p \cdot R_1 \cdot C_2}$	rpm
Error in rpm with duty cycle control[3] from 0 to 1				$\frac{0.224}{n \cdot p \cdot C_3}$	%
Switching Oscillator					
Frequency	f		$\frac{1}{0.4 \cdot R_2 \cdot C_4}$		Hz
Average voltage pin 10 Voltage pin 11 peak to peak $V_{Q\,OSC}$	$V_{Q\,OSC}$		$0.48 \times V_{11}$ $0.18 \times V_{11}$		V V
Battery Voltage Indicator					
Threshold voltage	$V_{I\,ON}$ $V_{I\,OFF}$	1.0		1.5	V V
Hysteresis	V_{hy}		220		mV
Input current	I_I			0.2	µA
Saturation voltage LED output[4]	$V_{Q\,LED}$			$0.5 + 500 \times I_{LED}$	V

Formulae

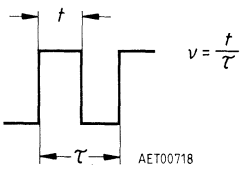
Rate rpm $n = \frac{14.85}{p \cdot R_1 \cdot C_2}$ [rpm]

Switching frequency $f = \frac{n \cdot p}{30}$ [Hz]

in operation without switching oscillator.

Reference value $V_{REF} = 0.44 \times V_{11}$ [V]
Precharging voltage at C_3 $V_F = 0.87 \times V_{REF}$ [V]
(pin 6 and pin 7 connected)

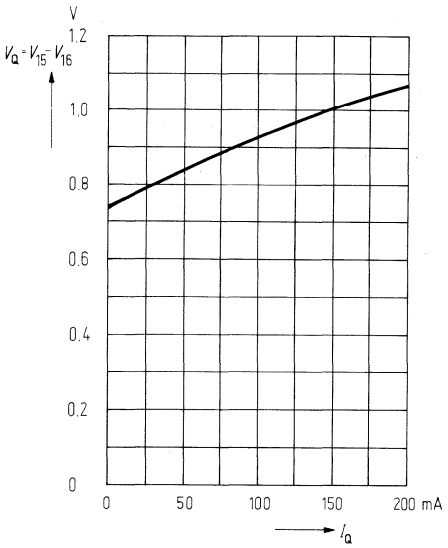
[1]) Duty cycle



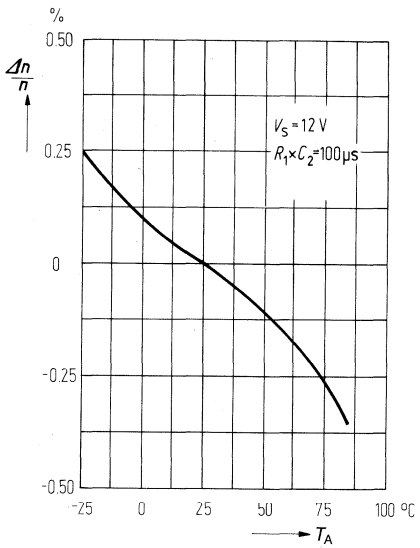
$\nu = \frac{t}{\tau}$

[2]) p = number of pole pairs of the tachometer generator.
[3]) in applications without switching oscillator.
[4]) A protective resistor of 500 Ω ± 20% is integrated inside the IC.

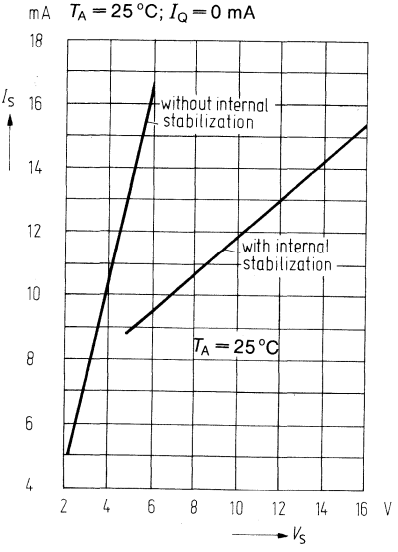
Saturation voltage of output transistor
Output voltage versus output current



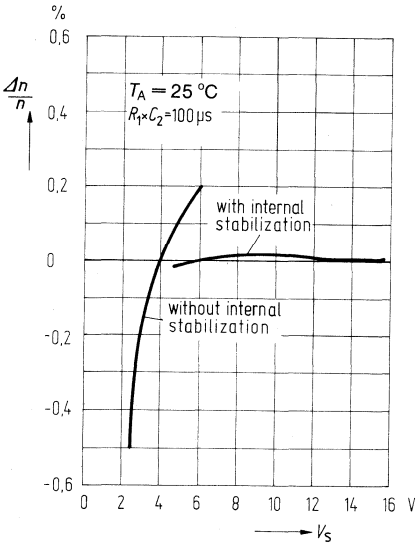
Rpm versus ambient temperature
$V_S = 12$ V; $R_1 \times C_2 = 100$ µs



Current consumption
versus supply voltage
$T_A = 25$ °C; $I_Q = 0$ mA



Rpm versus supply voltage
$T_A = 25$ °C; $R_1 \times C_2 = 100$ µs



Selector Guide

Type	Max. current (A)	Operating range V_S (V)	Max. voltage V_S (V)	Error monitoring: Overload, open circuit	Short circuit to ground	Overvoltage	Overtemperature	Typ. saturation voltage at I_{max} (V)	Temperature range (°C)	Package	Page
TLE 4211	2x2	5-20	70	●				0.6	−40 to 125	P-T66-7-H	695
TLE 4214	2x0.5	6-25	70	●				0.6	−40 to 125	P-DIP-8	705
TLE 4215	2x0.5	5-25	70	●				1.2	−40 to 125	P-DIP-16-L10	716
TLE 4216	2x0.5 4x0.05	5.2-30	40	overload			overtemp.	2x0.5 4x0.4	−40 to 110	P-DIP-20-L16	726
TLE 4220	1x4	6.5-18	65	●				0.8	−40 to 110	P-T66-7-H	737

*) The relay driver data sheet is not included in this book.
It is available stating the ordering no. B112-B6303-X-X-7600.

SIEMENS

Intelligent Double Low-Side Switch 2 x 2 A

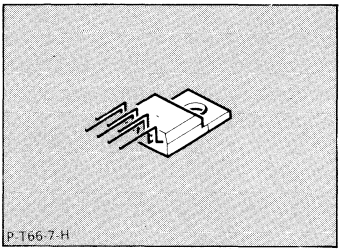
TLE 4211

Preliminary Data

Bipolar IC

Features

- Double low-side switch, 2 x 2 A
- Protection against reverse polarity
- Power limitation
- Temperature monitoring
- Voltage proof up to 70 V
- Integrated power Z diodes
- Error feedback
- Temperature range from −40 °C to 125 °C
- Suitable for applications in automotive electronics
- Short-circuit proof



Type	Ordering Code	Package
TLE 4211	Q67000-A8118	P-T66-7-H

Application

Applications in industrial electronics require intelligent power switches activated by logic signals, which are also short-circuit proof and provide for error feedback.

The IC contains two of these power switches (low-side switch). In case of inductive loads the integrated power Z diodes clamp the self-induction voltage.

Through TTL signals at the control inputs (active low) both switches can be activated independently of one another. If one of the inputs is not in use, it must be applied to high potential.

The status output (open collector) signals the following malfunctions through low potential:

- Overload
- Underload
- Short-circuit to ground
- Overvoltage

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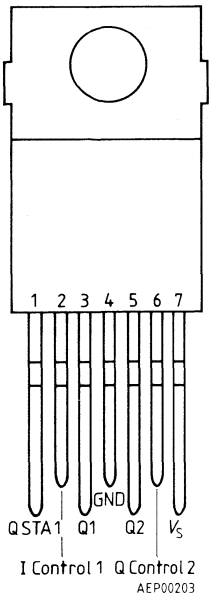
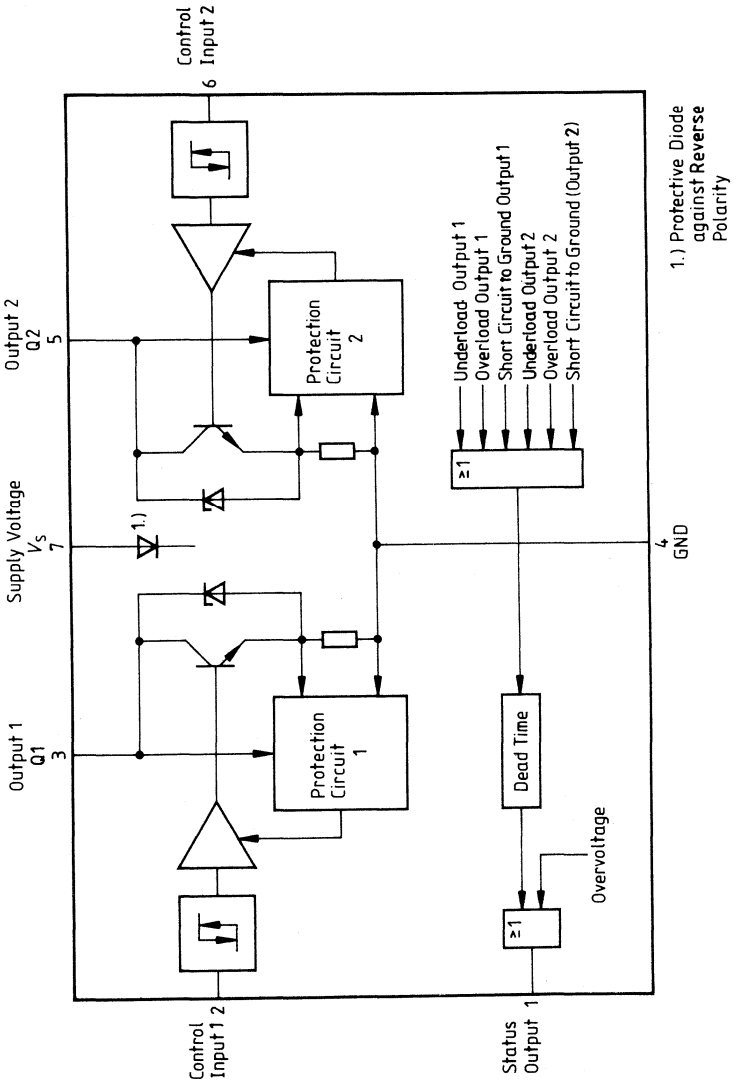
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	Q STA1	**Status output (open collector)** for both outputs; indicates overload, underload and short-circuits to ground as well as overvoltage at pin 7. In case of malfunction the status output is switched to low after a defined dead time (except overvoltage)
2	I Control 1	**Control input 1 (TTL-compatible)** activates output transistor 1 in case of low-potential
3	Q 1	**Output 1** Short-circuit proof, open collector output with 36 V power Z diode to ground
4	GND	**Ground** Wiring must be designed for a max. short-circuit current (2 x 3.5 A)
5	Q 2	**Output 2** Short-circuit proof, open collector output with 36 V power Z diode to ground
6	I Control 2	**Control input 2 (TTL-compatible)** activates output transistor 2 in case of low-potential
7	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates the malfunction without dead time.

Block Diagram



Circuit Description

Input Circuits

The control inputs comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the inverting buffer amplifiers convert the logic signal for driving the NPN power transistors.

Switching Stages

The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are short-circuit proof to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated power Z diodes.

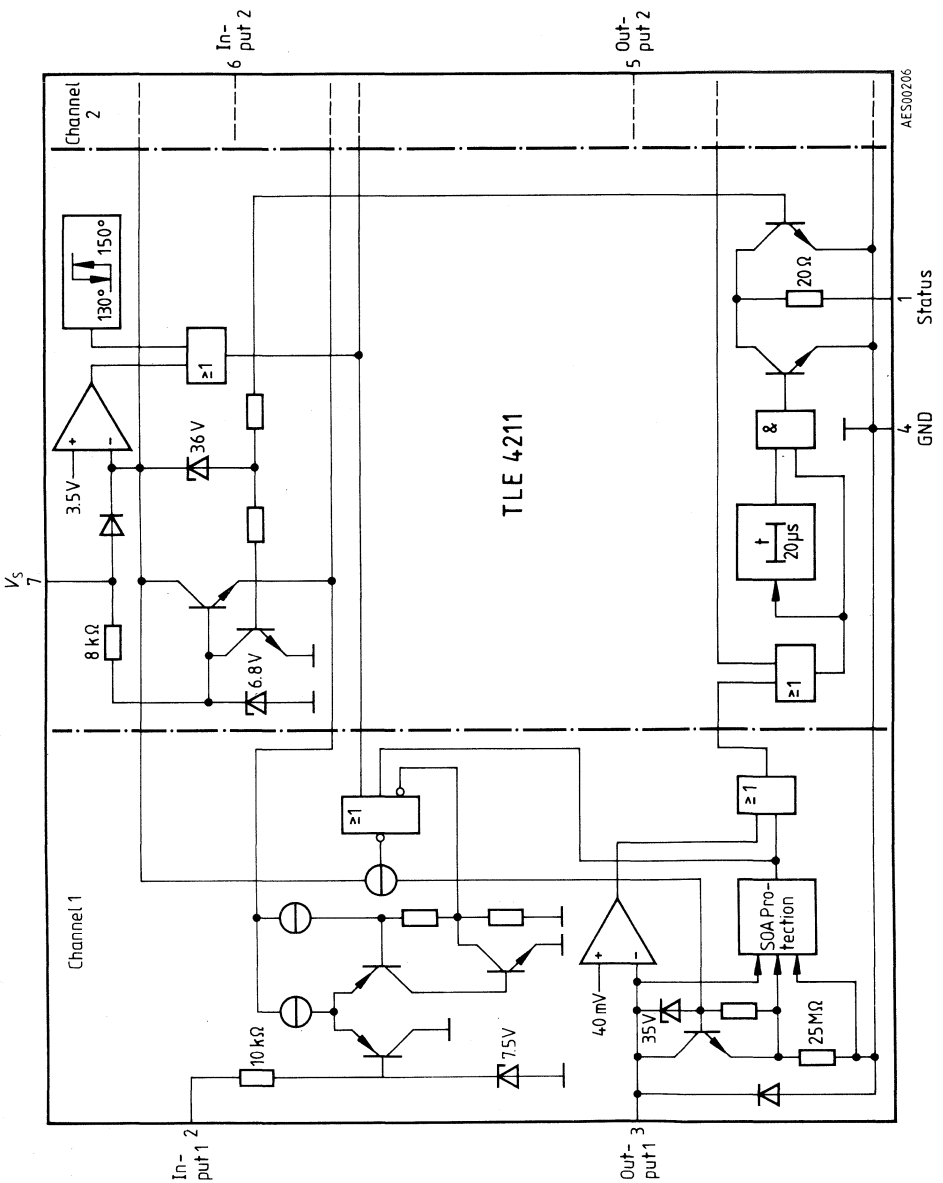
Monitoring and Protective Functions

The outputs are monitored for underload (open circuit), overload, and short-circuit to ground (see table below). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, normally high). An internally determined dead time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal destruction. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no short circuit of the load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated.

Status Output (L = Error)

	Undervoltage	**Operating range**		**Overvoltage**
		V_I = L (active)	V_I = H (passive)	
Standard operation	H	H	H	L
Overload	H	L	H	L
Underload	H	L	H	L
Short circuits to ground	H	L	L	L

Circuit Diagram



Absolute Maximum Ratings

$T_C = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Voltages				
Supply voltage (pin 7)[1]	V_S	−45	45	V
Supply voltage (pin 7) $t \leq 500$ ms	V_S		70	V
Input voltage (pin 2; pin 6)	V_I	−5	45	V
Output voltage (pin 1)	V_O	−0.3	45	V
Currents				
Switching current (pin 3; pin 5) internally limited	I_Q			
Current with reverse polarity (pin 3; pin 5) $T_C \leq 85\,°C$	I_Q	−2.8		A
Output current (pin 1)	I_O		10	mA
Max. current at inductive load	I_Q		see Diagram	
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	150	°C
Operating Range				
Supply voltage[2]	V_S	5.2	20	V
Case temperature	T_C	−40	125	°C
Thermal resistance				
system – case	$R_{th\,SC}$		4	K/W
system – air	$R_{th\,SA}$		65	K/W

[1] Refer to monitoring and protective functions
[2] Lower limit = 4.3 V, if previously V_S greater than or equal to 5.2 V (turn-on hysteresis)

Characteristics

$T_C = 25\,°C$ and $V_S = 12$ V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
General Characteristics						
Quiescent current	I_q		3.5	6	mA	$V_I = V_I > V_{IH}$
Quiescent current	I_q		100	140	mA	$V_I = V_I < V_{IL}$
Overvoltage threshold	V_{SO}	34	36	40	V	$I_O = 5$ mA; $V_O < 0.4$ V
Underload voltage switching threshold	V_{QU}		40		mV	$I_O = 5$ mA; $V_O < 0.4$ V
Underload current	I_{QU}			80	mA	$V_Q = V_{QU}$
Logic						
Control input H-input voltage L-input voltage	 V_{IH} V_{IL}	 2.0		 0.8	 V V	
Hysteresis of input voltage	ΔV_I		0.7		V	
H-input current	I_{IH}			10	µA	$V_I = 5$ V
L-input current	$-I_{IL}$			10	µA	$V_I = 0.5$ V
Status output (open collector) L-saturation voltage	V_{OSat}			0.4	V	$I_O = 5$ mA
Status dead time	t_{dS}	12	20	30	µs	[1]
Switching Stages						
Saturation voltage	V_{QSat}		0.6	0.8	V	$I_Q = 1.6$ A; $V_I < V_{IL}$
Leakage current	I_Q			300	µA	$V_Q = 6$ V; $V_I > V_{IH}$
Switch-on time	$t_{D\,ON}$		1.0	5	µs	**see fig. 1;** $R_L = 5.6\ \Omega$
Switch-off time	$t_{D\,OFF}$		1.5	5	µs	**see fig. 1;** $R_L = 5.6\ \Omega$
Forward voltage of substrate diode	$-V_{QF}$		1.4	1.8	V	$I_Q = -2.0$ A
Power Z Diode ($V_S = 40$ V; S_1 open)						
Z voltage	V_{QZ}	34	36	40	V	$I_Q = 0.1$ A
Internal impedance	τ_Z		2		Ω	0 A < I_Q < 2 A

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50% value of the status switching edge is reached.

Test Circuit

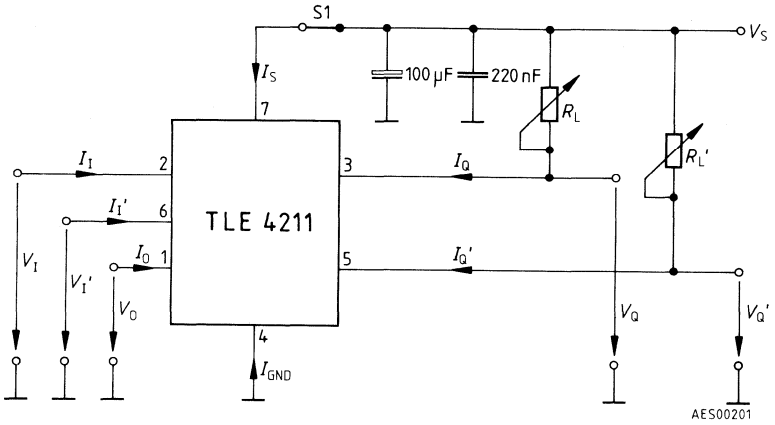
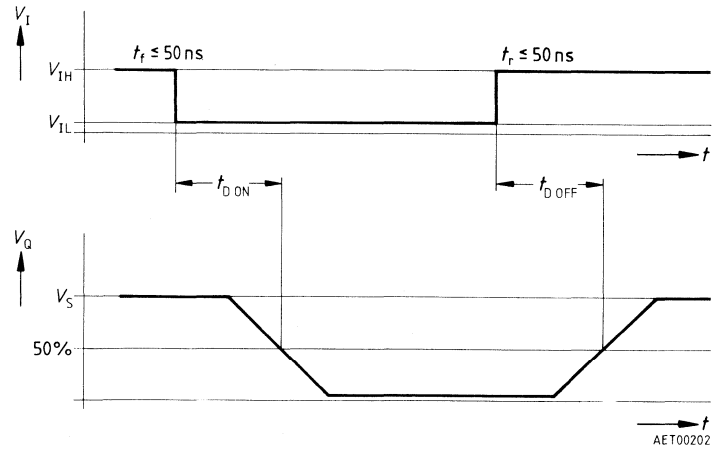
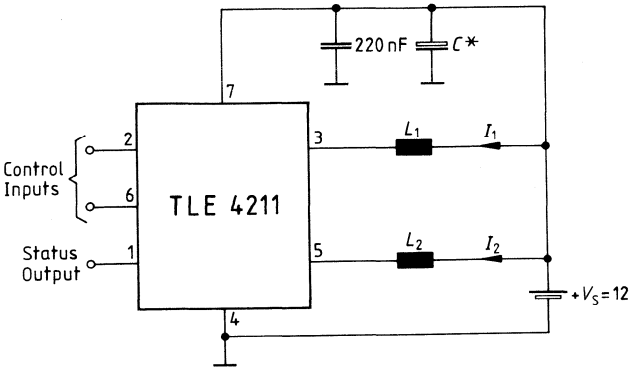


Figure 1
Timing Diagram



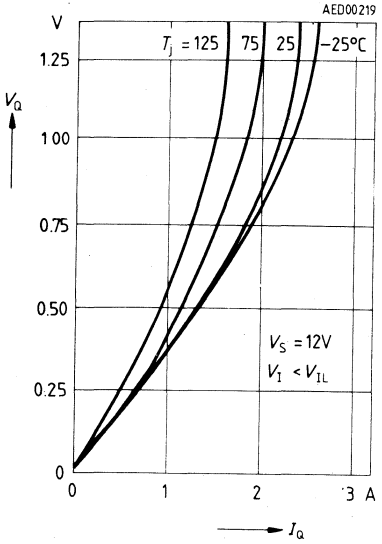
Application Circuit



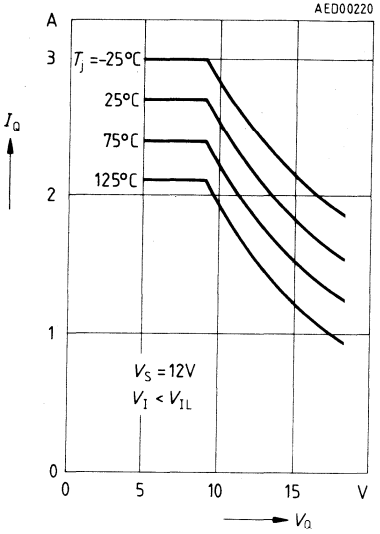
C* is to be dimensioned such that e.g. in case of a battery voltage failure the maximum ratings of the IC are not exceeded by the recirculation energy L_1, L_2.

10

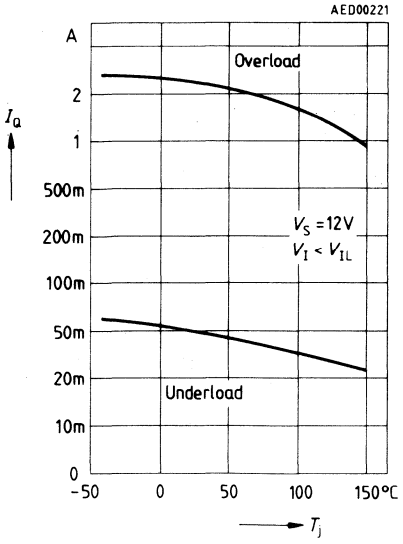
Output voltage V_Q versus output current I_Q



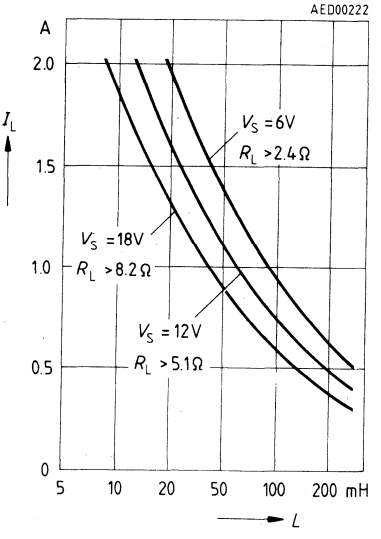
Short-circuit current I_{SC} versus output voltage V_Q



Status signal threshold versus chip temperature T_j



Maximum load current I_L versus load inductivity L



SIEMENS

Intelligent Double Low-Side Switch 2 x 0.5 A

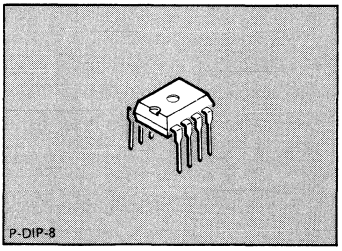
TLE 4214

Preliminary Data

Bipolar IC

Features

- Double low-side switch, 2 x 0.5 A
- Power limitation
- Overtemperature protection
- Integrated free-wheeling diodes
- Error monitoring
- Voltage proof up to 70 V
- Short-circuit proof
- Temperature range from −40 °C to 125 °C
- Suitable for applications in automotive electronics



Type	Ordering Code	Package
TLE 4214	Q67000-A8183	P-DIP-8

Application

Applications in industrial electronics require intelligent power switches activated by logic signals, which are also short-circuit proof and provide for error feedback.

The IC contains two of these power switches (low-side switches). In case of inductive loads the integrated free-wheeling diodes clamp the self-induction voltage.

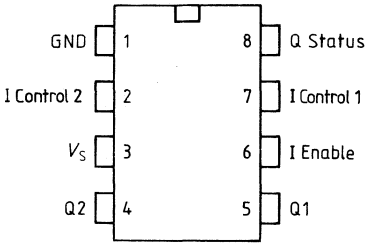
If a "high" signal is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The inputs are highly resistive and must therefore not be floated, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions through high potential:

- Overload
- Underload
- Short-circuit to ground
- Overvoltage
- Overtemperature

10

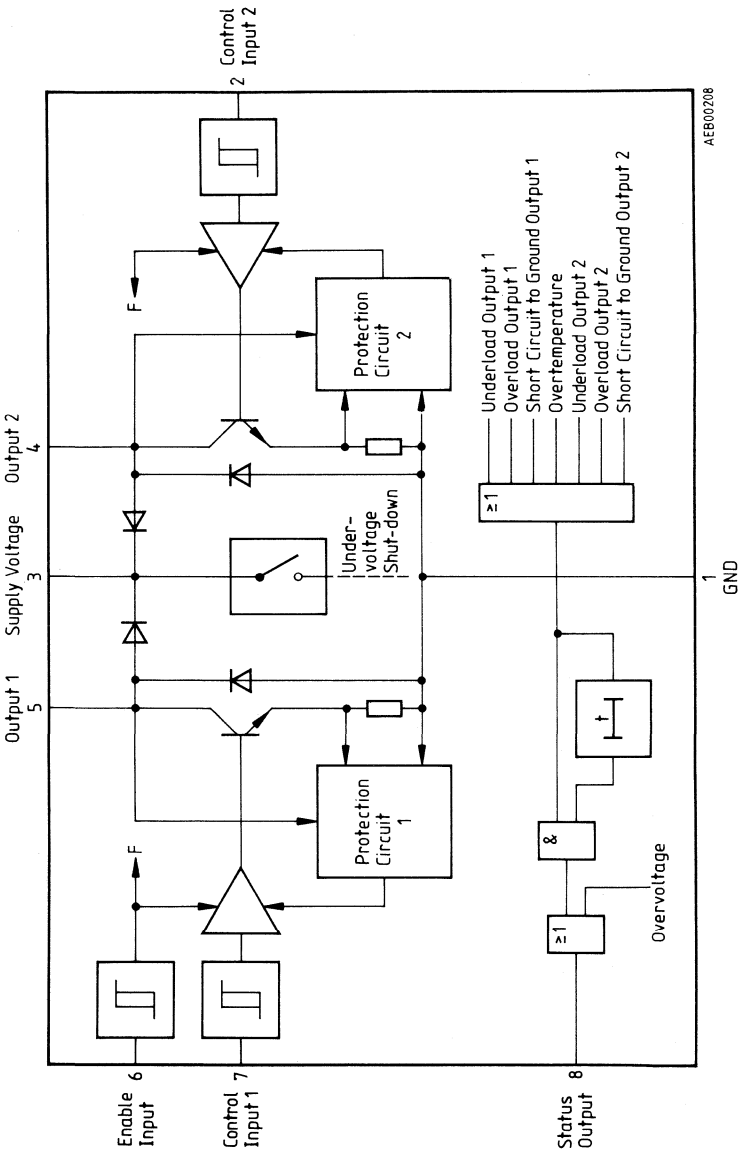
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground** Design wiring for the max. short-circuit current (2 x 1 A)
2	I Control 2	**Control input 2** (TTL compatible) activates the output transistor 2 in case of high potential
3	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates this malfunction without dead time.
4	Q2	**Output 2** Short-circuit proof, open collector output for currents up to 0.5 A, with free-wheeling diodes to supply voltage.
5	Q1	**Output 1** Short-circuit proof, open collector output for currents up to 0.5 A, with free-wheeling diodes to supply voltage.
6	I Enable	**Enable input,** active high
7	I Control 1	**Control input 1** (TTL compatible) activates output transistor 1 in case of high potential
8	Q Status	**Status output** (open collector) for both outputs; indicates over-temperature, overload, underload and short-circuits to ground in the load circuit as well as overvoltage at pin 3. Is switched to high after a defined dead time in case of malfunction (except: overvoltage)

Block Diagram



Circuit Description

Input Circuits

The control inputs and the enable input comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors to the required form.

Switching Stages

The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are short-circuit proof to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated free-wheeling diodes.

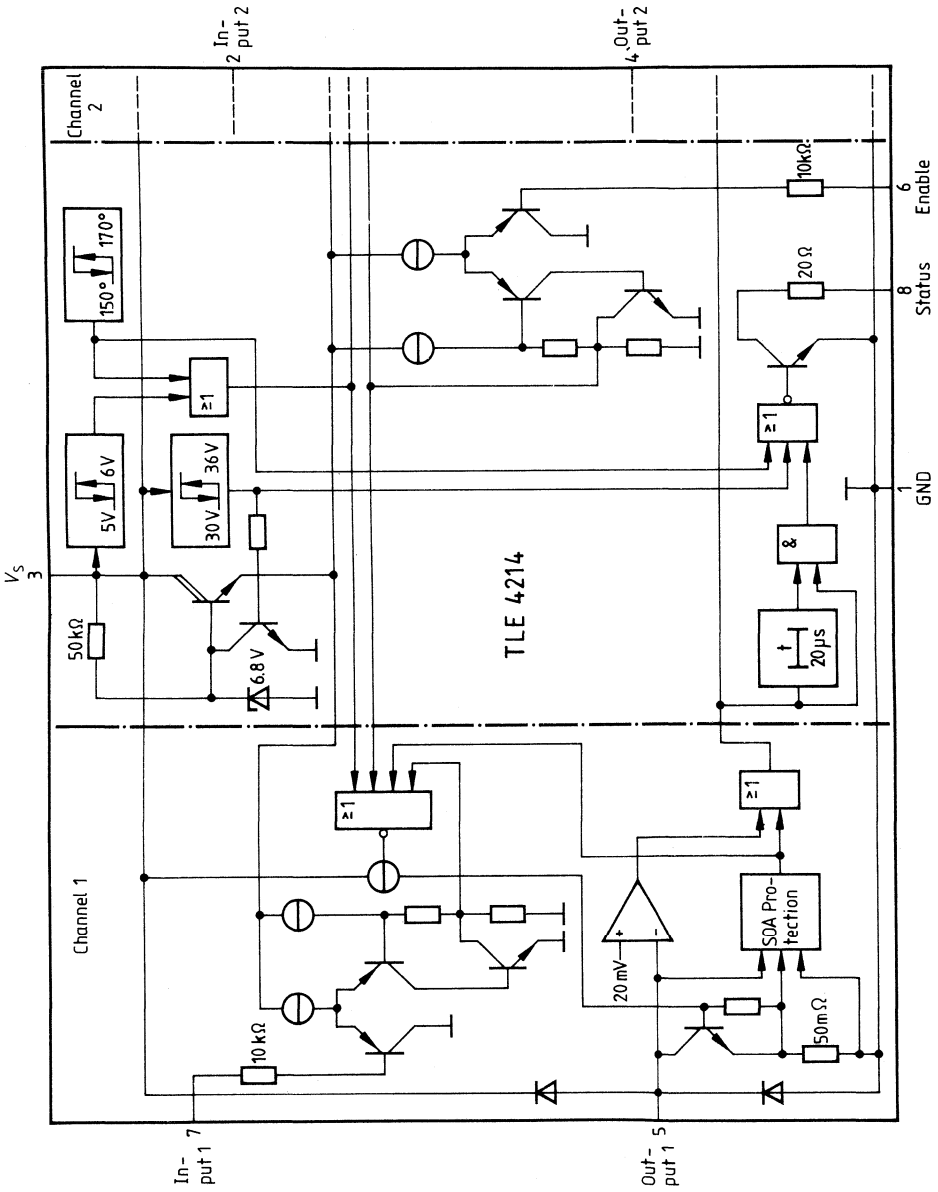
Monitoring and Protective Functions

During the activated status the outputs are monitored for underload (open circuit), overload, and short-circuit to ground (see table below). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active high). An internally determined dead time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal destruction. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no short circuit of the load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated. At supply voltages below the operating range the output stages are de-activated.

Status Output (H = Error)

	Undervoltage > 3.5 V	**Operating range** $V_I = L$ (passive)	$V_I = H$ (active)	**Overvoltage**
Standard operation	L	L	L	H
Overload	L	L	H	H
Underload	L	L	H	H
Short circuit to ground	L	H	H	H
Overtemperature	L	H	H	H

Circuit Diagram



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Absolute Maximum Ratings

$T_j = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Voltages				
Supply voltage (pin 3) $t < 0.2$ s	V_S		70	V
Supply voltage (pin 3)	V_S	−1.3	40	V
Input voltage (pin 2; pin 6; pin 7)	V_I	−5	40	V
Output voltage (pin 8)	V_O	−0.3	40	V
Output voltage (pin 4; pin 5)	V_Q	−0.3	$+V_S$	V
Currents				
Switching current (pin 4; pin 5) Internally limited	I_Q			
Current with reverse polarity (pin 4; pin 5) $t < 0.1$ s	I_Q	−0.7		A
Free-wheeling current (pin 4; pin 5)	I_Q		0.7	A
Ground current (pin 1)	I_{GND}	−1.4	2.0	A
Output current (pin 8)	I_O		10	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	125	°C
Operating Range				
Supply voltage[1])	V_S	6	25	V
Output current	I_Q	−0.5	0.5	A
Input voltage	V_I, V_F	−5	32	V
Output current	I_O	0	5	mA
Ambient temperature	T_A	−40	100	°C
Supply voltage during load short circuit	V_S		16	V
Thermal resistance system – air	$R_{th\ SA}$		91	K/W

[1]) Lower limit = 5 V, if previously V_S greater than or equal to 6 V (turn-on hysteresis)
[2]) $T_j \leq 150\,°C$

Characteristics

$V_S = 6\ V \ldots 16\ V$ (typ. $V_S = 12\ V$)
$T_j = -40\,°C \ldots 150\,°C$ (typ. $T_j = 25\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
General Characteristics						
Quiescent current	I_q		2	4	mA	$V_F < V_{FL}$
Quiescent current	I_q		35	50	mA	$V_I = V_I > V_{IH}$; $V_F > V_{FH}$
Overvoltage switching threshold	V_{SO}	30	36	40	V	$V_L = 5\ V$; $V_O > 4.5\ V$
Hysteresis of overvoltage turn-off	ΔV_{SO}	4	6	9	V	$V_L = 5\ V$; $V_O > 4.5\ V$
Underload voltage threshold	V_Q	5	20	50	mV	$V_L = 5\ V$; $V_O > 4.5\ V$
Underload current	I_{QU}	1		20	mA	$V_Q = V_{QU}$
Logic						
Control inputs						
H-switching threshold	V_{IH}	1.3	1.8	2.1	V	pin 2, 7
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	pin 2, 7
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	pin 2, 7
H-switching threshold	V_{FH}	1.6	2.1	2.7	V	pin 6
L-switching threshold	V_{FL}	1.4	1.8	2.3	V	pin 6
Hysteresis of input voltage	ΔV_F	0.1	0.3	0.7	V	pin 6
H-input current	I_{IH}	0		10	µA	$V_I = 5\ V$; pin 2, 6, 7
L-input current	$-I_{IL}$	0		10	µA	$V_I = 0.5\ V$; pin 2, 6, 7
Status Output (open collector)						
L-saturation voltage	V_{QSat}	0.1	0.2	0.4	V	$I_O = 5\ mA$
Status dead time	t_{dS}	8	20	32	µs	[1]
Switching Stages (also valid for input I' and output Q-)						
Saturation voltage	V_{QSat}		0.6	0.8	V	$I_Q = 0.5\ A$; $V_I > V_{IH}$; $V_F > V_{FH}$
Saturation voltage	V_{QSat}		45	100	mV	$I_Q = 50\ mA$; $V_I > V_{IH}$; $V_F > V_{FH}$
Output current	I_Q	0.5			A	$V_{Q\,sat} = 0.8\ V$ $V_I > V_{IH}$
Leakage current	I_Q	−5		50	µA	$V_Q = 6\ V$; $V_I < V_{IL}$
Switch-on time	$t_{D\,ON}$	0.2	0.5	5	µs	**see fig. 1;** $I_Q = 0.5\ A$
Switch-off time	$t_{D\,OFF}$	0.2	2	5	µs	**see fig. 1;** $I_Q = 0.5\ A$
Forward voltage of substrate diode	V_{QF}		1.3	1.7	V	$I_Q = -0.5\ A$ $t < 0.1\ s$
Forward voltage of Free-wheeling diode	V_{QS}		1.3	1.7	V	$I_Q = 0.5\ A$ $t < 0.1\ s$

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50% value of the status switching edge is reached.

10

Test Circuit

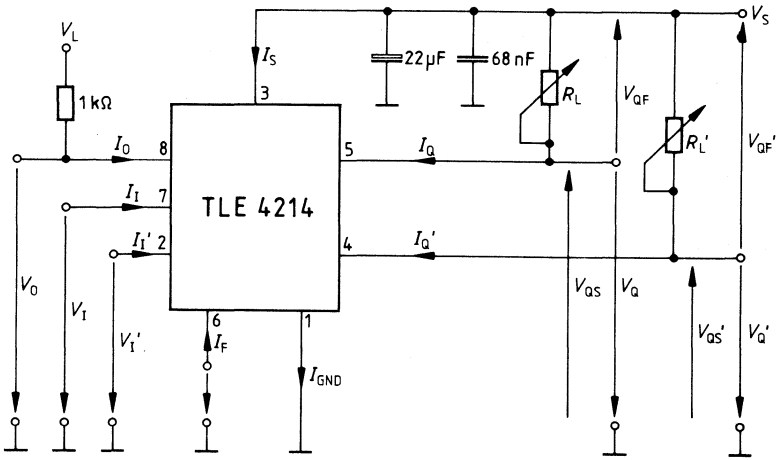
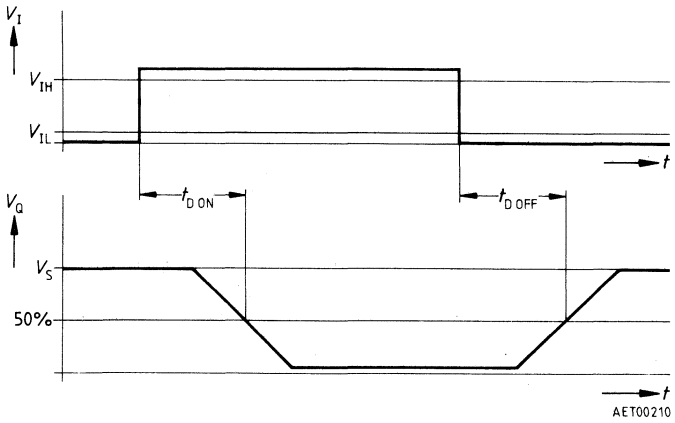
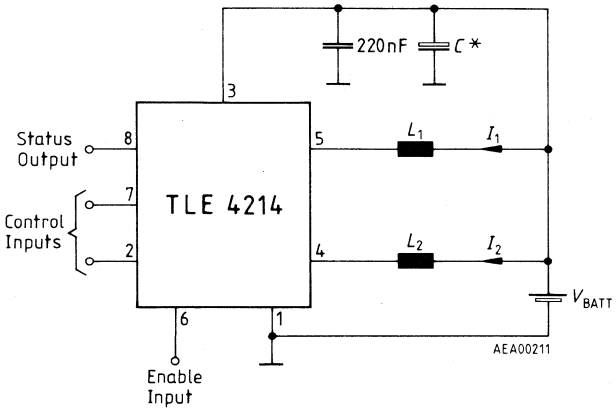


Figure 1
Timing Diagram



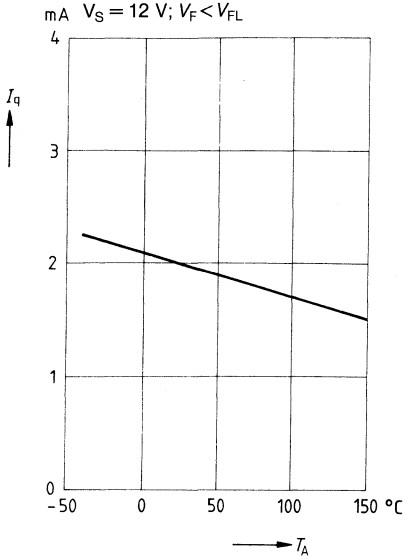
Application Circuit



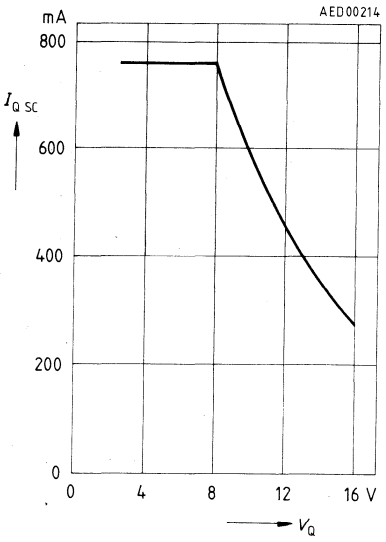
$C^* \geq (L_1 I_1^2 + L_2 I_2^2) / (70\,V - V_{BATT})^2$

Quiescent current I_q versus ambient temperature T_A in the OFF status

$V_S = 12$ V; $V_F < V_{FL}$

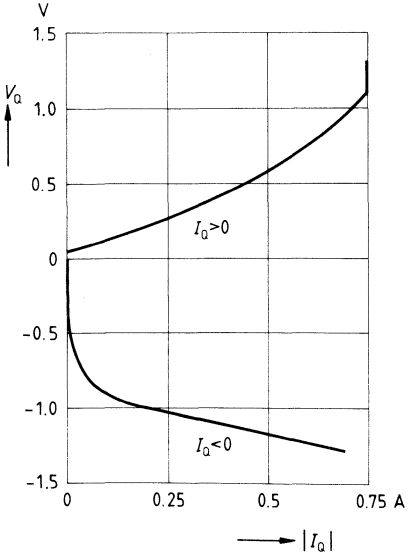


Short-circuit current I_{SC} versus output voltage V_Q



Output voltage V_Q versus output current

$V_S = 12$ V; $V_I > V_{IH}$

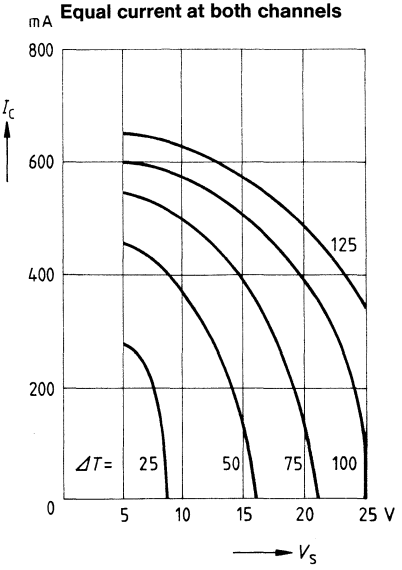


Maximum permissible output currents, being the result of the typical thermal power dissipation in a P-DIP-8 package, for three operating modes.

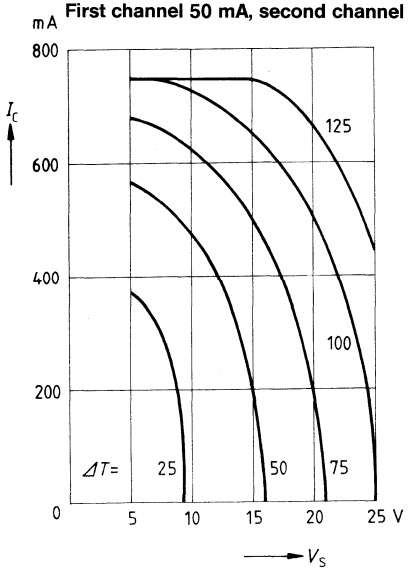
ΔT: Difference between junction and ambient temperature ($T_j - T_A$) [K].

I_C: Max. output current (steady current) per channel.

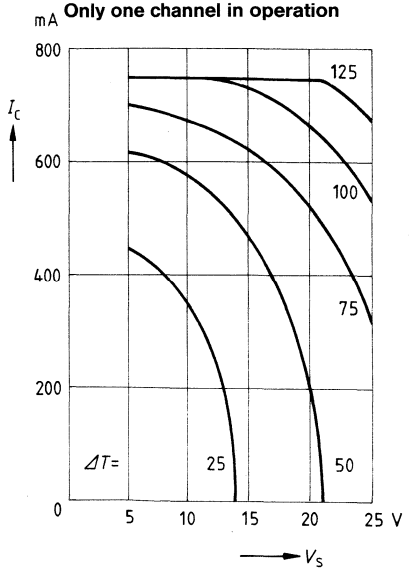
Equal current at both channels



First channel 50 mA, second channel I_C



Only one channel in operation



10

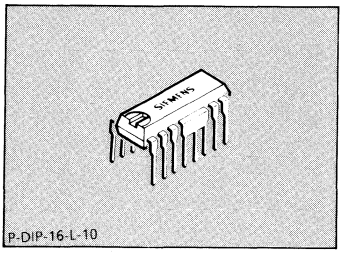
SIEMENS

Intelligent Double High-Side Switch 2 x 0.5 A — TLE 4215

Preliminary Data — **Bipolar IC**

Features

- Two high-side switches 2 x 0.5 A
- Power limiting
- Temperature monitoring
- Integrated free-wheeling diodes
- Error monitoring
- Operating voltage 5.0 to 25 V
- Maximum supply voltage 42 V, 60 V (shortterm)
- Temperature range −40 to 125 °C



Type	Ordering Code	Package
▼ TLE 4215	Q67000-A8184	P-DIP-16-L-10

▼ New type

Applications in industrial electronics call for intelligent power switches that can be activated by logic signals, which have to be short-circuit proof and which produce error feedback.

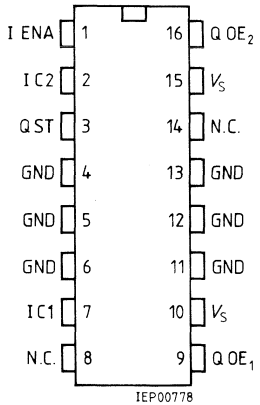
This IC incorporates two such power switches (high-side switches). On inductive loads the integrated free-wheeling diodes clamp the induction voltage.

By means of TTL signals on the control inputs (active high) the two switches can be activated independently of one another when a high level appears on the enable input. The inputs are very high-impedance and therefore may not be left open-circuit but should always be on fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions with high potential:

- Overload,
- Underload (wire break),
- Short-circuit to $+V_S$,
- Overvoltage,
- Overtemperature.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	I ENA	**Enable Input,** active high
2	IC2	**Control Input 2** activates output transistor 2 (active high)
3	QST	**Status Output** (open collector) for both output; signals overtemperature, overload, underload and shortcircuit in the load circuit as well as overvoltage on pin 10 or 15; is switched high after a defined dead time in the event of a malfunction (exeption: overvoltage)
4, 5, 6, 11, 12, 13	GND	**Ground**
7	IC 1	**Control Input 1** activates output transistor 1 (active high)
8		Not connected
9	QOE 1	**Short-Circuit Proof Open-Emitter Output 1** with free-wheeling diode to ground
10	V_S	**Supply Voltage;** large parts of the circuit are deactivated if overvoltage appears on this pin; the status output will signal this malfunction without a dead time
14	N.C.	Not connected
15	V_S	**Supply Voltage,** connected internally to pin 10; both pins should be put on $+V_S$
16	QOE 2	**Short-Circuit Proof Open-Emitter Output 2** with free-wheeling diode to ground

10

Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal into the form that is required for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with an open emitter. Each stage has its own protective circuit for limiting power dissipation, which makes the outputs short-circuit proof to ground throughout the operating range. Integrated free-wheeling diodes limit voltage spikes that occur when inductive loads are switched.

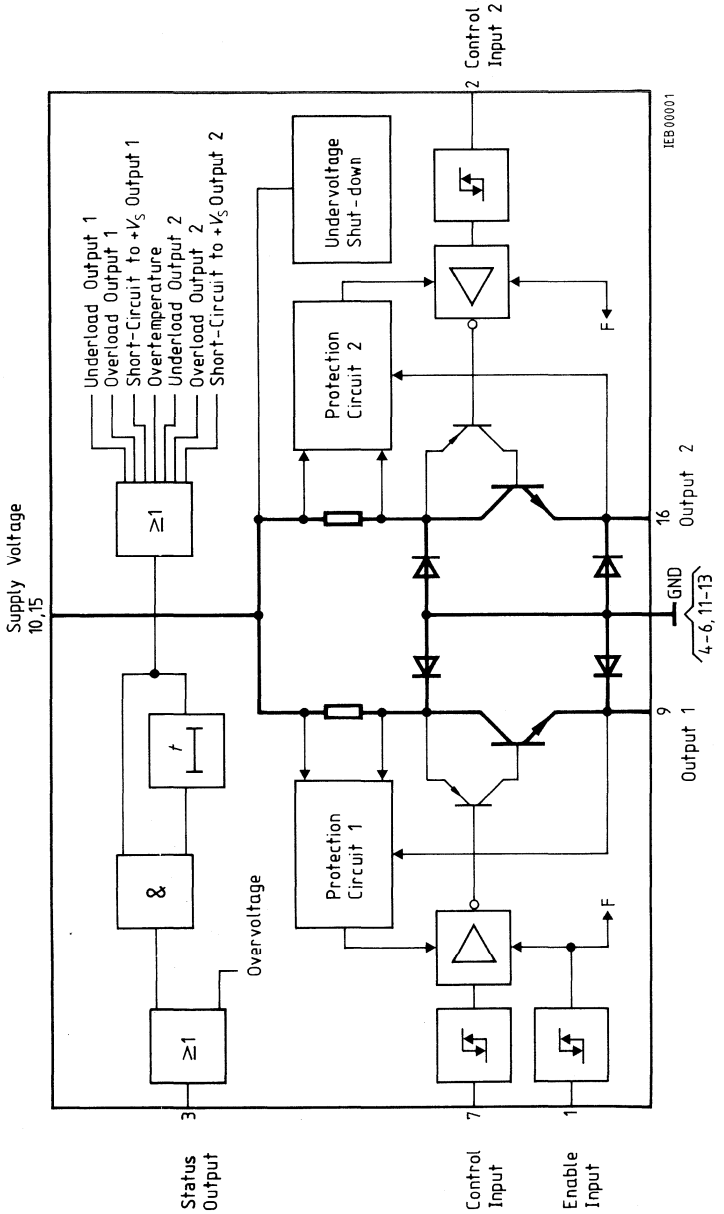
Monitoring and Protective Functions

If the supply voltage V_S is too high or there is overtemperature, several parts of the circuit are deactivated. Each output is monitored for underload (e.g. wire break) and overload while activated. Furthermore, any shorting to the supply voltage is detected. The information from these malfunctions in ORed and applied to the status output (open collector, active high). An internally defined dead time for all malfunctions, with the exception of overvoltage, prevents transient faults from being signaled.

If the minimal supply voltage for a function is not maintained, the output stages become inactive.

Status Output (H = Error)				
	Undervoltage > 3.5 V	**Operating Range** $V_I = L$ (passive)	$V_I = H$ (active)	**Overvoltage**
Normal operation	L	L	L	H
Overload	L	L	H	H
Underload	L	L	H	H
Shortcircuit to $+V_S$	L	H	H	H
Overtemperature	L	H	H	H

Block Diagram



Absolute Maximum Ratings

$T_j = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Notes
Voltages					
Supply voltage (pin 10, 15)	V_S		60	V	$t < 0.2$ sec
Supply voltage (pin 10, 15)	V_S	−0.3	42	V	
Input voltage (pin 1, 2, 7)	V_I	32	42	V	
Output voltage (pin 3)	V_O	−0.3	42	V	
Output voltage (pin 9, 16)	V_Q	−0.3	$+V_S$	V	
Currents					
Switching current (pin 9, 16)	I_Q				limited internally
Free-wheeling current (pin 9, 16)	I_Q		0.7	A	$t < 0.1$ sec
Ground current (pin 4-6, 11-13)	I_{GND}	−1.4	0.05	A	
Output current (pin 3)	I_Q		10	mA	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−50	125	°C	
Operating Range					
Supply voltage	V_S	6	25	V	[1]
Output current	I_Q	−500	500	mA	
Input voltages	V_I, V_F	−10	40	V	
Output current	I_O	0	5	mA	
Ambient temperature	T_A	−40	125	°C	$T_j \leq 150\,°C$
Thermal Resistance					
System-air	$R_{th\ SA}$		60	K/W	
System-case (pin 5)	$R_{th\ SC}$		15	K/W	

[1] Lower limit = 5.2 V if V_S was previously ≥ 6 V (turnon hysteresis)

Characteristics

$V_S = 6...16$ V; $T_j = -40...150$ °C; unless otherwise specified in accordance with test circuit 1

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
General Data						
Quiescent current	I_q		2	5	mA	$V_E < V_{EL}$
Quiescent current	I_q		10	20	mA	$V_I = V_I > V_{IH}$; $V_E > V_{EH}$
Overvoltage switching threshold	V_{Sov}	30	36	40	V	$V_L = 5$ V; $V_O > 4.5$ V
Hysteresis of overvoltage turnoff	ΔV_{Sov}	3	6	9	V	$V_L = 5$ V; $V_O > 4.5$ V
Underload voltage switching threshold	V_{Qu}		200		mV	$V_L = 5$ V; $V_O > 4.5$ V
Underload current	I_{Qu}	0.5		5	mA	$V_Q = V_{Qu}$
Logic						
Control inputs						
H-switching threshold	V_{IH}	1.2	1.8	2.2	V	pin 2, 7
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	pin 2, 7
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	pin 2, 7
H-switching threshold	V_{EH}	1.7	2.1	2.8	V	pin 1
L-switching threshold	V_{EL}	1.4	1.8	2.3	V	pin 1
Hysteresis of input voltage	ΔV_E	0.1	0.3	0.7	V	pin 1
H-input current	I_{IH}			10	µA	$V_I = 5$ V; pin 1, 2, 7
L-input current	$-I_{IL}$			10	µA	$V_I = 0.5$ V; pin 1, 2, 7
Status Output (open collector)						
L-saturation voltage	V_{OSat}	0.1	0.2	0.4	V	$I_O = 5$ mA
Status dead time	t_{DS}	8	25	40	µs	1)
Switching Stages (also applies to input and output Q')						
Saturation voltage	V_{Lsat}	0.9	1.2	1.5	V	$I_Q = 0.5$ A; $V_I > V_{IH}$; $V_E > V_{EH}$
Leakage current	I_{QL}			75	µA	2) $V_I > V_{IL}$; $V_S = 6$ V
Turn-on time	t_{Don}	0.2	0.5	5	µs	**see fig. 1;** $I_Q = 0.5$ A
Turn-off time	t_{Doff}	0.2	1	5	µs	**see fig. 1;** $I_Q = 0.5$ A
Forward voltage of free-wheeling diode	$-V_Q$	0.8	1.3	1.7	V	$I_Q = 0.5$ A $t < 0.1$ sec

1) Time from beginning of malfunction on channel (exception: overvoltage) until 50% value of status switching edge
2) $V_Q = 0$ V

Test Circuit 1

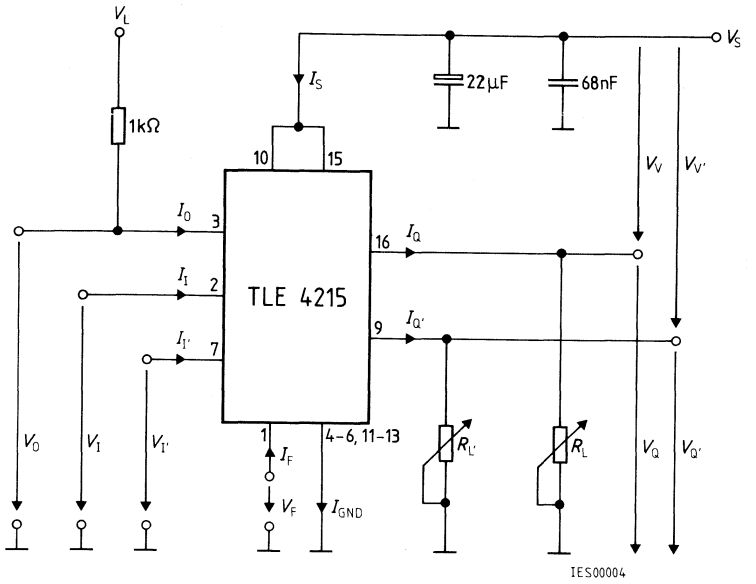
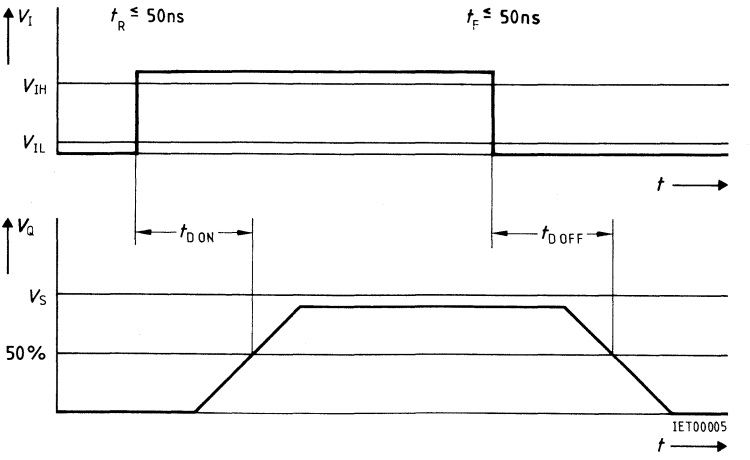
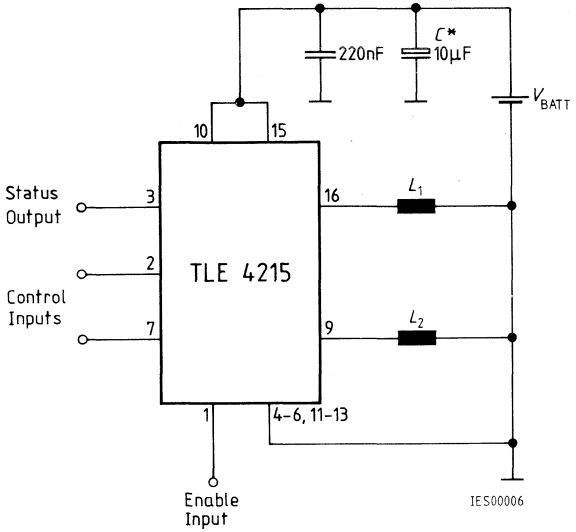


Figure 1
Timing Diagram



Application Circuit



C* is to be dimensioned such that in case of an incoming-line failure the maximum ratings are not exceeded by the recirculation energy of L_1, L_2.

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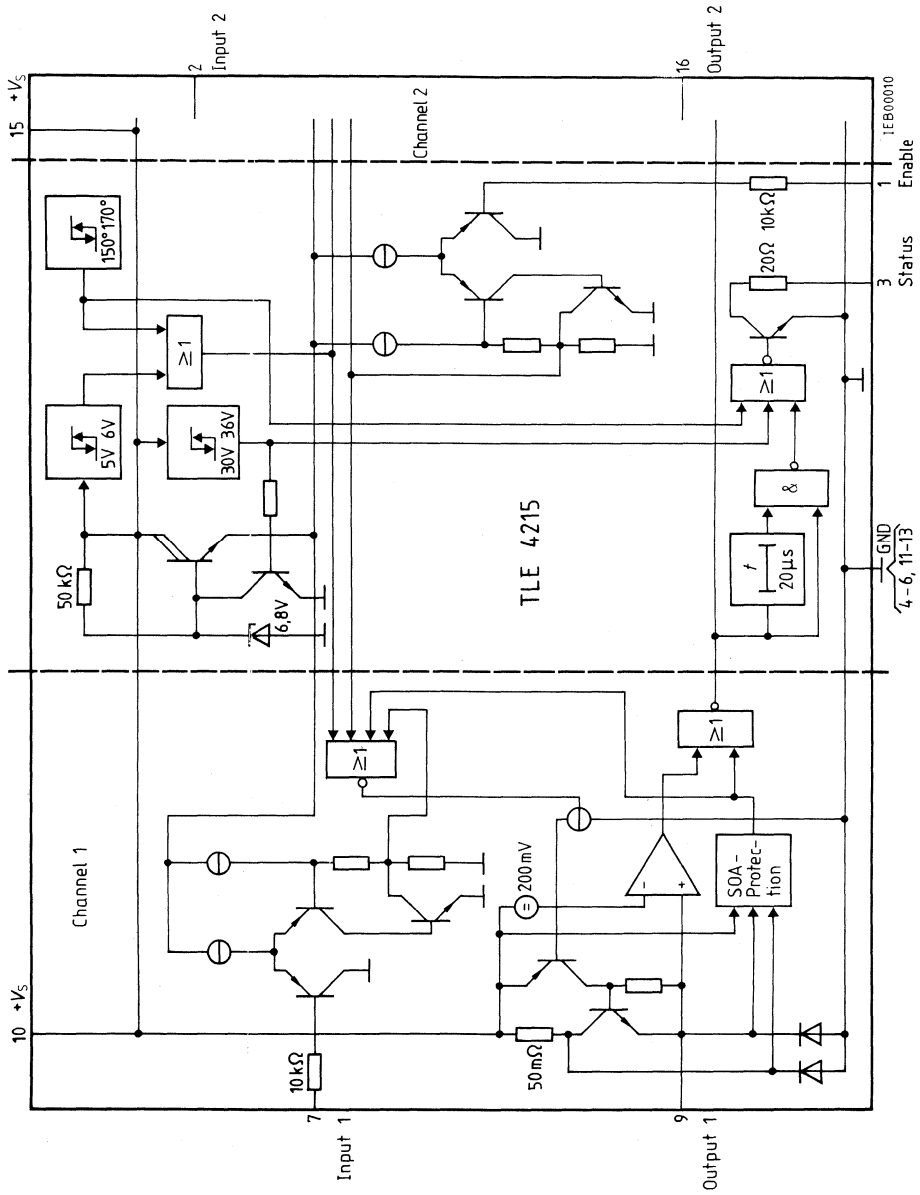
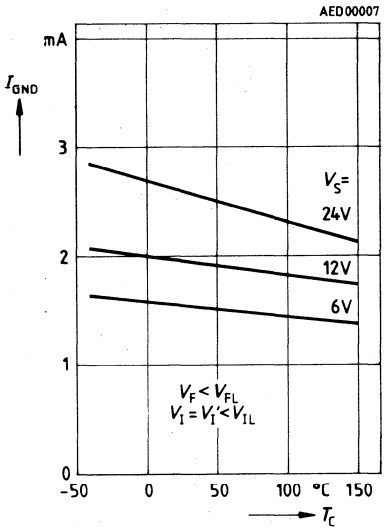
Circuit Diagram

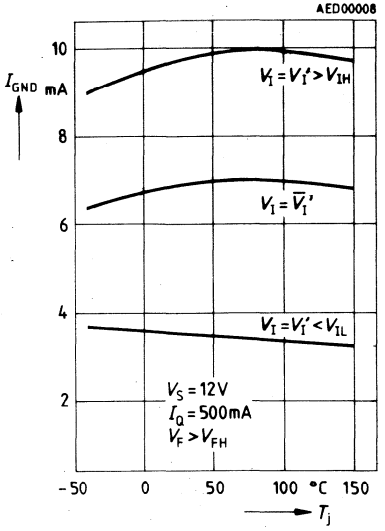


Diagrams

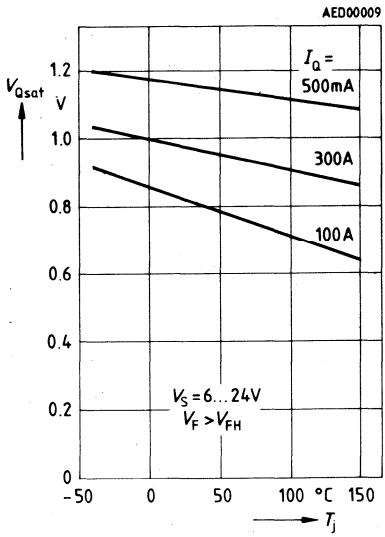
Typ. quiescent current I_{GND} versus I_C in the off-state



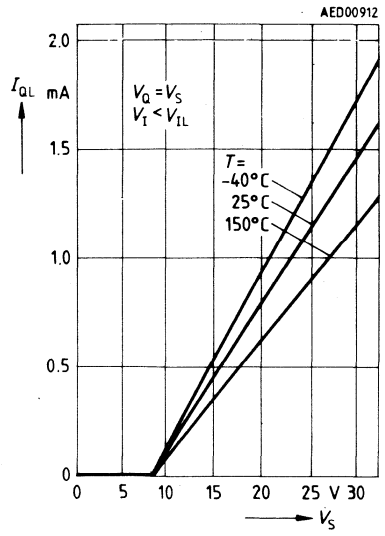
Typ. quiescent current I_{GND} versus chip temperature T_j in the on-state



Typ. output saturation voltage V_{Qsat} versus chip temperature T_j



Typ. output leakage current I_{QL} versus supply voltage V_S



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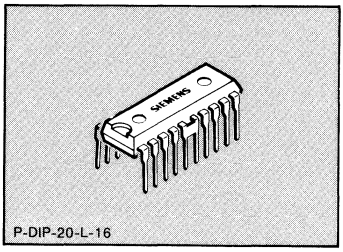
SIEMENS

Intelligent Sixfold Low-Side Switch

TLE 4216

Preliminary Data

Bipolar-IC



Features

- Quad 50 mA outputs
- Dual 500 mA outputs
- Output stages with power limiting
- Open-collector outputs
- Shortcircuit-proof over operating range
- Z-diodes to ground
- Status signalling
- TTL-compatible control inputs
- Temperature monitoring
- Wide temperature range $-40\,°C \leq T_j \leq 150\,°C$

Type	Ordering Code	Package
▼ TLE 4216	Q67000-A8237	P-DIP-20-L-16

▼ New type

TLE 4216 is an integrated, sixfold low-side power switch with power limiting of the 0.5 A outputs, shortcircuit protection of the 50 mA switches and Z-diodes on all switches from output to ground. TLE 4216 is particularly suitable for automotive and industrial applications.

Application Description

Applications in industrial electronics call for intelligent power switches that can be activated by logic signals, which have to be shortcircuit-proof and which produce error feedback.

This IC incorporates six power switches connected to ground (low-side switch) possessing the features described above. On inductive loads the integrated Z-diodes clamp the self-induction voltage.

By means of TTL signals on the control inputs (active high) all six switches can be activated independently of one another when a high level ($V_{IP} > 2.1$ V) appears on the preferred-state input. When there is a low level on the preferred-state input, switches 1 to 4 are switched through, Q5 and Q6 are inactive regardless of the input level. The inputs are very high-impedance and therefore must not be left open-circuit but should always be on fixed potential (noise immunity).

The status output signals the following malfunctions by analog voltage levels:

- Overload
- Overtemperature

Possible Input and Output Levels

Supply Voltage V_S	**V**	$I_1 \ldots I_6$	$Q_1 \ldots Q_4$	Q_5, Q_6
2 to 30 V	L	X	L	H
4 to 30 V	H	L	H	H
4 to 30 V	H	H	L	L

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Circuit Description

Input Circuits

The control inputs and the preferred-state input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal into the form that is required for driving the NPN power transistors.

Switching Stages

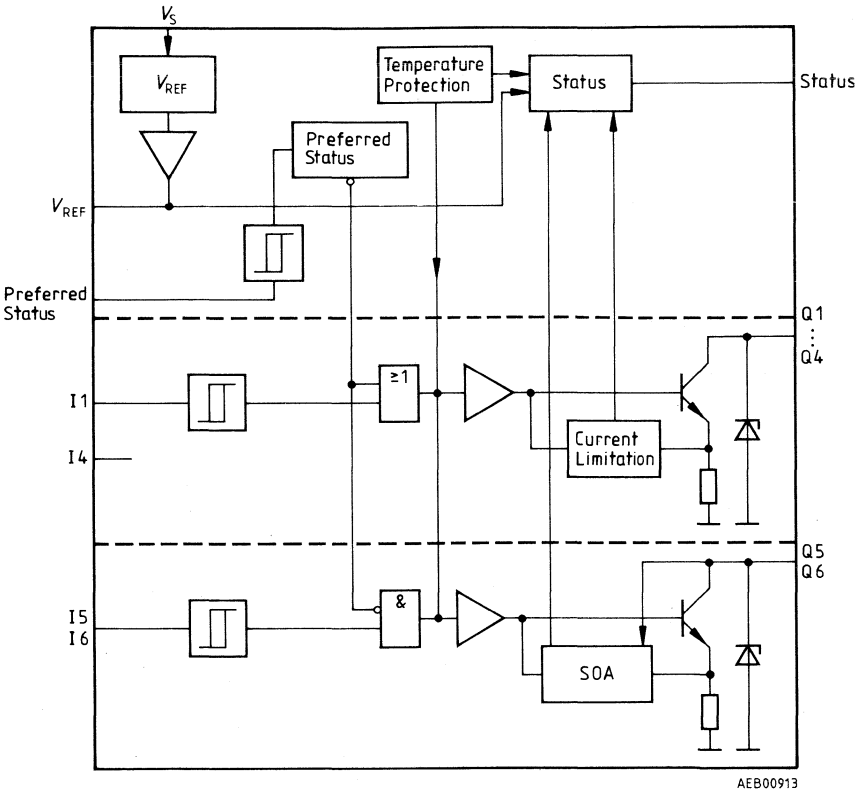
The output stages consist of NPN power transistors with open collectors. Each stage has its own protective circuit for limiting power dissipation and shortcircuit current, which makes the outputs shortcircuit-proof to the supply voltage throughout the operating range. Integrated Z-diodes limit positive voltage spikes that occur when inductive loads are switched.

Monitoring and Protective Functions

Each output is monitored in its activated status for overload. Furthermore, large parts of the circuitry are blocked (Control, Output stages). The information from these malfunctions is ORed and applied to the status output. If several malfunctions appear simultaneously, the highest voltage level will dominate. The IC is also protected against thermal overload. If a chip temperature of typically 160 °C is reached, overtemperature is signalled on the status output. If the temperature continues to increase, all outputs are turned off at 170 °C.

If the minimum supply voltage for functioning is not maintained, the output stages become inactive. At a supply voltage of higher than 2 to 4 V, the outputs are switched to a preferred state regardless of the level on pin 12. If the preferred state is to be maintained beyond this range, pin 12 must be switched to low potential. Above a supply voltage of typical 3 V (max. 4 V) the preferred state is controlled by pin 12. From 4 to 5.2 V the logic operation of the outputs is guaranteed, but the status output cannot be evaluated. At a supply voltage of 5.2 to 30 V the full function is guaranteed.

Block Diagram



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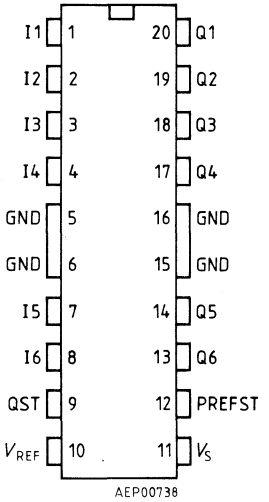
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1, 2, 3, 4	I1, I2, I3, I4	Inputs of 50-mA switches 1, 2, 3, 4
5, 6	GND	Ground, cooling
7, 8	I5, I6	Inputs of 0.5 A switches 5, 6
9	Q_{ST}	Status analog output
10	V_{REF}	Reference voltage; a higher reference voltage than the internal one can be applied from the exterior as a voltage reference for the status output (A/D converter).
11	V_S	Supply voltage
12	PREFST	Preferred state (Low = preferred state of all outputs regardless of inputs)
13, 14	Q6, Q5	Output switch 6 (0.5 A), open collec. and output switch 5 (0.5 A)
15, 16	GND	Ground, cooling
17, 18, 19, 20	Q4, Q3, Q2, Q1	Outputs 4, 3, 2, 1 (50 mA)
19	Q2	Output 2 (50 mA)

Absolute Maximum Ratings

Maximum ratings for junction temperature T_j from −40 to 150 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Voltages					
Supply voltage	V_S	−1	40	V	
Supply voltage load circuit	$V_{Q1\text{-}6}$	−0.7	25	V	
Input voltage	$V_{I1\text{-}6}$, V_{REF}	0	V_S	V	
Input voltage	$V_{REF\ ext}$	−0.7	7	V	
Currents					
Switching current	I_{Q1}-I_{Q6}				limited internally
Current on reverse poling in load circuit	$I_{Q5,\ Q6}$	−0.5		A	
Current on reverse poling in load circuit	$I_{Q1\text{-}Q4}$	−50		mA	
Free-wheeling current	$I_{Z5\text{-}Z6}$		0.7	A	
Free-wheeling current	$I_{Z1\text{-}Z4}$		70	mA	
Junction temperature	T_j	−40	150	°C	Temp. protection cuts out at 170 °C
Storage temperature	T_{stg}	−50	125	°C	

Operating Range

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Supply voltage	V_S	5.2	30	V	$V_{REF} \leq V_S$, for V_{REF} = 5 V functioning is guaranteed at V_S = 4-5.2 V but status output cannot be evaluated.
Voltage in load circuit		0.3	24	V	
Ambient temperature	T_A	−40	110	°C	
Supply voltage for load shortcircuit	V_S		16	V	
Input current (high)	I_{IH}		100	µA	

Thermal Resistance

System-case (pin 5, 6, 15, 16)	R_{thSC}		15	K/W	
System-air	R_{thSA}		55	K/W	

Characteristics

$V_S = 12$ V (unless stated otherwise); $T_j = -25$ to 140 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
General						
Current consumption	I_S		50		mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$
Current consumption	I_S		36		mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$; $V_S = 5$ V
Standby current	I_S		8		mA	$V_I < V_{IL}$; $V_{IP} > V_{IH}$
Logic						
Control inputs + preferred state						
H-switching threshold	V_{IH}		1.8		V	pin 1, 2, 3, 4, 7, 8, 12
L-switching threshold	V_{IL}		1.2		V	pin 1, 2, 3, 4, 7, 8, 12
Hysteresis	ΔV_I		0.6		V	pin 1, 2, 3, 4, 7, 8, 12
Input current						
H-input current	I_{IH}	0		20	µA	$V_I < 6$ V
L-input current	$-I_{IL}$	0		20	µA	0.5 V $< V_I <$ 6 V
Switching Stages						
Load current	$I_{Q1\text{-}Q4}$		50		mA	$V_S = 2$ V (preferred state)
Saturation voltage	$V_{Qsat\ 5,6}$		0.5		V	$I_Q = 0.4$ A; $V_I > V_{IH}$
Saturation voltage	$V_{Qsat\ 1\text{-}4}$		0.4		V	$I_Q = 50$ mA: $V_I > V_{IH}$
Saturation voltage	$V_{Qsat\ 1\text{-}4}$			0.22	V	$I_Q = 20$ mA: $V_I > V_{IH}$
Turnon time	t_{Don}		1		µs	see diagrams
Turnoff time	t_{Doff}		1		µs	see diagrams; $I_L = I_{max}$
Temperature Protection						
Overtemperature (signalled on status output)			160		°C	
Overtemperature (turnoff of outputs)			170		°C	

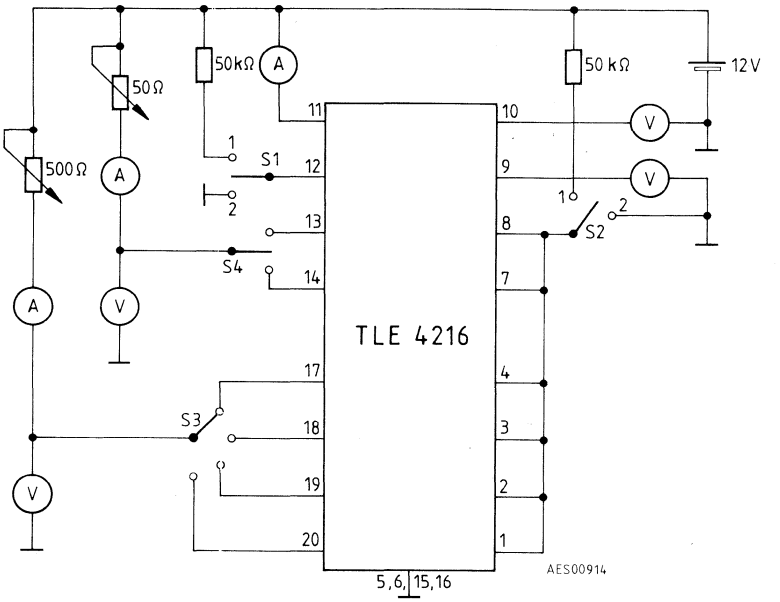
Characteristics

$V_S = 12$ V (unless stated otherwise); $T_j = -25$ to 140 °C)

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Outputs						
Free-wheeling voltage	V_{Q1}-V_{Q4}	25.5		33	V	$I = 50$ mA
Free-wheeling voltage	V_{Q5}-V_{Q6}	25.5		33	V	$I = 0.5$ A
Shortcircuit current	I_{Q1max}-I_{Q4max}	50			mA	$V_Q < 16$ V
Shortcircuit current	I_{Q5max}-I_{Q6max}					**see diagrams**
Status output						
No fault	V_{st}			0.5	V	$V_{REF} = 5$ V[1]
Overload output 6	V_{st}	1.0		1.3	V	$V_{REF} = 5$ V[1]
Overload output 5	V_{st}	1.4		1.7	V	$V_{REF} = 5$ V[1]
Overload output 4	V_{st}	1.8		2.1	V	$V_{REF} = 5$ V[1]
Overload output 3	V_{st}	2.2		2.5	V	$V_{REF} = 5$ V[1]
Overload output 2	V_{st}	2.6		2.9	V	$V_{REF} = 5$ V[1]
Overload output 1	V_{st}	3.0		3.3	V	$V_{REF} = 5$ V[1]
Overtemperature	V_{st}	3.5			V	$V_{REF} = 5$ V[1]
Source resistance of status output	R_{QSt}		250		Ω	
Delay time of status	t_{dst}		10		µs	Short circuit of load
Reference voltage (internal)	V_{REF}		2.5		V	
Input resistance of reference pin	$R_{REF\ in}$	8	10	14.5	Ω	$V_{REF} = 2.6 - 6.5$ V

[1]) The limits shift proportionally for a different value of reference voltage.

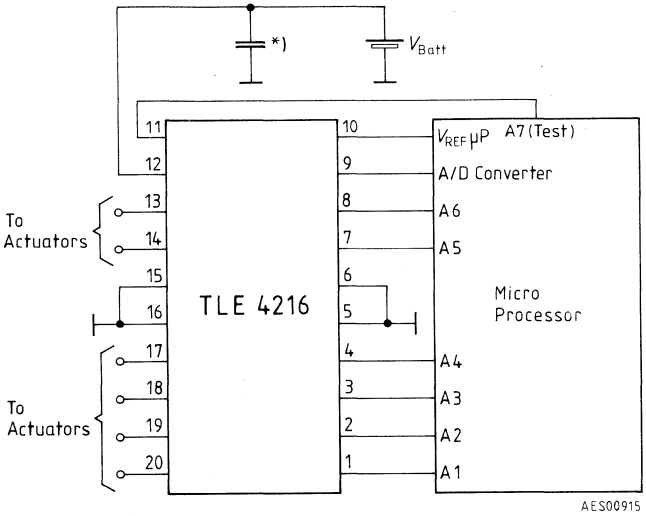
Test Circuit



S1 in position 1: all switches can be activated by S2 (position 1) or deactivated (position 2)

S1 in position 2: preferred state

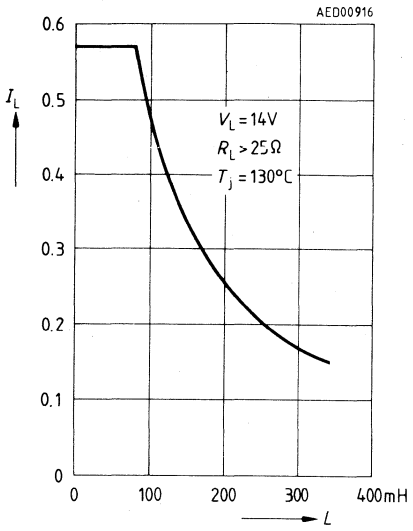
Application Circuit



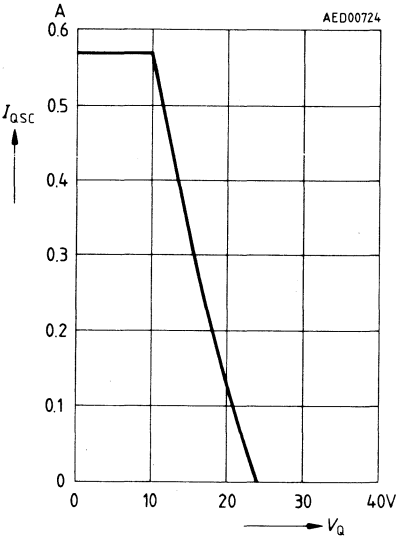
*) The capacitance depends on the inductance and current load of the supply.

Diagrams

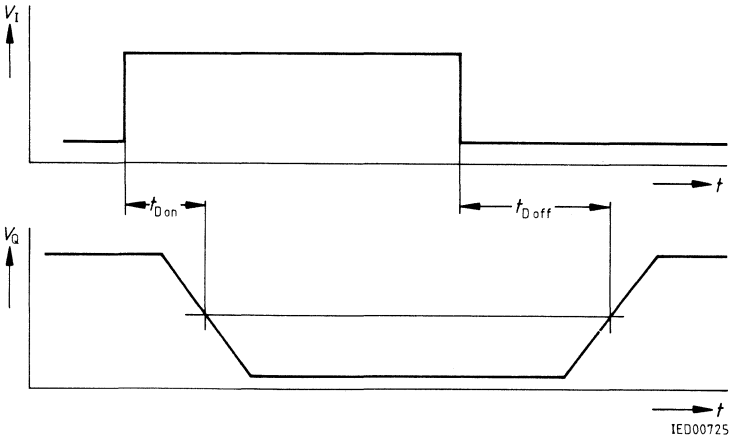
Permissible load inductance versus load current



Shortcircuit current I_{QSC} versus output voltage V_Q (0.5 A outputs)



When switching the maximum inductive loads, the maximum temperature T_j of 150 °C may be briefly exceeded. The IC will not destroyed by this, but the restrictions concerning useful life should be observed.



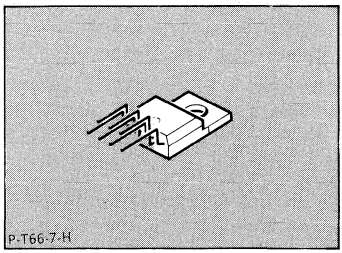
SIEMENS

4 A Low-Side Switch with Fault Diagnostics — TLE 4220

Preliminary Data — **Bipolar-IC**

Features

- Maximum load current 4 A
- Low saturation voltage (typical 0.8 V)
- Status signalling
- Load dump protection 65 V (V_S and V_Q)
- Reverse-polarity protection (V_S and V_Q)
- Z-diode clamping
- Temperature monitoring
- Power limiting
- Wide temperature range: $-40\,°C \leq T_j \leq 150\,°C$



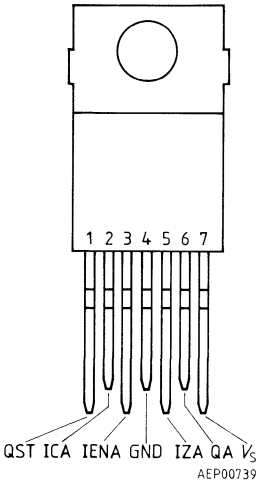
Type	Ordering Code	Package
▼TLE 4220	Q67000-A9010	P-T66-7H

▼ New type

TLE 4220 is an integrated low-side power switch with reverse-polarity protection, power limiting, temperature monitoring, fault signalling via a status output and an integrated Z-diode for output clamping. TLE 4220 is designed for automotive applications.

10

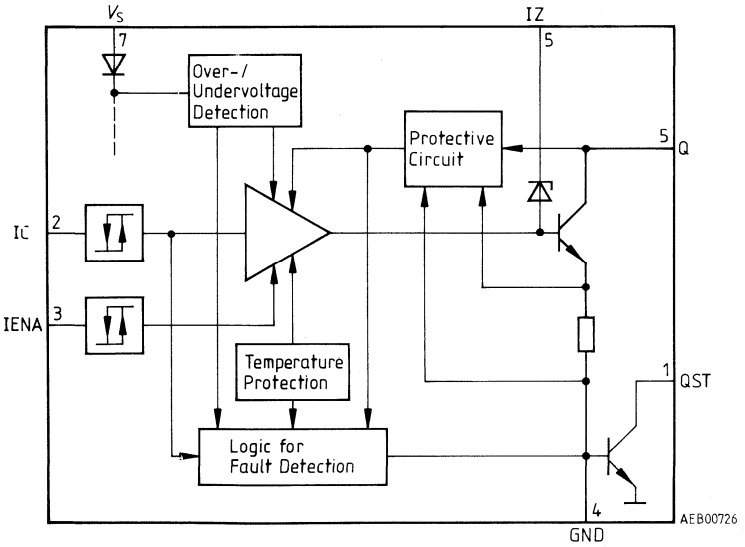
Pin Configuration



Pin Definitions and Functions

Pin	Symbol	Function
1	QST	**Status output** (open collector) for fault signalling; shortcircuit-proof to $V_{ST} \leq 6.25$ V
2	IC	**Control input,** activ high.
3	IENA	**Enable input,** activ high.
4	GND	**Ground,** connected internally to cooling lug.
5	IZ	**Z-diode;** if this pin is not connected to pin 6, appropriate provisions have to be taken for protecting the power output against the self-induced EMF when inductive loads are turned off.
6	Q	**Power output** (open collector) for inductive loads; shortcircuit-proof.
7	V_S	**Supply voltage;** if there is over-voltage on this pin, the major part of the circuitry is deactivated.

Block Diagram



Application Description:
This IC is specially designed to drive inductive loads (relays, electromagnetic valves). An integrated Z-diode limits during switch off the self-induced EMF when pin 5 is connected to pin 6. It is also possible to implement this limiting through external-measures (free-wheeling diode, Z-diode).
For the detection of faults there is a status output, which signals the following faults by logic level:

- Overvoltage or undervoltage on $+V_S$,
- Overvoltage in the load circuit,
- Load interruption or shortcircuit to ground with activated and inactivated switch,
- Overloading of output (also shortcircuit to $+V_S$) with switch activated.

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of Schmitt triggers with hysteresis. The control signal activates the buffer amplifier for the output stage when there is high potential on the enable input.

Switching Stages

The power output consists of a NPN power transistor with open collector. A protective circuit for limiting power dissipation makes the output stage shortcircuit-proof throughout the operating range. The integrated Z-diode can be connected externally to the output and in this way limits voltage spikes produced when inductive loads are turned off.

Protective Circuits

At supply voltages that are above or below the operating range, the output stage is turned off independently of the input signals. An integrated diode protects against reverse poling of the operating voltage. The load circuit is also protected against reverse poling within the bounds of the maximum ratings (no load shortcircuit permissible at the same time). There is temperature protection to guard the IC against thermal overload.

Fault Detection

The status output signals overvoltage or undervoltage on $+V_S$ as well as overtemperature and, with the enable input activated, faults on the output (overload, underload, overvoltage) by the logic connectives given in the table

Supply voltage	Control input	Output state	Status output
Overvoltage	X	X	H
Undervoltage	X	X	H
Operating range	L	No fault	L
Operating range	H	No fault	H
Operating range	L	Fault or overtemperature	H
Operating range	H	Fault or overtemperature	L

x = random

Because of the internal propagation delays, the correct status information is output with a delay of up to 50 µs Therefore a corresponding wait interval is necessary before precise evaluation of the status signal can commerce.

Absolute Maximum Ratings

Maximum ratings for case temperature T_C from −40 to 125 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Voltages					
Supply voltage	V_S	−45	45	V	
Supply voltage	V_S		65	V	$t \leq 500$ ms
Output voltage	V_Q		45	V	
Output voltage	V_Q		70	V	$t \leq 500$ ms
Output voltage	V_{ST}	−0.3	45	V	
Input voltage	V_I	−45	45	V	
Input voltage	V_F	−45	45	V	
Currents					
Z current	I_Z	−1	1	mA	pin 5 not connected to pin 6
Switching current	I_Q	limited internally; for driving via Z diode only inductive off-commutating current is permissible			
Current on reverse poling	I_Q; I_{GND}	−4		A	
Output current, status pin	I_{ST}	−1		mA	
Output current, status pin	I_{ST}		1	mA	$V_{ST} \geq 6.25$ V
Breaking energy on inductive load	E		200	mJ	
Junction temperature	T_j	−40	150	°C	
Storage temperature	T_{stg}	−50	150	°C	

Operating Range

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Remarks
Supply voltage	V_S	6.5	18	V	
Rate of supply voltage rise	dV_s/dt	−1	1	V/µs	
Input voltages	V_I, V_F	−5	40	V	
Output voltage	V_{ST}		40	V	
Output current	I_{ST}	0	1	mA	
Case temperature	T_C	−40	110	°C	$T_j \leq 150$ °C
Response threshold of temperature protection		150		°C	165 °C typical

Thermal Resistance

System-case	R_{thSC}		3	K/W	
System-air	R_{thSA}		65	K/W	

Characteristics

V_S = 6.5 to 18 V (typ. 12 V)
T_C = −40 to 110 °C; $T_j \leq 150$ °C (typ. 25 °C)
V_D = 5.1 V

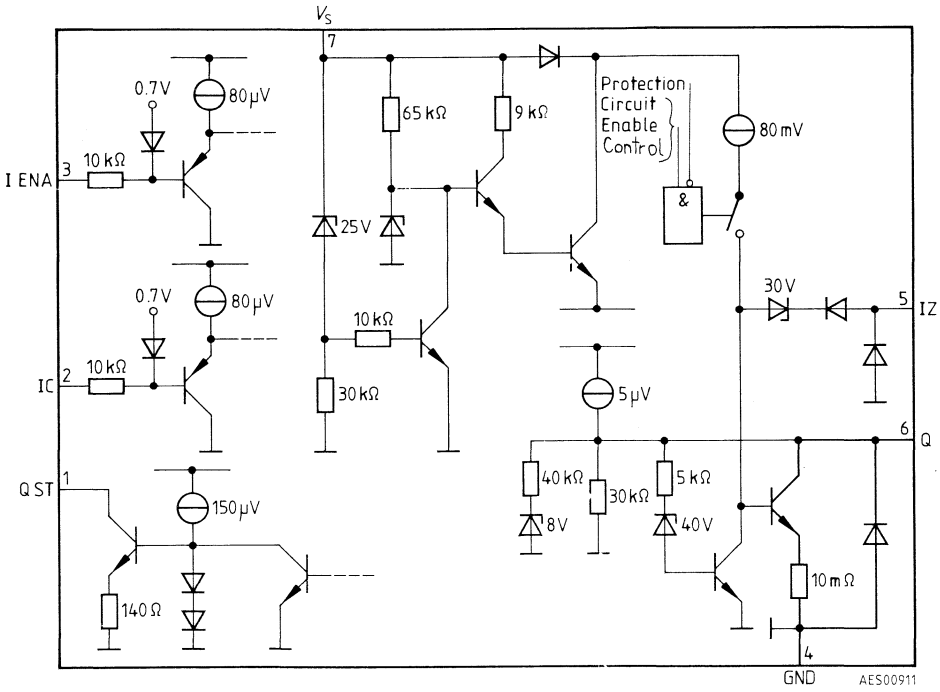
Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Standby current	I_S			10	mA	$V_I < V_{IL}$ or $V_F < V_{FL}$
Current consumption	I_S		100	180	mA	$V_I > V_{IH}$ and $V_F > V_{FH}$
Overvoltage switching threshold	V_{Sov}	18		28	V	$V_I < V_{IL}$; $V_{ST} > 5$ V
Overvoltage switching threshold	V_{Qov}	34		44	V	$V_I < V_{IL}$; $V_{ST} > 5$ V
Differential voltage	ΔV_{QZ}	4			V	V_{Qov}-V_Z
Underload current	I_{Qun}			450	mA	$V_I > V_{IH}$; $V_F > V_{FH}$; $V_{ST} < 0.5$ V
Underload voltage switching threshold	V_{Qun}		2.4		V	$V_I < V_{IL}$; $V_F > V_{FH}$; $V_{ST} > 5$ V
Overload switching threshold	V_{QL}	1.5		2.5	V	$V_I > V_{IH}$; $V_F > V_{FH}$; $V_{ST} < 0.5$ V

Characteristics

V_S = 6.5 to 18 V (typ. 12 V)
T_C = −40 to 110 °C; $T_j \leq 150$ °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Control Input						
H-input voltage	V_{IH}	2.0			V	
L-input voltage	V_{IL}			1.0	V	
Hysteresis	ΔV_I		0.5		V	
H-input current	I_{IH}	0		10	µA	V_I = 5 V
L-input current	$-I_{IL}$	0		10	µA	V_I = 0.5 V
Enable Input						
H-input voltage	V_{FH}	2.4			V	
L-input voltage	V_{FL}			1.6	V	
Hysteresis	ΔV_F		0.4		V	
H-input current	I_{FH}	0		10	µA	V_F = 5 V
L-input current	$-I_{FL}$	0		10	µA	V_F = 0.5 V
Status Output						
Low voltage level	V_{ST}			0.5	V	I_{ST} = 1 mA; V_D variable
Low voltage level	V_{ST}			0.3	V	I_{ST} = 125 µA; V_D variable
High reverse current	I_{ST}			2	µA	V_S = 0 V
Propagation delay	t_{ST}			50	µs	*)
Switching Stages						
Saturation voltage	V_{QSat}			1.25	V	I_Q = 4 A; $T_j \leq 125$ °C
Saturation voltage	V_{QSat}			1.25	V	I_Q = 3 A **see diagram 3**
Overload current	I_{QL}					**see SOA diagram**
Reverse current	I_{QR}			100	µA	$V_I < V_{IL}$; V_S = 6 V
Turn-on time	t_{dOn}			5	µs	**see fig. 1;** I_Q = 2 A
Turn-off time	t_{dOff}			10	µs	**see fig. 1;** I_Q = 2 A
Forward voltage substrate diode	$-V_{QF}$			2	V	I_Q = −4 A
Z Diode						
Z voltage	V_Z		30		V	I_Z = 0.1 A; $V_Z = V_Q$
Internal resistance	r_Z		0.7		Ω	0 A < I_Q < 4 A; $V_Z = V_Q$

Circuit Diagram



10

Test Circuit

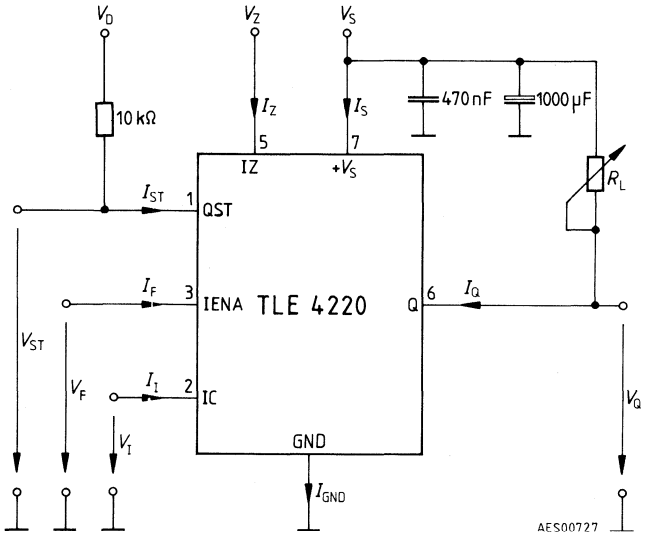
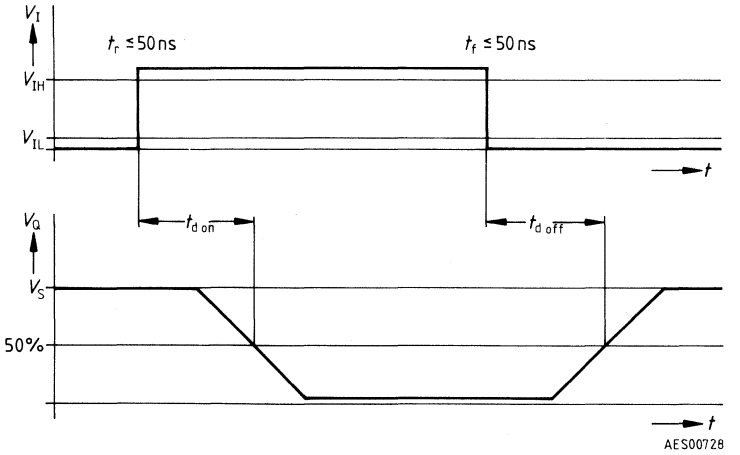
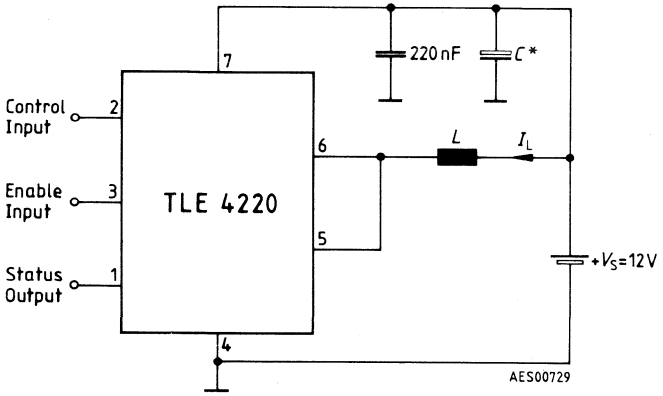


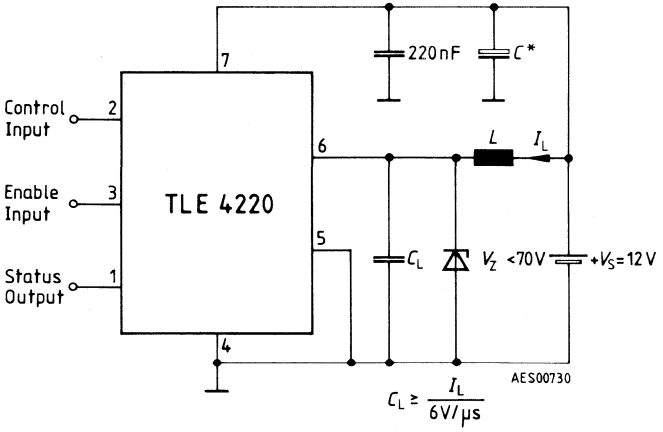
Figure 1
Timing Diagram



Application Circuit 1



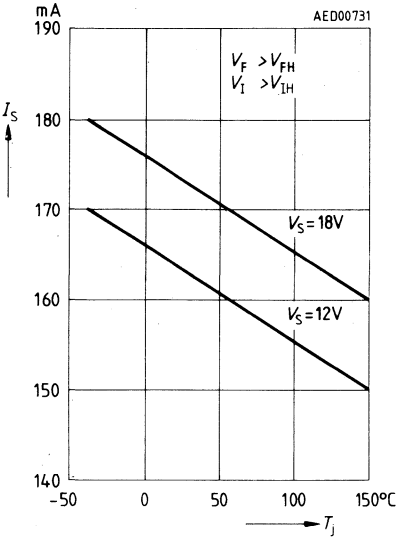
Application Circuit 2



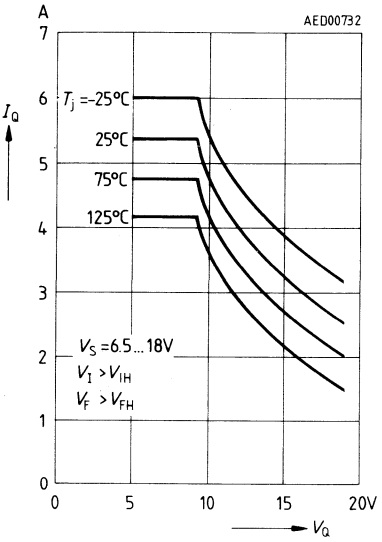
The blocking capacitor C* is to be rated large enough so that the maximum ratings of the IC for negative supply voltage are not exceeded during the off-commutating operation in interruption of the battery voltage.

Diagrams

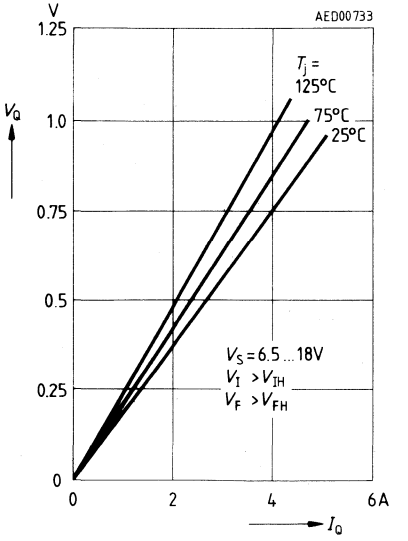
Maximum standby current I_S versus junction temp. T_j in active state



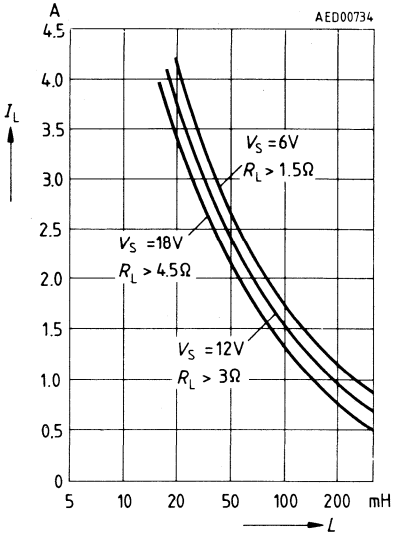
Shortcircuit current I_Q versus output voltage V_Q



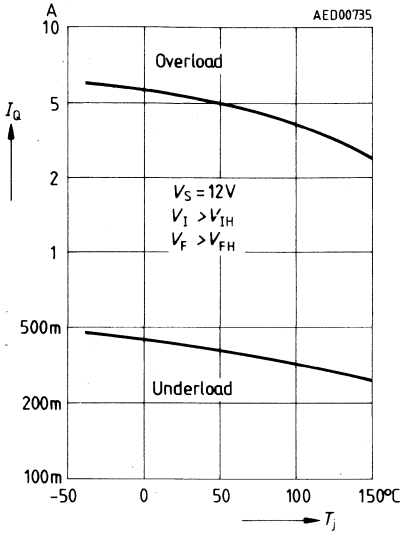
Typical output voltage V_Q versus output current I_Q



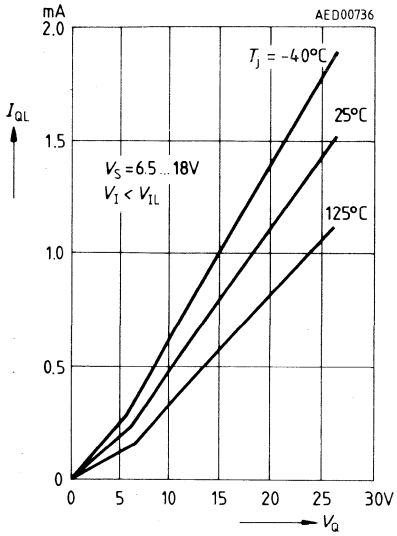
Maximum load current I_L versus load inductance L



Response threshold of status signal versus junction temperature T_j

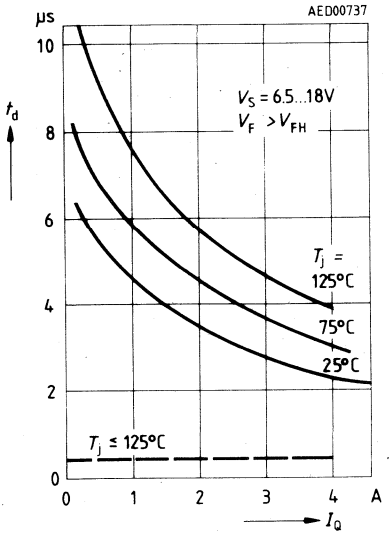


Typical output leakage current I_{QL} versus output voltage V_Q



Typical switching times versus output current I_Q

t_{dOn}: ——— t_{dOff} - - - -



10

ICs für Sensoranwendungen, Hall-IC, Näherungsschalter

ICs for Sensors, Hall-Effect ICs, Proximity Switches

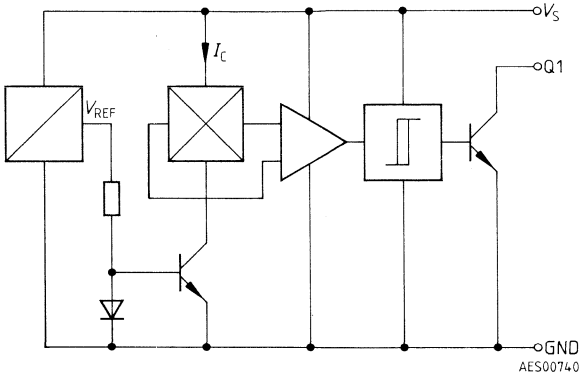
Selector Guide

Type	Package	Temperature range °C	Supply voltage V_S V	Output current I_{Qmax} mA	Magnetic switching thresholds * Flux density mT	Main applications	Page
TLE 4901 F[1]	P-SSO-3	−40 to 135	4.5 to 30	40	−12/12	RPM sensor, angle indicator, electronic commutation, speed sensor	752
TLE 4902 F[1]	P-SSO-3	−40 to 125	4.5 to 6.8	20	−15/15	RPM sensor, electronic commutation, speed sensor	758
TLE 4903 F[2]	P-SSO-3	−40 to 130	4.3 to 24	40	18/13	Breakerless triggering, limit switch	763
TLE 4910 G[3]	P-DSO-8 (SMD)	−40 to 135	4.75 to 18	10	$-\infty < B < \infty$	Positive sensor, current sensor	768
TLE 4920 F	P-SSO-3	−40 to 180	4.5 to 24	40	[1]	Geer wheel sensor, poles-wheel sensor	779
TLE 4920 G	P-DSO-8 (SMD)	−40 to 180	4.5 to 24	40	[1]	Geer wheel sensor, poles-wheel sensor	779

[1] alternating magnetic field
[2] unipolar magnetic field
[3] output voltage proportional to magnetic fiels

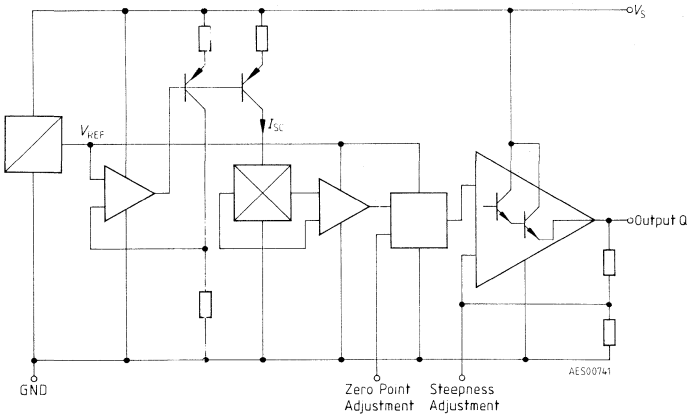
Schematic Circuit Diagrams

Digital Hall-Effect IC



On a semiconductor crystal the contactless, magnetically controlled switches contain a constant voltage regulator, a regulated voltage source for the Hall generator, a differential amplifier, a Schmitt trigger, two driver stages, and an end transistor with open collector. Their use is of advantage when high reliability, no bounce pulses, insensitivity to dirt and corrosion, and a long service life are required.

Linear Hall-Effect IC



The Hall generator is fed from a constant voltage source which uses a regulated voltage as reference. The Hall generator is followed by a differential amplifier. In the subsequent stage, the differential signal is converted into a ground-referenced signal.

At this point, the offset can be changed in a manner that is simple and interference-free, by the substraction or addition of a current.

The inverted amplifier input has been brought out, so that the steepness of the output characteristic (amplification) can be varied within a wide range by means of external components.

SIEMENS

Integrated Hall-Effect Switch for Alternating Magnetic Fields

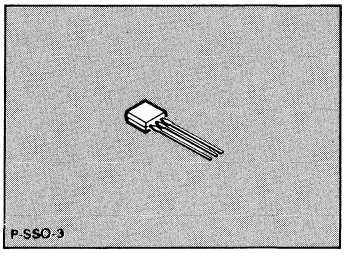
TLE 4901 F

Preliminary Data

Bipolar IC

Features

- Low switching thresholds with good-long-term stability
- High interference immunity
- Overvoltage protection
- Extended temperature range −40 to 135 °C
- Insensitive to mechanical stress
- Plastic package: P-SSO-3



Type	Ordering Code	Package
S TLE 4901 F	Q67000-A2518	P-SSO-3

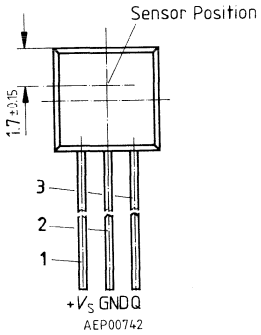
The Hall-effect IC TLE 4901 is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of the magnetic field and blocked by its north pole.

The IC is provided with an integrated overvoltage protection against most of the transients occuring in automotive and industrial applications.

The IC is particularly intended as an rpm sensor or an angle indicator.

Multiple-pole ring magnets are especially suited for switching the IC.

Pin Configuration
TLE 4901 F



Pin Definitions and Functions

Pin	Symbol	Function
1	$+V_S$	Supply voltage
2	GND	Ground
3	Q	Output

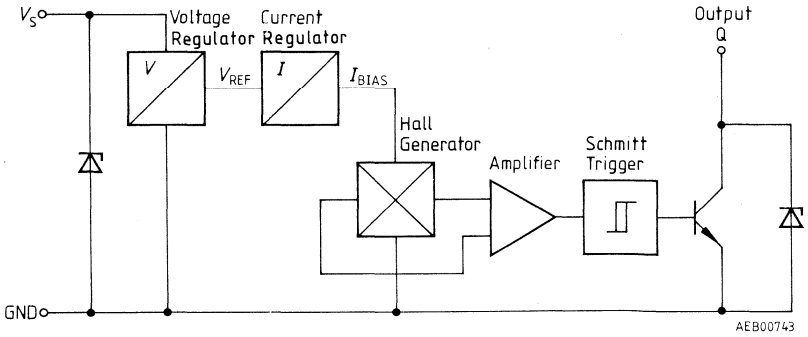
Circuit Description

The circuit includes a Hall generator, amplifier and a Schmitt trigger. The supply and the output terminals have protection circuits with Z characteristics to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt-triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

To minimize the effects of supply voltage and temperature fluctuations on the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

Block Diagram



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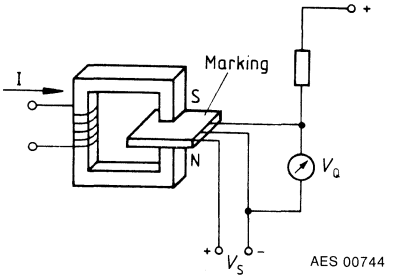
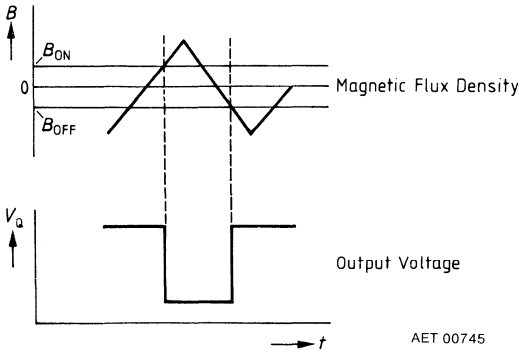
Functional Description

Whan a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reversal of the current direction in the electromagnet (i.e. reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Absolute Maximum Ratings

$T_A = -40$ to 135 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	−1.2	30	V
Output voltage, output off-state	V_Q		30	V
Output current, output on-state	I_Q		40	mA
Flux density range	B	unlimited		T
Junction temperature[1]), $t < 70000$ h	T_j		150	°C
Storage temperature, $t < 70000$ h	T_{stg}	−55	150	°C
Thermal resistance, system – air	$R_{th\ SA}$		250	K/W
Overvoltage limits Current through protection devices $t < 2$ ms	I_Z	−200	200	mA

Operating Range

Supply voltage	V_S	4.5	30	V
Ambient temperature	T_A	−40	135	°C

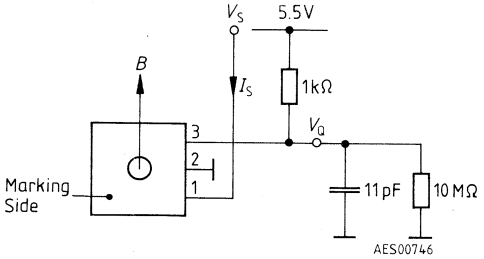
Characteristics

$V_S = 6$ to 16 V; $T_A = -30$ to 125 °C

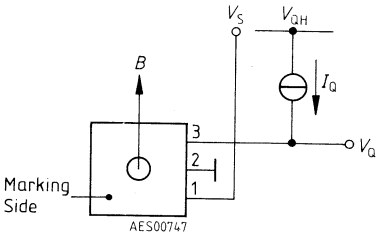
Parameter	Symbol	Limit Values			Unit	Test Circuits
		min.	typ.	max.		
Supply current $B \leqq B_{OFF}$ $B \leqq B_{ON}$	I_S	 2 3		 8 13	 mA mA	 2 2
Flux density for "ON" ($T_A = 25$ °C)	B_{ON}			10	mT	2
Flux density for "OFF" ($T_A = 25$ °C)	B_{OFF}	−10			mT	2
Flux density for "ON" ($T_A = -25$ to 85 °C)	B_{ON}			12	mT	2
Flux density for "OFF" ($T_A = -25$ to 85 °C)	B_{OFF}	−12			mT	2
Hysteresis ($T_A = -25$ to 85 °C)	B_{Hy}	3		14	mT	2
Output leakage current ($B \leqq B_{Off}$)	I_{QH}			10	µA	2
Output voltage ($I_{QL} = 16$ mA; $B \geqq B_{ON}$)	V_{QL}			0.4	V	2
Transition times of output Fall time Rise time	 t_{HL} t_{LH}		 0.3 0.5	 1 1	 µs µs	 1 1

[1]) An optimal reliability and life time of the IC are assured as long as the junction temperature does not exceed 125 °C. Though operation of the IC at the given max. junction temperature of 150 °C is possible, continuous operation at this rating could however impair the reliability of the IC considerably.

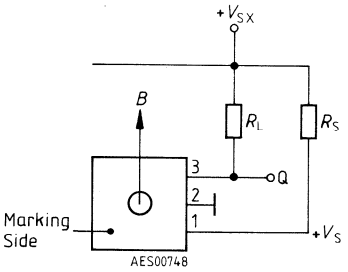
Test Circuit 1



Test Circuit 2



Application Circuit



For optimum protection against destruction, R_s is required to be as high as possible.
Dimensioning:

$$R_s = \frac{V_{SX\,min} - V_{S\,min}}{I_{S\,max}}$$

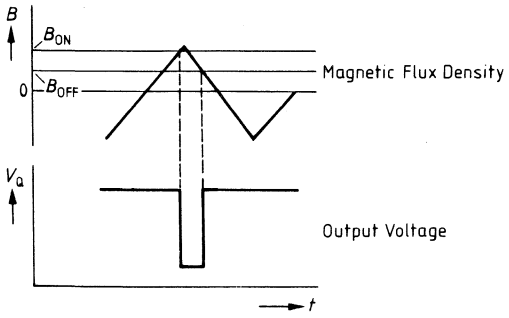
$V_{SX\,min}$ is the minimum supply voltage in each application.

Pulse Diagrams

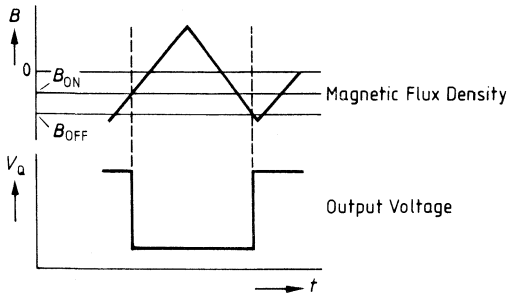
Flux density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:

$B_{ON} = B_{ON\ max}$



$B_{OFF} = B_{OFF\ min}$



11

SIEMENS

Integrated Hall-Effect Switch for Alternating Magnetic Fields

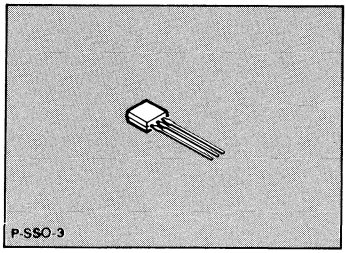
TLE 4902 F

Preliminary Data

Bipolar IC

Features

- Low switching threshold with good long-term stability
- Extended temperature range –40 to 125 °C
- Plastic package: P-SSO-3
- Suited lo low-cost applications, e.g. electronic commutation of electric motors
- Insensitive to mechanical stress

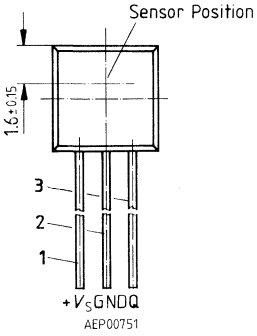


Type	Ordering Code	Package
TLE 4902 F	Q67000-A8048	P-SSO-3

The Hall-effect IC TLE 4902 F is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of a magnetic field and is blocked by its north pole.

The IC is especially suited for applications as an rpm sensor or an angle indicator.

Pin Configuration



Pin Definitions and Functions

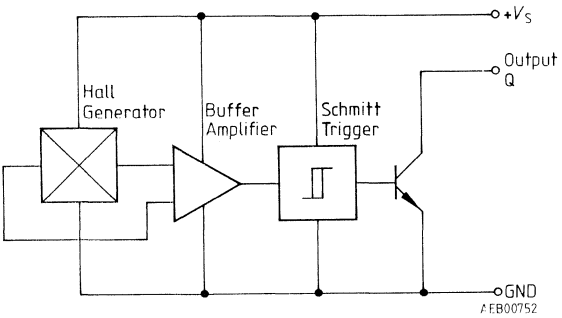
Pin	Symbol	Function
1	+V_S	Supply voltage
2	GND	Ground
3	Q	Open collector output

Circuit Description

The circuit includes a Hall generator, amplifier, a Schmitt trigger and an open collector output.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

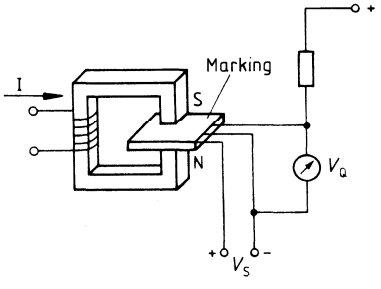
Block Diagram



Functional Description

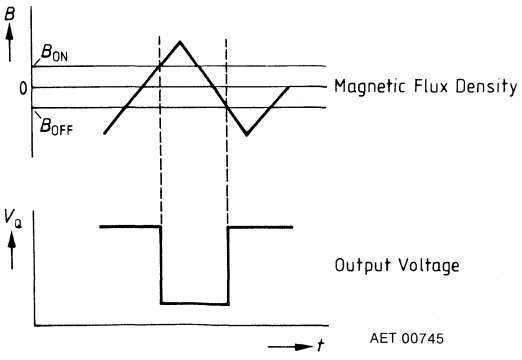
When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reversal of the current direction in the electromagnet (i.e. reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



AES 00744

Switching Characteristics



AET 00745

Absolute Maximum Ratings

$T_A = -40$ to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	−0.5	7	V
Output voltage, output off-state	V_Q		30	V
Output current, output on-state	I_Q		20	mA
Magnetic flux density range	B	unlimited		T
Junction temperature, $t < 70000$ h	T_j		150	°C
Storage temperature, $t < 70000$ h	T_{stg}	−40	150	°C
Thermal resistance, system – air	$R_{th\ SA}$		240	K/W

Operating Range

Supply voltage	V_S	4.5	6.8	V
Ambient temperature	T_A	−40	125	°C

Characteristics

$T_A = 0$ to 85 °C; $V_S = 4.5$ to 5.5 V (unless otherwise specified)

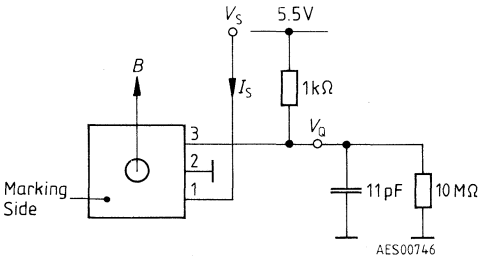
Parameter	Symbol	Limit Values			Unit	Test Circuits
		min.	typ.	max.		
Flux density for "ON" $T_A = 25$ °C	B_{ON}			10	mT	2
Flux density for "OFF" $T_A = 25$ °C	B_{OFF}	−10			mT	2
Flux density for "ON"	B_{ON}			15	mT	2
Flux density for "OFF"	B_{OFF}	−15			mT	2
Hysteresis	B_{Hy}	3		14	mT	2
Flux density $T_A = -40$ to 125 °C; $V_S = 4.5$ to 6.8 V	B_{ON}			20	mT	2
Flux density for "OFF" $T_A = -40$ to 125 °C; $V_S = 4.5$ to 6.8 V	B_{OFF}	−20			mT	2

Characteristics

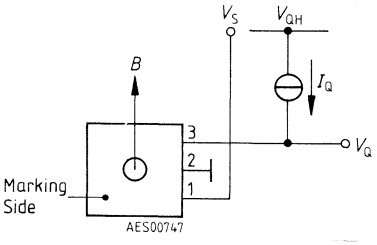
$T_A = 0$ to 85 °C; $V_S = 4.5$ to 5.5 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Circuits
		min.	typ.	max.		
Hysteresis $T_A = -40$ to 125 °C; $V_S = 4.5$ to 6.8 V	B_{Hy}	2		15	mT	2
Output current $B \leq B_{OFF}$	I_{QH}			10	µA	2
Output voltage $I_{QL} = 16$ mA; $B \geq B_{ON}$	V_{QL}			0.4	V	2
Transition times of output Fall time Rise time	 t_{HL} t_{LH}	 	 0.3 0.5	 1 1	 µs µs	 1 1
Supply current $B \leq B_{OFF}$ $B \geq B_{ON}$	 I_S I_S	 2 3	 	 5.5 6.5	 mA mA	 2 2

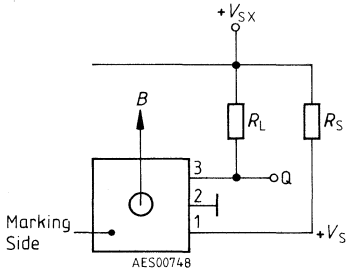
Test Circuit 1



Test Circuit 2



Application Circuit



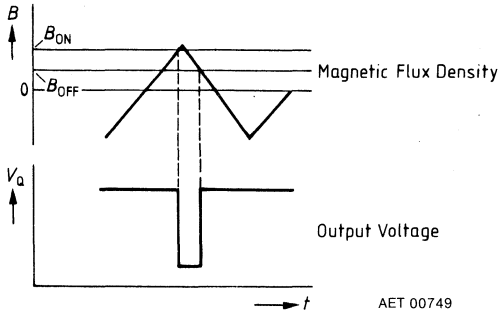
11

Pulse Diagrams

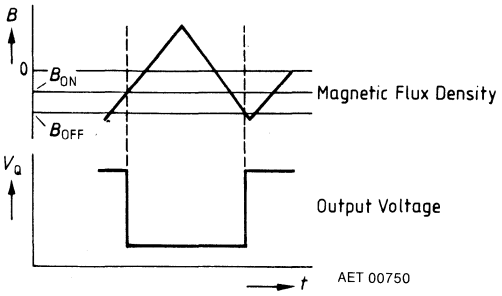
Flux density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:

$B_{ON} = B_{ON\ max}$



$B_{OFF} = B_{OFF\ min}$



SIEMENS

Integrated Hall-Effect Switch for Unipolar Magnetic Fields

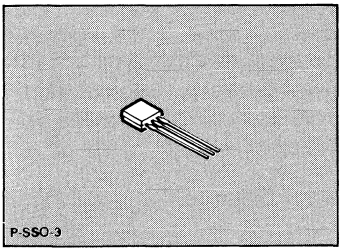
TLE 4903 F

Preliminary Data

Bipolar IC

Features

- Low switching threshold with good long-term stability
- High interference immunity
- Overvoltage protection
- Extended temperature range −40 to 130 °C
- Insensitive to mechanical stress
- Plastic package: P-SSO-3

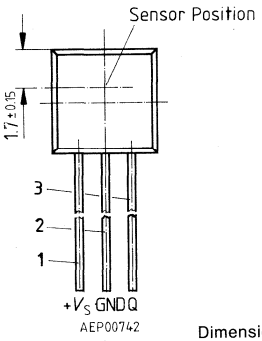


Type	Ordering Code	Package
TLE 4903 F	Q67000-A8047	P-SSO-3

The integrated Hall IC TLE 4903 F is a contactless switch operated by a magnetic field. On reaching the turn-on flux density of the south-pole of a magnetic field, the output conducts. As the flux density strength sinks below the turn-off level, the output stops conducting.

The IC is provided with an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

Pin Configuration



Dimensions in mm

Pin Definitions and Functions

1	+V_S	Supply voltage
2	GND	Ground
3	Q	Open collector output

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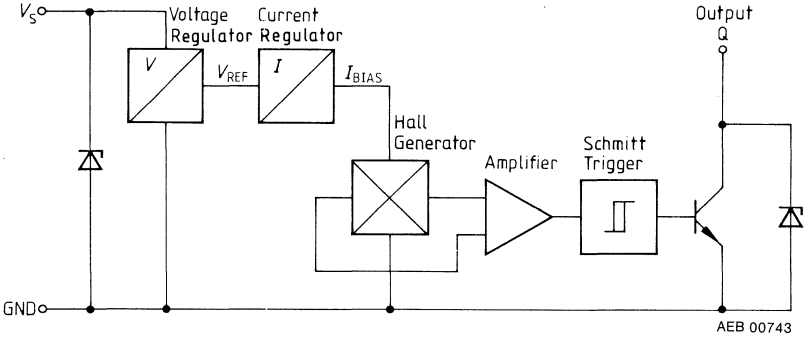
Circuit Description

The circuit includes a Hall generator, amplifier, Schmitt trigger and an open collector output. The supply and the output terminals have protection circuits to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

To minimize the effects of supply voltage and temperature fluctuations of the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

Block Diagram

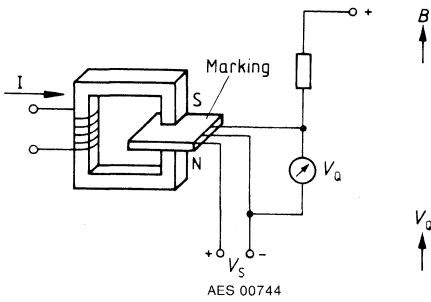


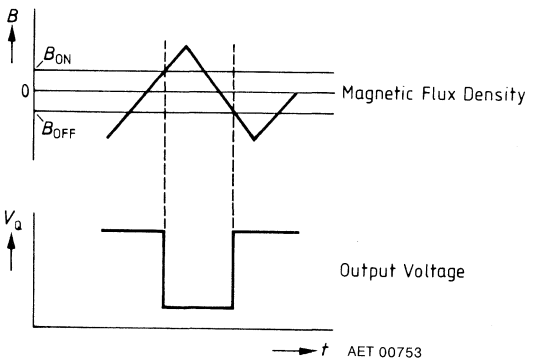
Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reduction of the current and falling below the turn-off flux density, leaves the output non-conducting.

Switching Characteristics





Absolute Maximum Ratings

$T_A = -40$ to 130 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	−1.2	30	V
Output current	I_Q		40	mA
Junction temperature[1]), $t < 70000$ h	T_j	−40	150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance, system – air	$R_{th\ SA}$		240	K/W
Flux density range	B	$-\infty$	$+\infty$	
Output voltage	V_Q		30	V

Overvoltage Limits

Current through protection devices at pins 1 and 3, $t < 10$ µs		−200	200	mA

Operating Range

Supply voltage	V_S	4.3	24	V
Ambient temperature	T_A	−40	130	°C

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[1]) An optimal reliability and life time of the IC are assured as long as the junction temperature does not exceeded 125 °C. Though operation of the IC at the given max. junction temperature of 150 °C is possible, a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

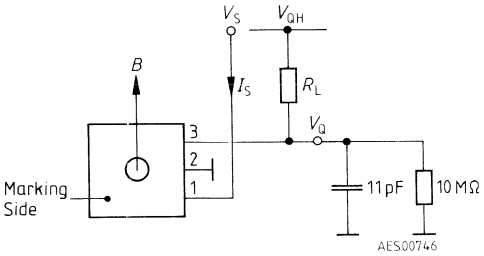
Characteristics

$V_S = 14$ V; $T_A = 25$ °C

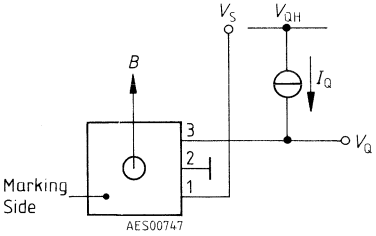
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuits
Magnetic Parameters*)							
Flux density "ON"	B_{ON}	20		50	mT**)	$T_A = 25$ °C	
		18		52	mT	$T_A = 0$ to 70 °C	
		18		57	mT	$T_A = -30$ to 100 °C	
		12		58	mT	$T_A = -30$ to 125 °C	2
Flux density "OFF"	B_{OFF}	15		35	mT	$T_A = 25$ °C	
		13		37	mT	$T_A = 0$ to 70 °C	
		8		42	mT	$T_A = -30$ to 100 °C	
		7		43	mT	$T_A = -30$ to 125 °C	2
Hysteresis ($B_{ON} - B_{OFF}$)	B_{Hy}	5		15	mT		2
Output junction current	I_{QO}			10	µA	$B < B_{OFF}$; $V_{OH} = 24$ V $T_A = 25$ °C	
Supply current	I_S			13	mA	$B < B_{ON}$	1
				14	mA	$B > B_{OFF}$	1
Output voltage	V_Q			0.4	V	$I_Q = 30$ mA	2
Rise time	t_{LH}			1	µs	$I_Q = 10$ mA	
Fall time	t_{HL}			1	µs	$I_Q = 10$ mA	
Overvoltage Limit							
Supply voltage	V_{SZ}	32		42	V	$I_S = 16$ mA	
Output	V_{QZ}	32		42	V	$I_{QZ} = 16$ mA	

*) The magnetic parameters are specified for a homogenous magnetic field at the sensor center.
**) 1 mT = 10 G

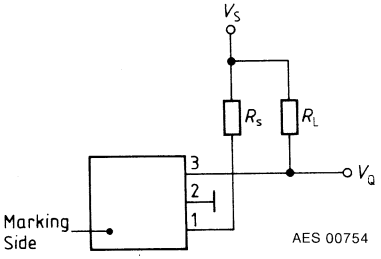
Test Circuit 1



Test Circuit 2



Application Circuit

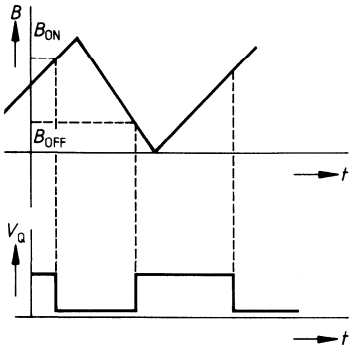


For optimum protection against destruction, R_s is required to be as high as possible.
Dimensioning:

$$R_s = \frac{V_{SX\ min} - V_{S\ min}}{I_{S\ max}}$$

$V_{SX\ min}$ = is the minimum supply voltage in each application.

Pulse Diagram



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SIEMENS

Hall-Effect IC with Analog Output

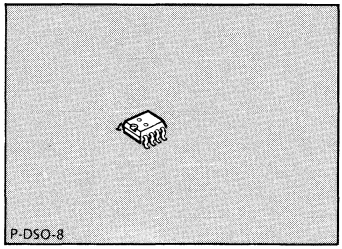
TLE 4910 G

Preliminary Data

Bipolar IC

Features

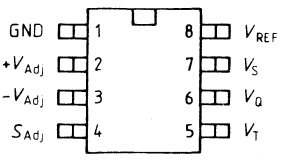
- Linear output characteristic
- Extended temperature range (−40 to 135 °C)
- Virtually independent of supply voltage and temperature fluctuations
- Reference voltage available (3 V)



Type	Ordering Code	Package
TLE 4910 G	Q67000-A9009	P-DSO-8 (SMD)

The Hall-effect IC TLE 4910 G generates at its output a voltage referred to ground that is directly proportional to the magnetic flux density passing vertically through the chip. A positive magnetic field (i.e. magnetic south pole facing the surface of the chip = stamped side) causes the output voltage to increase. The device is fully functional without any wiring. According to the application, the zero point (pin 2, 3) and the sensitivity (pin 4) can be varied over a wide range by external circuitry.

Pin Configuration

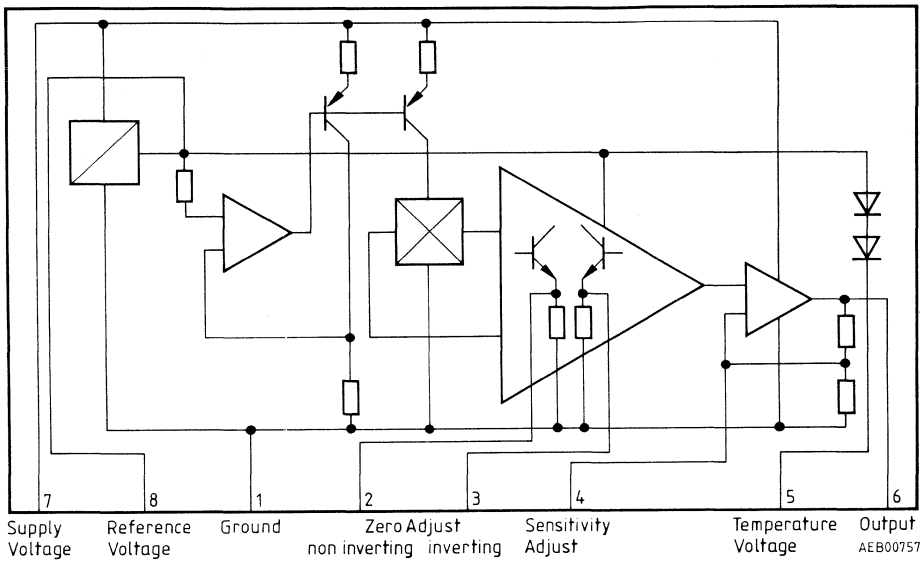


AEP 00756

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$+V_{Adj}$	+ Zero adjustment
3	$-V_{Adj}$	− Zero adjustment
4	S_{Adj}	Sensitivity adjustment
5	V_T	Temperature voltage
6	V_Q	Voltage output
7	V_S	Supply voltage
8	V_{REF}	Reference voltage

Block Diagram



Circuit Description

First a regulated voltage of 3 V is produced from the supply voltage. This voltage is brought out and feeds all parts of the circuitry whose accuracy is critical. The control current for the Hall generator is also derived from it. The Hall voltage is initially transformed by an transimpedance amplifier into a current referred to ground.

The zero point (offset) can be influenced from the exterior by way of the current balance (pin 2, 3). The signal is boosted further by a current amplifier and transformed back into a voltage on a resistor. An operational amplifier with variable gain produces a stable signal at the output.

The temperature voltage is derived from the 3 V reference voltage by subtracting two diode-forward voltages.

By adjusting the zero point:

- The manufacturing spread can be eliminated.
- The characteristic can be matched to the application so that both unipolar and bipolar magnetic fields can be detected with almost any conversion factors (magnetic field → voltage).

The circuit also provides

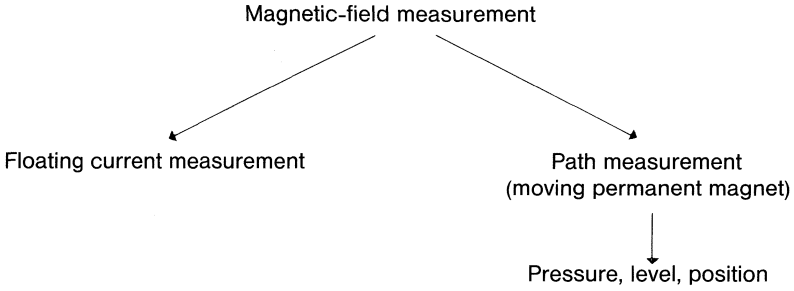
- a precise reference voltage of 3 V,
- a temperature-dependent voltage for measuring chip temperature.

The latter can be used for individual temperature compemsation of the device if very high demands are made for temperature stability (pin 2, 3).

The output characteristic begins very close to 0 V (V_{Qmin} is typically 0.005 V), so that measurement can start practically at zero with just one supply voltage. The output voltage can be loaded with up to 5 mA without degrading the accuracy.

To minimize the piezoresistive effect (change in the zero point through mechanical tension) four Hall probes are configured in a suitable manner. Even after extreme temperature cycling (–65 to 150 °C), leading to changes in the tension of the chip, there are only slight shifts in the magnetic zero B_0 of maximally ± 3 mT.

The main areas of application are:



Absolute Maximum Ratings

$T_A = -40\,°C$ to $180\,°C$, $t < 50$ h

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage	V_S	−0.8	30	V
Output current	I_Q		10	mA
Current at reference (pin 8)	I_{VREF}		10	mA
Zero-adjustment current	I_{Adj}	−1	1	mA
Junction temperature $t < 3400$ h $t < 1000$ h $t <$ 75 h	T_j		 150 170 210	 °C °C °C
Thermal resistance	R_{th}		170	K/W

Operating Range

Supply voltage	V_S	4.75	18	V
Output current	I_Q		5	mA
Ambient temperature	T_A	−40	150	°C

Characteristics

$V_S = 4.75 \leq 15$ V, $T_A = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Circuits
Total current $R_L = 10$ kΩ; $B < -20$ mT	I_S			10	mA	1
Output voltage $R_L = 10$ kΩ; $B < -20$ mT $R_L = 10$ kΩ; $B > 300$ mT	V_Q	 V_S-2	 5 $V_S-1.5$	 20 	 mV V	 1 1
Sensitivity $T_A = 25\,°C$	S	22	30	38	V/T	1
Magnetic offset	B_0	−20		20	mT	1
Reference voltage $T_A = 25\,°C$	V_{REF}	2.9	3.0	3.1	V	1

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Characteristics

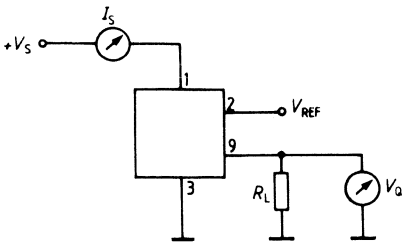
$V_S = 4.75 \leq 15$ V, $T_A = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values			Unit	Test Circuits
		min.	typ.	max.		
Output voltage/adjustment current (pin 2, 3) $T_A = 25\,°C$	V_Q/I_{Adj}		±0.3		V/µA	2
Voltage at pin 2, 3 $T_A = 25\,°C$	V_{Adj}	50	70	90	mV	2
Temperature voltage $R = 5$ kΩ; $T_A = 25\,°C$	V_T	1.4		1.7	V	3
Temperature coefficient of V_T $R = 5$ kΩ	TC_T	3.2	3.5	3.7	mV/K	3
Output impedance $V_S = 5$ V; $I_Q = 5$ mA	R_Q			10	Ω	1
Sensitivity change due to V_S changes $T_A = 25\,°C$	$\Delta S/\Delta V_S$			0.2	%/V	1
Magnetic offset due to V_S changes	$\Delta B_0/\Delta V_S$	−20		20	µT/V	1
Magnetic offset change after high temperature endurance test 1000 h / 150 °C	ΔB_0			±3	mT	
Thermal cycling −65 °C / 150 °C (1000 x)				±3	mT	
Humidity test 85 °C / 85%				±3	mT	

For temperature changes due to magnetic offset and sensitivity, **see diagrams.**

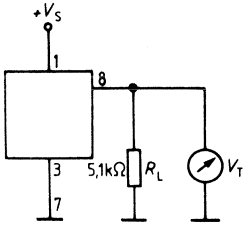
Hall ICs may change their magnetic offset slightly after climatic stress.

Test Circuit 1



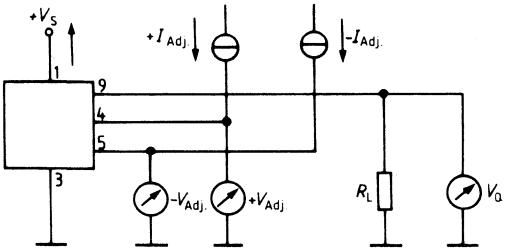
AES 00758

Test Circuit 3



AES 00759

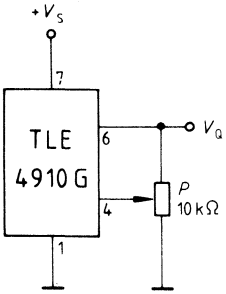
Test Circuit 2

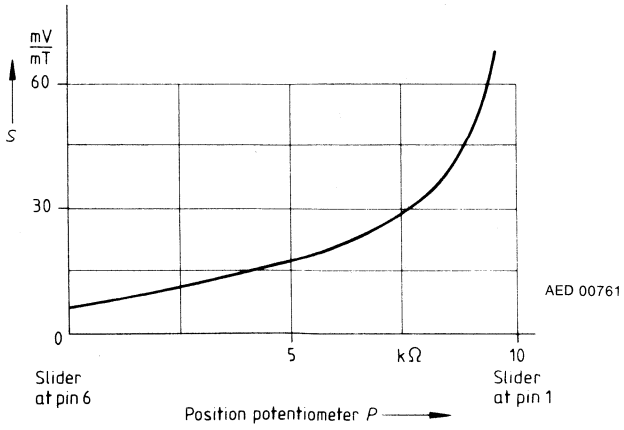


AES 00759

Diagrams

Position Characteristics of Sensitivity Adjustment





AED 00761

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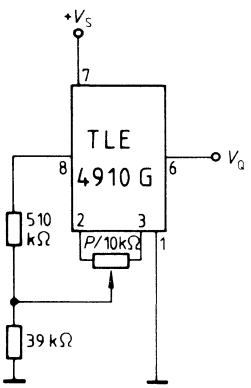
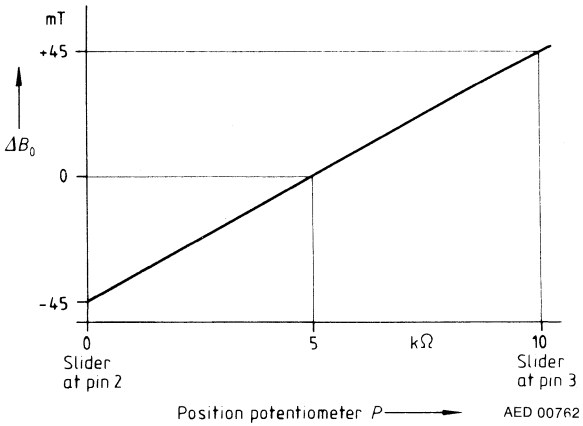
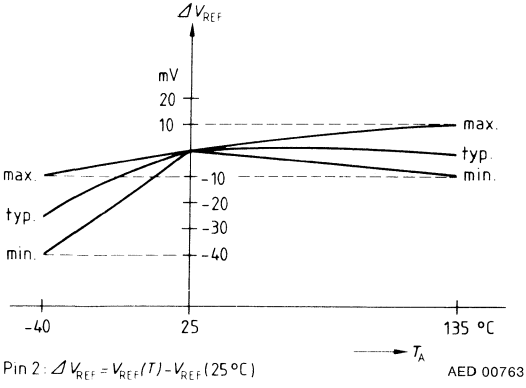
Diagrams
Position Characteristics at Magnetic Offset



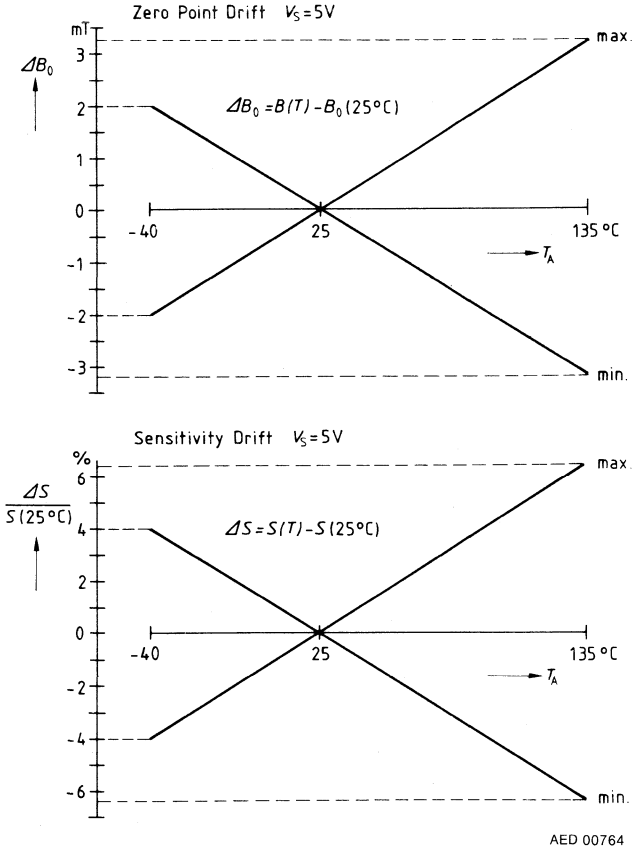


Diagrams
Temperature Dependence of Reference Voltage



Diagrams

Temperature Dependence of Zero Point and Sensitivity



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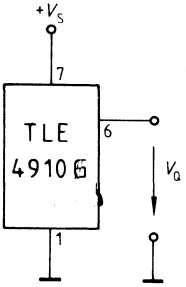
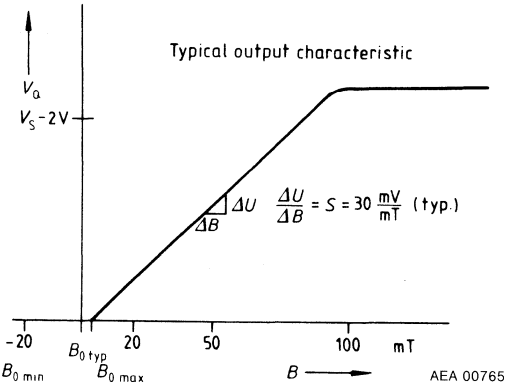
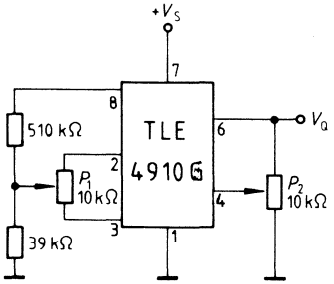
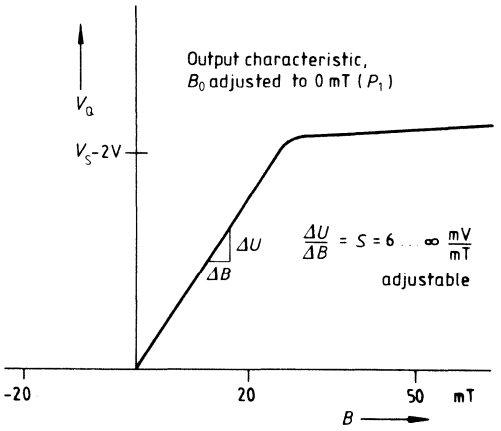
Application Circuit 1
Measuring Positive Magnetic Field without Electrical Adjustment



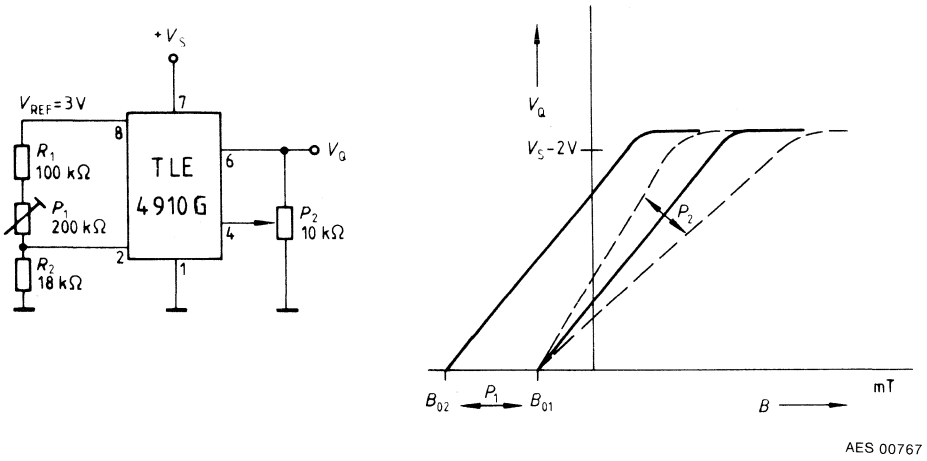


Application Circuit 2
Measuring Positive Magnetic Field with Adjustment of Offset and Sensitivity

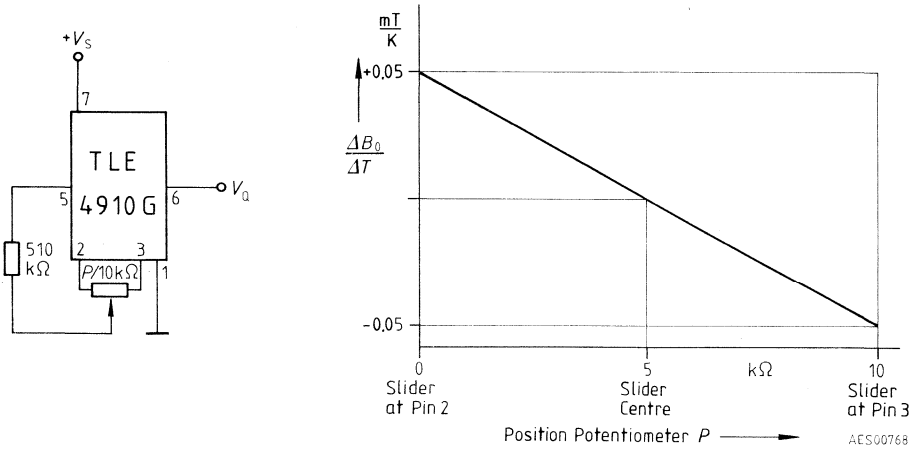




Application Circuit 3
Measuring Bipolar Magnetic Field by Shifting "Starting Point" to Negative Field



Application Circuit 4
Application Circuit for Individual Compensation of B_0 Temperature Drift



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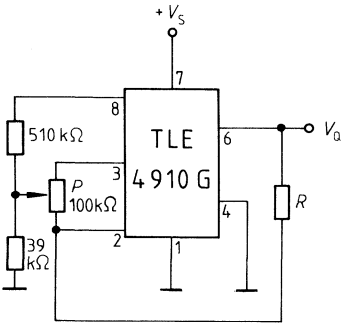
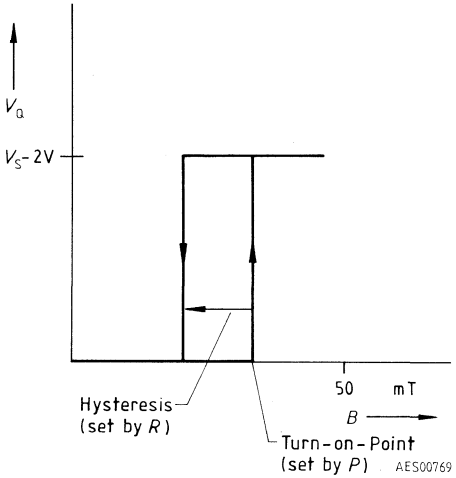
Application Circuit 5
Switching Mode with Adjustable Threshold



$$R = \frac{V_S - 2}{B_{Hy} \times 10^{-5}}$$

B_{Hy} in mT
R in



SIEMENS

Differential Gear Tooth Sensor IC

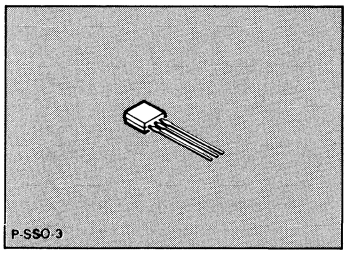
TLE 4920 F
TLE 4920 G

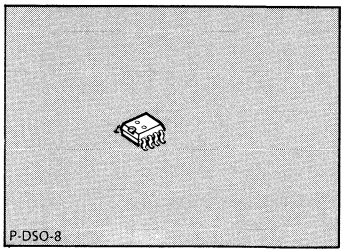
Preliminary Data

Bipolar IC

Features

- Wide range of effective air gaps
- Digital output signal
- Static operation down to 0 rpm
- Supply voltage 4.5 V to 24 V
- Wide operating temperature range −40 to +150 °C
- Short term up to 180 °C
- 2-wire or 3-wire application
- Overvoltage protection
- Reverse polarity protection





Type	Ordering Code	Package
▼ TLE 4920 F	Q67000-A9023	P-SSO-3
S ▼ TLE 4920 G	Q67000-A9000	P-DSO-8 (SMD)

▼ New type

Functional Description

The gear tooth sensor-ICs TLE 4920 F/G are particularly suitable for detecting the speed of ferromagnetic gear wheels (e.g. in anti-lock braking systems in automobiles, in transmissions and the like). The integrated circuit (based on Hall effect) provides a digital signal with a frequency that is proportional to the speed of the gear wheel. Over the total operating air gap range this signal remains unaffected by radial vibration of the gear wheel resulting from bearing clearance or other influences.

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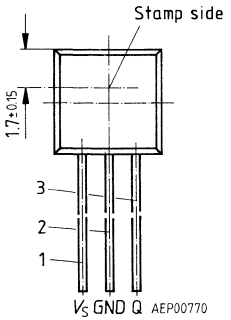
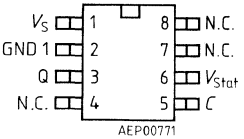
Pin Configuration
TLE 4920 F



Pin Definitions and Functions

Pin	Symbol	Description
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

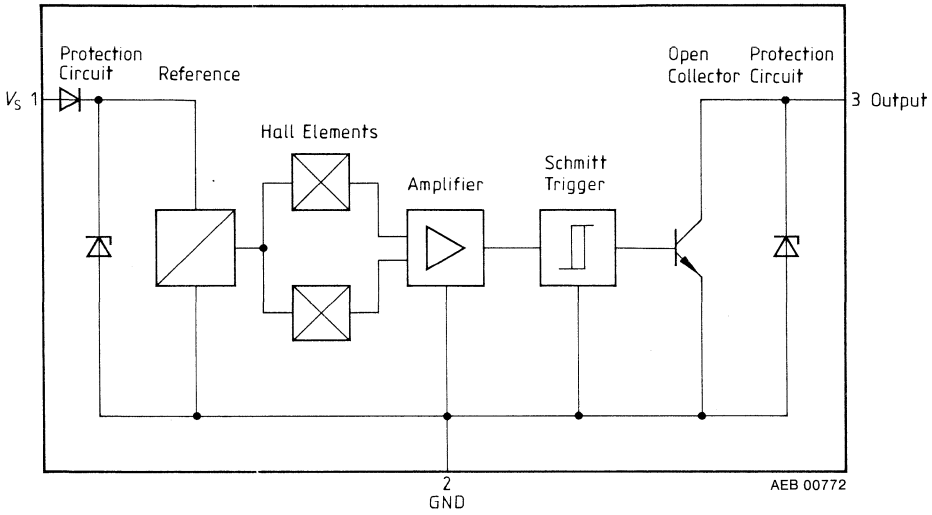
Pin Configuration
TLE 4920 G



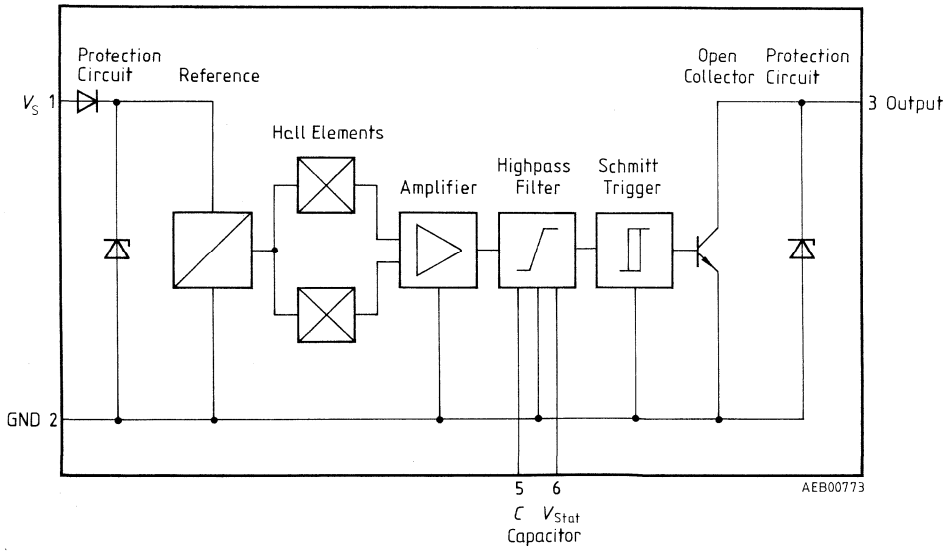
Pin Definitions and Functions

Pin	Symbol	Description
1	V_S	Supply voltage
2	GND 1	Ground 1
3	Q	Output
4	N.C.	Not connected
5	C	Capacitor
6	V_{Stat}	Highpass bypass
7	N.C.	Not connected
8	N.C.	Not connected

Block Diagram
TLE 4920 F



Block Diagram
TLE 4920 G



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Circuit Description (see Block Diagrams)

The integrated circuits TLE 4920 F/G include two Hall-arrays that produce a voltage proportional to the magnetic field.

The integrated signal processing circuit produces the difference between the two Hall-voltages and switches the output after exceeding a certain threshold.

The **TLE 4920 G version** includes an active highpass filter requiring an external capacitor. This case (dynamic mode) **permits larger operating air gaps** (0 rpm operation cannot be achieved).

The open-collector output as well as the input of the devices are protected against overvoltage by special clamp structures (together with an external series resistor, complying with ISO-TR 7637).

Reverse polarity protection is also integrated.

Absolute Maximum Ratings

$V_S = -40$ to 30 V; $T_A = -40\,°C$ to $150\,°C$

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Output voltage	V_Q	−0.7	30	V	
Output current	I_Q		40	mA	
Output reverse current	$-I_Q$		40	mA	$T_A \leq 40\,°C$
Junction temperature	T_j T_j T_j		125 170 210	°C °C °C	 < 2000 h < 75 h
Storage temperature	T_{stg}	−40	150	°C	
Thermal resistance, system-air	$R_{th\ SA}$		125	K/W	
Overvoltage protection Current through input and output protection structures	I_Z	−200	200	mA	$t < 2$ ms

Load dump according to DIN 40839, ISO-Technical Report 7637

Test pulse	Supply voltage	Pulse duration
1	$V_S = -100$ V	$t_d = 2$ ms, no protective resistor necessary
2	$V_S = 100$ V	$t_d = 0.2$ ms, protective resistor $R_p = 300\ \Omega$ necessary
3a	$V_S = -150$ V	$t_d = 0.1\ \mu$s, no protective resistor necessary
3b	$V_S = 100$ V	$t_d = 0.1\ \mu$s, protective resistor $R_p = 300\ \Omega$ necessary
4	$V_S = -7$ V	$t_d = 130$ ms, protective resistor necessary
5	$V_S = 120$ V	$t_d = 400$ ms, protective resistor $R_p = 300\ \Omega$ necessary

R_p: **see application circuit**

Operating Range

Parameter	Symbol	Limit Values		Unit	Conditions
		min.	max.		
Supply voltage	V_S	4.5	24	V	
Ambient temperature	T_A	−40	125[1]	°C	
	T_A	−40	140[1]	°C	< 2000 h
	T_A	−40	180[1]	°C	< 75 h

[1] at $V_S = 12$ V maximum T_A can be exceeded by 15 °C

Characteristics

$V_S = 4.5$ to 24 V; $T_A = -40$ to 125 °C

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
TLE 4920 G						
Current consumption	I_S		12		mA	V_Q = High
	I_S		13		mA	V_Q = Low
Saturation voltage	V_{QSat}			0.4	V	$I_Q = 40$ mA $V_S \geq 7$ V
Reverse current	I_{QR}			1	µA	
Switching frequency	f	2.5[1]		12000	Hz	
Differential turn-on induction	ΔB		1[1]		mT	$T_A = 25$ °C
Overvoltage						
Supply voltage	V_{SZ}	30		38	V	$I_S = 16$ mA
Output	V_{QZ}	30		38	V	$I_S = 16$ mA
Distance IC/target wheel	see Diagrams 1 and 2					
TLE 4920 F						
Current consumption	I_S		8		mA	V_Q = High
	I_S		9		mA	V_Q = Low
Saturation voltage	V_{QSat}			0.4	V	$I_Q = 40$ mA $V_S \leq 7$ V
Reverse current	I_{QR}			1	µA	
Switching frequency	f	0		12000	Hz	
Differential turn-on induction	ΔB		3		mT	$T_A = 25$ °C
Overvoltage						
Supply voltage	V_{SZ}	30		38	V	$I_S = 16$ mA
Output	V_{QZ}	30		38	V	$I_S = 16$ mA
Distance IC/target wheel	see Diagrams 1 and 2					

[1] TLE 4920 G in dynamic mode with gear wheel m = 2, d = 1 mm, C = 680 nF

Application Description

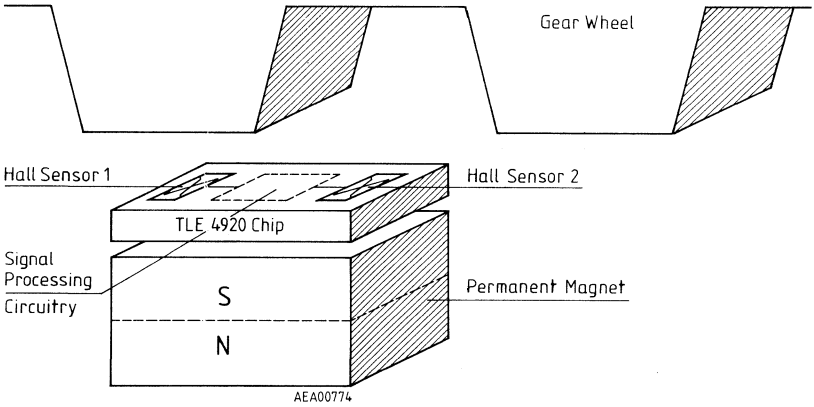
Two possible applications are shown in the figures below.

In the case of ferromagnetic gear wheel application the IC has to be biased by the south pole of a permanent magnet (e.g. Sm_2Co_{17}, Vacuumschmelze VX225, with the dimensions 8 mm x 8 mm x 4 mm).

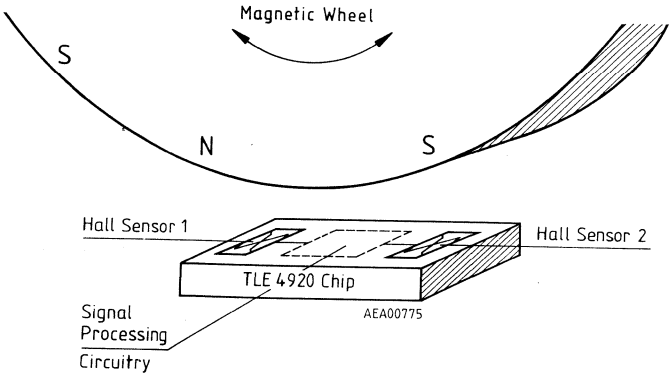
The maximum air gap depends on
- the magnetic field strength, i.e. magnet used
- the gear wheel (dimensions, material, etc),
- the ambient temperature
- the capacitor (dynamic mode TLE 4920 G)

The differences between 2-wire and 3-wire mode are shown in **application circuits**

TLE 4920 with Ferromagnetic Gear Wheel



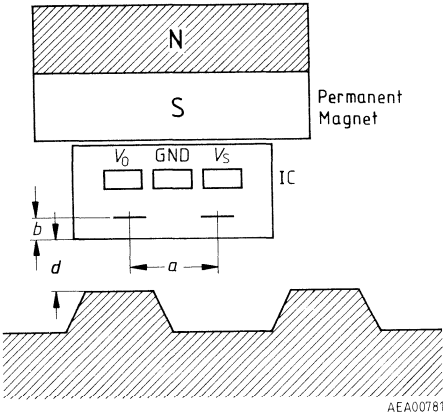
TLE 4920 with Magnetic Wheel



Application Description

Sensor dimensions

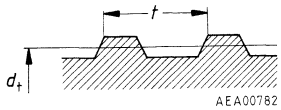
a distance between Hall sensor arrays $a = 2.49$ mm
b distance between Hall sensor arrays $b = 0.50$ mm
d gap between IC surface and gear wheel



Permanent magnet

The permanent magnet is placed with its south pole toward the rear of the IC and should cover both Hall sensors. A powerful magnet will provide a large operating air gap.

Gear wheel dimensions



DIN
d_t pitch diameter (mm)
z number of teeth
m modulus m = d/z (mm)
t pitch t = π x m (mm)

ASA
p diametral pitch p = z/d (inch)
PD pitch diameter PD = z/p (inch)
CP circular pitch CP = 1 inch x π /p

Conversion:
m = 25.4 mm/p
t = 25.4 mm x CP

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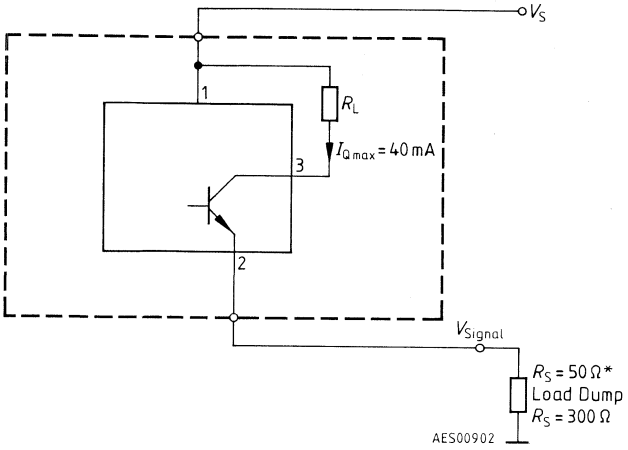
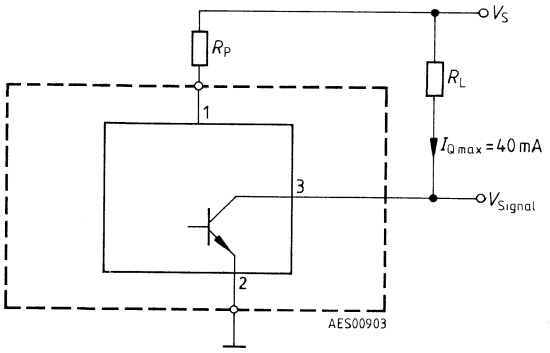
Application Circuits

2-Wire Connection



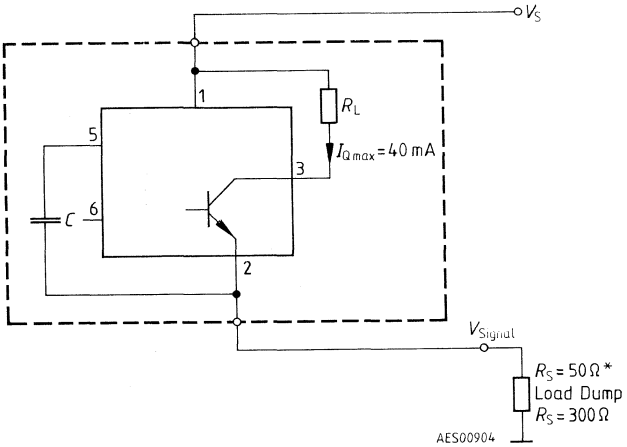
3-Wire-Connection



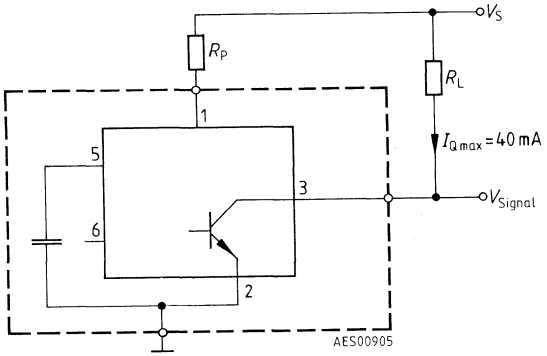
* for load dump protection "Absolute Maximum Ratings": $R_S = R_P = 300\ \Omega$

Application Circuits

2-Wire Connection

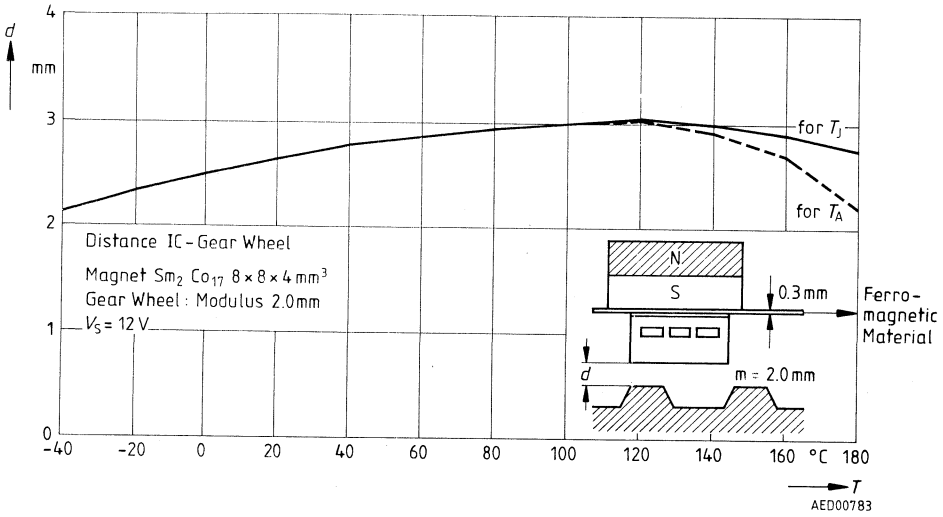


3-Wire Connection

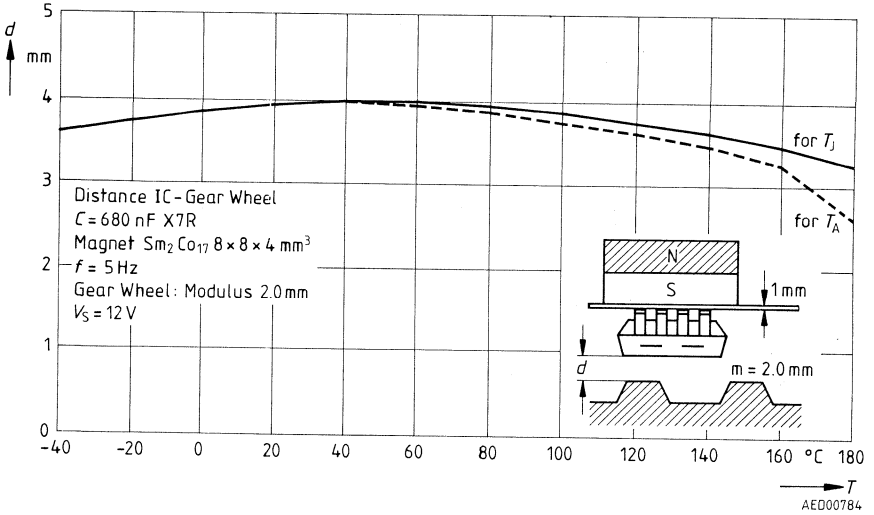


* for load dump protection "Absolute Maximum Ratings": $R_S = R_P = 300\ \Omega$

Maximum Air Gap versus Temperature (Typical Value) TLE 4920F

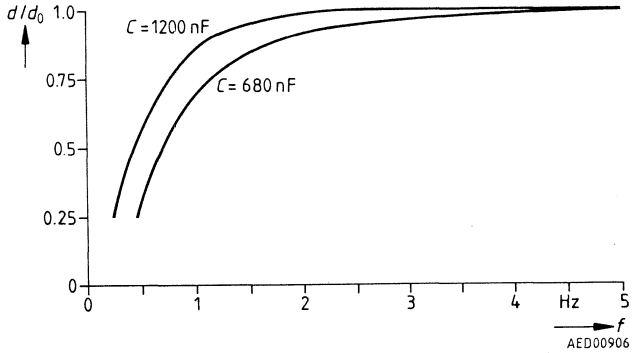


Maximum Air Gap versus Temperature (Typical Value) TLE 4920G

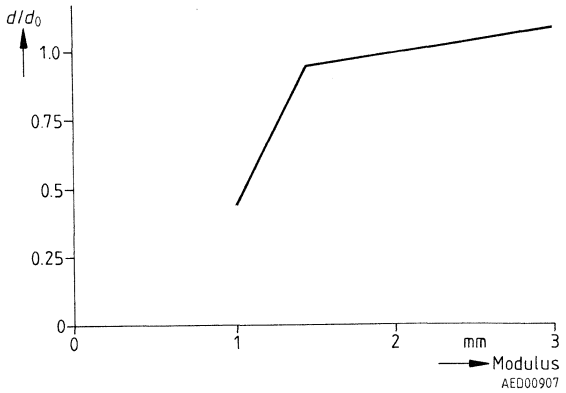


Diagrams

Dynamic mode: **normalized distance IC/target wheel d/d_0**
versus lowest detectable speed f
gear wheel modulus $m = 2.0$ mm
permanent magnet Sm_2Co_{17}, size 8 x 8 x 4 mm³
$V_S = 12$ V



Dynamic mode: **normalized distance IC/target wheel d/d_0**
versus modulus m
permanent magnet Sm_2Co_{17}, size 8 x 8 x 4 mm³
capacitor $C = 680$ nF, $V_S = 12$ V



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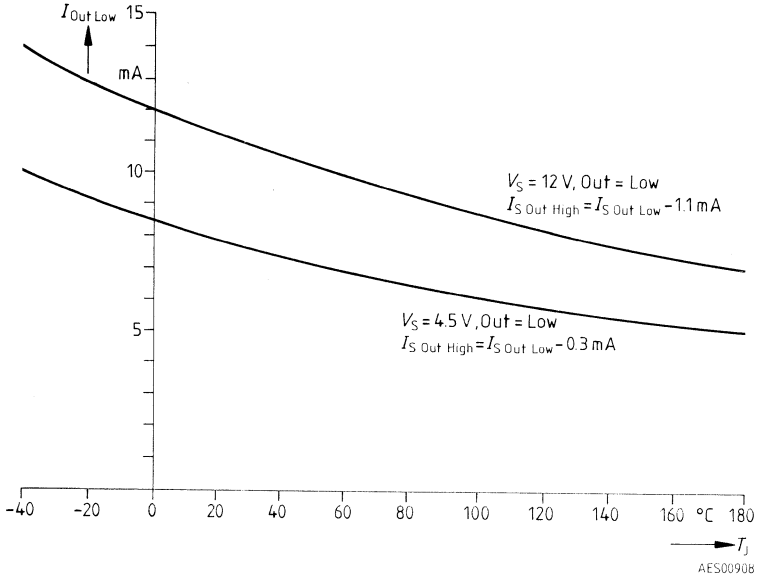
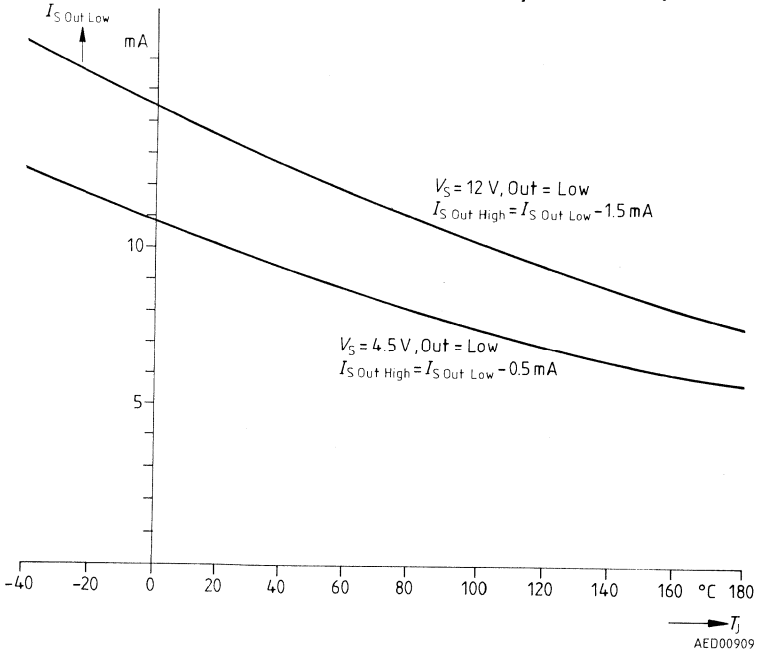
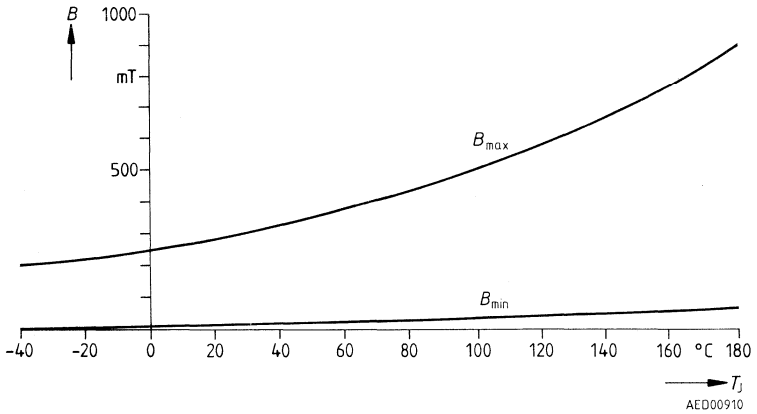
Supply Current I_S versus Junction Temperature T_j (TLE 4920 F)



Supply Current I_S versus Junction Temperature T_j (TLE 4920 G)



Range of Magnetic Flux for proper function, measured on the chip (Southpole at the reverse side of the IC)



11

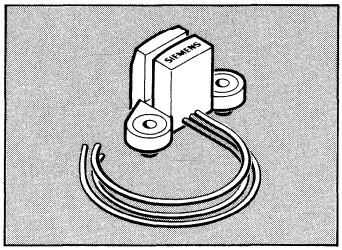
Hall-Effect Vane Switch

HKZ 101

Bipolar IC

Features

- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity

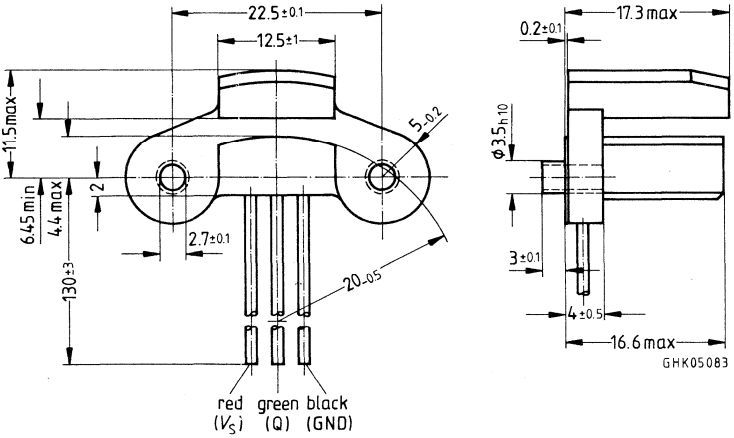


Type	Ordering Code	Package
HKZ 101	Q67000-A9002-A401	Special package

The Hall-effect vane switch HKZ 101 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a soft-iron vane which is passed through the air gap between magnet and Hall sensor.

The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmental conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).

Special Package

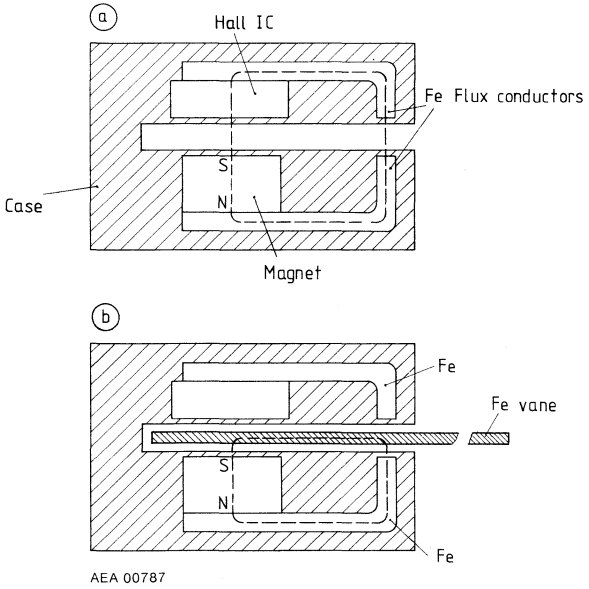


Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the hall-effect sensor, as shown below. The open collector output is conductive (low) when the vane is outside the air gap, and blocks (high) when the vane is introduced into the air gap. The output remains high as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.

Principle of Operation



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

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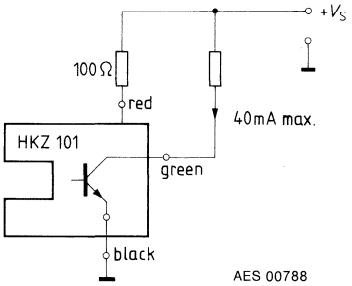
Mechanical Characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic package, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply, output and ground.

Application Notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.



Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Supply voltage	V_S	−1.2	24	V	
			30	V	$T_A = 25\,°C$
Output voltage in OFF-state	V_Q	−0.8	30	V	
Inverse supply current (limited externally)	$-I_S$		200	mA	$T_A \leq 80\,°C$, $t \leq 1$ h
Output current	I_Q		40	mA	without vane
Inverse output current	$-I_Q$		30	mA	
Ambient temperature	T_A	−40	135	°C	
Storage temperature	T_{stg}	−40	150	°C	
Thermal resistance system – air	$R_{th\,SA}$		170	K/W	

Operating Range

Supply voltage		V_S	4.5	24	V	
Ambient temperature		T_A	−40	130	C	
Vane[1]:	thickness	a	0.5		mm	
	width	b	8		mm	
	gap length	c	8		mm	
	immersion depth	h	4.6	9	mm	
	gap height	d	17.3 − h		mm	

[1]) **see figure 3**

Characteristics

$V_S = 5$ V to 18 V, $T_A = -30\,°C$ to $130\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Output saturation voltage	$V_{Q\,sat}$				without vane $I_Q = 40$ mA
			0.4	V	$T_A = -30$ to $110\,°C$
			0.6	V	$T_A = 110$ to $130\,°C$
Output reverse current	$I_{Q\,R}$		10	µA	with vane
Supply current	I_S		12	mA	without vane
Delay time	t_{LH}, t_{HL}		1	µs	$I_Q = 40$ mA
Overvoltage protection – Supply voltage (V_S) – Output (V_Q)	 V_{SZ} V_{SO}	 32 32	 42 42	 V V	 $I_S = 16$ mA $I_S = 16$ mA

Switching Point Characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics are important on temperature and operating voltage.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown the following figure.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions ($V_S = 12$ V, $T_A = 25\,°C$) within the characteristic device deviation.

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$

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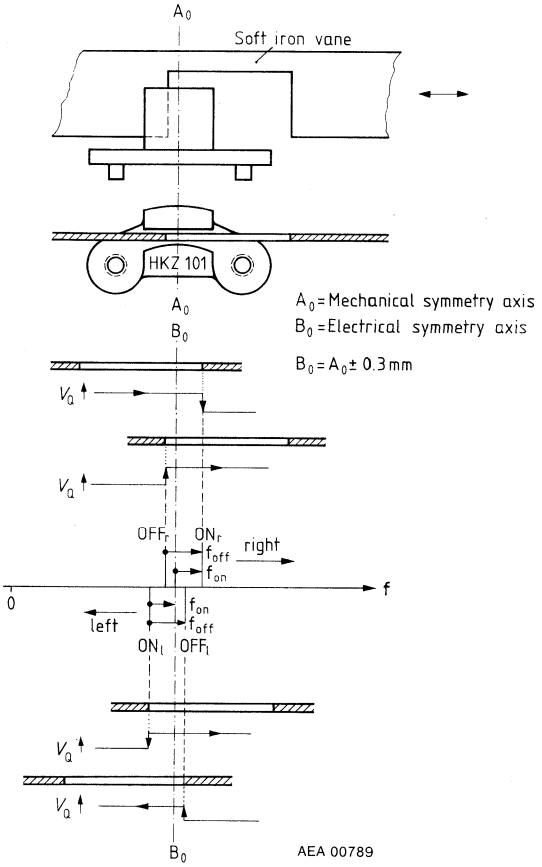
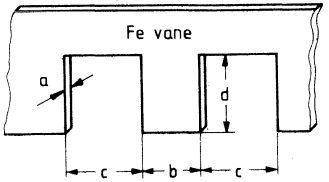
Switching Point Definitions

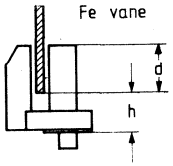


Mechanical Measurement Conditions

a) Measuring vane (material: soft iron)



b) Immersion depth



AEA 00790

Switching Point Characteristics

Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
HKZ 101						
Operate point	$f_{ON\,0}$	0.85	1.45	2.05	mm	V_S = 12 V, T_A = 25 °C
Deviations	Δf_{ON}	−0.4	+0.15	+0.7	mm	T_A = −30 to 25 °C
		−0.2	+0.15	+0.4	mm	T_A = 25 to 80 °C
		−0.4	+0.2	+0.7	mm	T_A = 80 to 130 °C
Release point	$f_{OFF\,0}$	1.54	2.54	3.54	mm	V_S = 12 V, T_A = 25 °C
Deviations	Δf_{OFF}	−0.8	+0.3	1.4	mm	T_A = −30 to 25 °C
		−0.4	+0.3	0.8	mm	T_A = 25 to 80 °C
		−0.8	+0.4	1.4	mm	T_A = 80 to 130 °C

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Selector Guide

Typ	Package	Output current mA	Current consumption mA	Supply voltage V	Feature	Page
TCA 205 A	P-DIP-14	50	2	4.75 to 30	Turn-on delay	799
TCA 305 A	P-DIP-14	50	1	5 to 30	Temporarily short-circuit proof	805
TCA 305 G	P-DSO-14 (SMD)	50	1	5 to 30	Temporarily short-circuit proof	805
TCA 355 B	P-DIP-8	50	1	5 to 30	Temporarily short-circuit proof	805
TCA 355 G	P-DSO-8 (SMD)	50	1	5 to 30	Temporarily short-circuit proof	805
TCA 505 A	P-DIP-16	60	0.75	3.1 to 4.5/ 4 to 40	Short-circuit protection	812
TCA 505 G	P-DSO-16 (SMD)	60	0.75	3.1 to 4.5/ 4 to 40	Short-circuit protection	812

SIEMENS

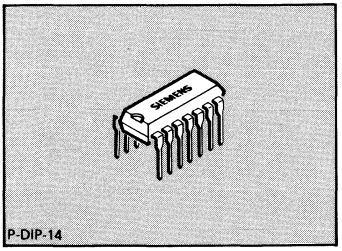
Proximity Switch

TCA 205

Bipolar IC

Features

- Large supply voltage range
- High output current
- Antivalent outputs
- Adjustable switching distance
- Adjustable hysteresis
- Turn-on delay

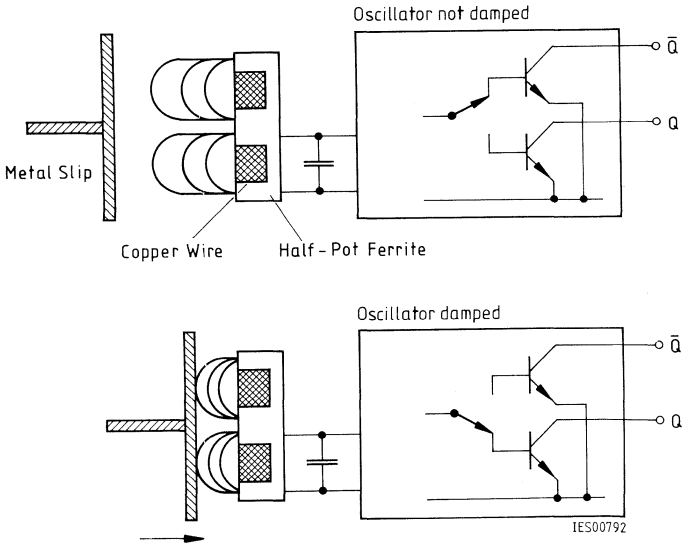


Type	Ordering Code	Package
■ TCA 205 A	Q67000-A1034	P-DIP-14

■ Not for new design.

This IC is intended for applications in inductive proximity switches. The outputs switch when the oscillation is damped, e.g. by the approach of a metal object.

Operation Schematic



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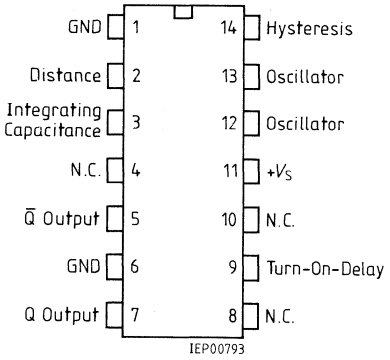
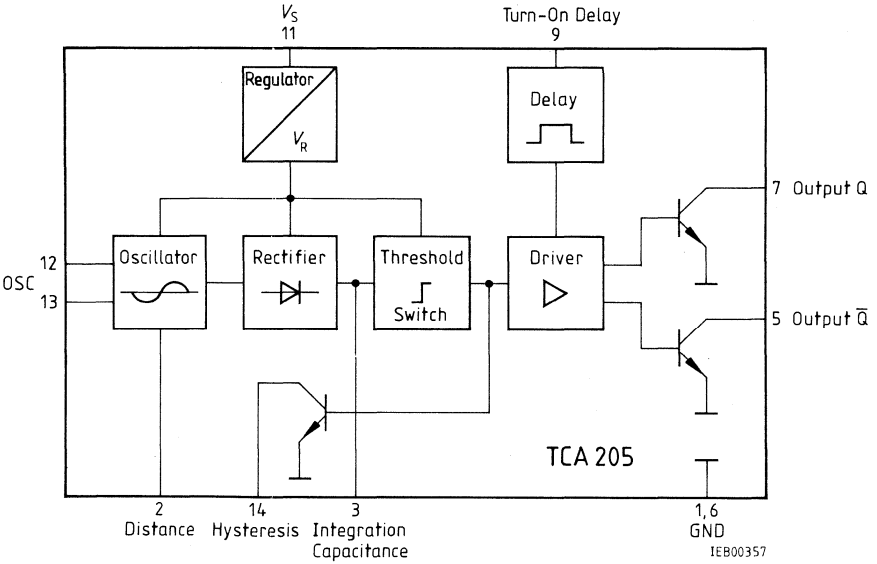
Pin Configurations
(top view)



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage Output voltage	V_S V_Q	30 30	V V
Output current	I_Q	50	mA
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 205 A	$R_{th\ SA}$	85	K/W

Operating Range

Supply voltage	V_S	4.75 to 30	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

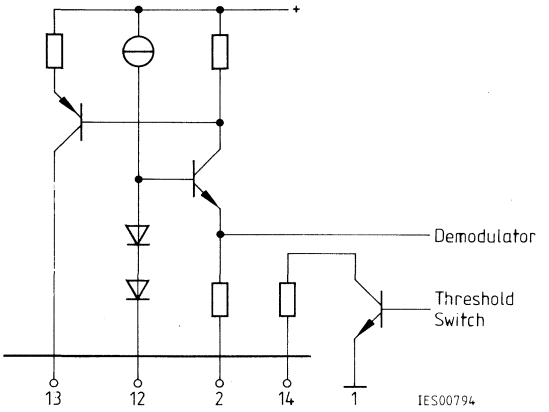
$V_S = 12$ V, $T_A = 25$ °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Open-loop supply current consumption	I_S		1	2	mA	open pins
L-output voltage per output	$V_{Q\,L}$ $V_{Q\,L}$		0.8 1.25	1 1.5	V V	$I_{Q\,L} = 5$ mA $I_{Q\,L} = 50$ mA
H-output current per output	$I_{Q\,H}$			10	µA	$V_{Q\,H} = 30$ V
Integrating capacitance	C_I		10		nF	
Internal resistance at 3	$R_{I\,3}$	200	350	660	kΩ	
Threshold voltage at 3	$V_{S\,3}$		1.3	1.5	V	
Distance adjustment (circuit 1) Hysteresis adjustment (circuit 1)	R_{Di} R_{Hy}	6 0			kΩ kΩ	
Distance adjustment (circuit 2) Hysteresis adjustment (circuit 2)	R_{Di} R_{Hy}	6[1]) 6[1])			kΩ kΩ	$R_{Hy} \rightarrow \infty$ $R_{Di} \rightarrow \infty$
Turn-on delay	t_{Don}		200		ms/µF	
Oscillating frequency Switching frequency without C_I	f_{OSC} f_S	0.015		1.5 5	MHz kHz	

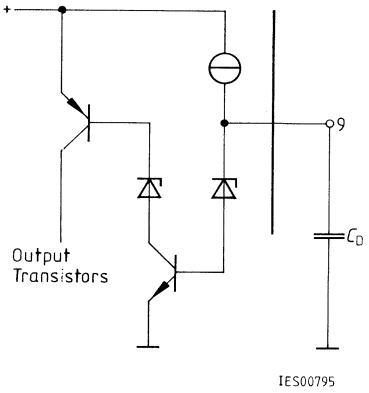
[1]) Parallel connection of R_{Hy} to R_{Di} may at least amount to 6 kΩ

Schematic Circuit Diagrams

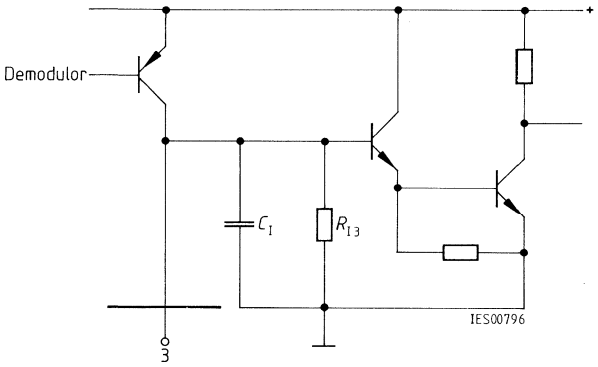
Oscillator



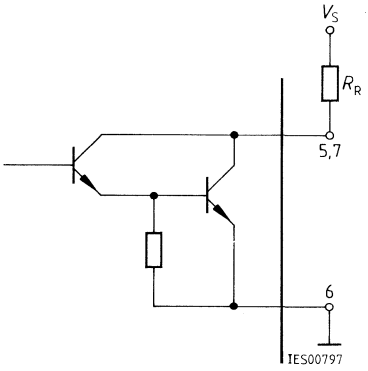
Turn-on delay



Integrating capacitor

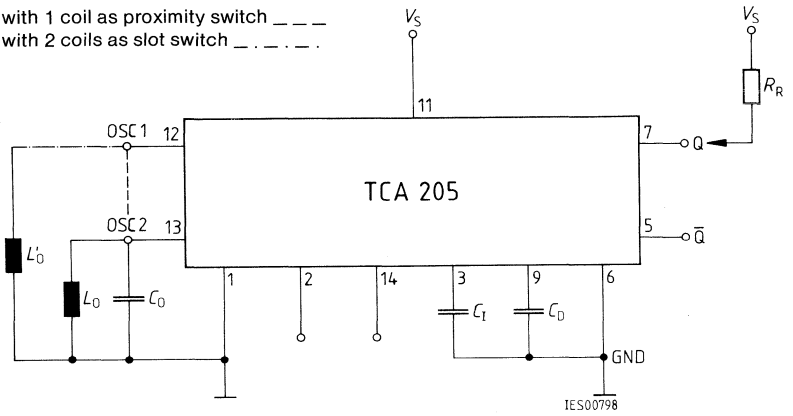


Outputs



Application Circuit

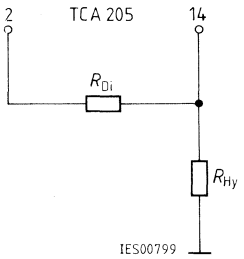
with 1 coil as proximity switch _ _ _
with 2 coils as slot switch _ . _ . _ .



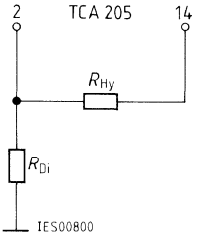
L_0, C_0	oscillator
R_{Di}	distance adjustment
R_{Hy}	hysteresis adjustment
C_I	integrating capacitor
C_D	delay capacitor

The resistance of distance and hysteresis R_{Di} and R_{Hy}, for proximity switch TCA 205 A; may be applied as follows:

1. Series hysteresis



2. Parallel hysteresis



Circuit 1 is more suitable for proximity switches with oscillator frequencies of $f > 200$ kHz to 300 kHz, and small distances. Circuit 2 is more favorable for AF proximity switches having larger distances. This is due to the lower R_{Hy} values enabled by circuit 1 (min. 0 Ω) compared with 2 circuit 2 (min. 6 kΩ). Starting at frequencies of 200 kHz, high R_{Hy} values effect in addition to the hysteresis also the oscillator phase. Practical applications, however, require little phase response to receive a clear evaluation.

Application Example for a Proximity Switch

Coil data

pot core B65939-A-X22
coil former B65940-A-M1
Ø = 25 mm x 8.9 mm
L = 642 µH
n = 100 CuLS 30 x 0.05

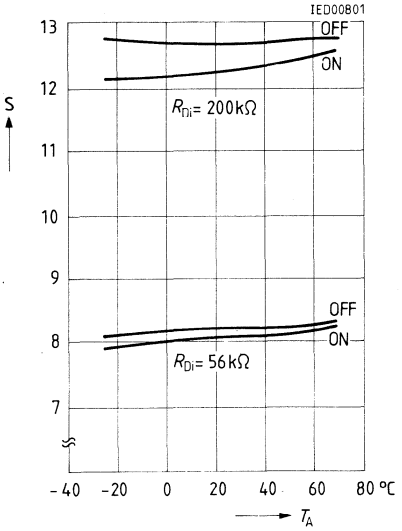
Measuring plate

30 mm x 30 mm x 1 mm, Fe

Circuitry

R_{Di} = 56 to 200 kΩ, metal layer
R_{Hy} = ∞
C_0 = 1500 pF, STYROFLEX
f = 162 kHz
} circuit 2

Switching distance versus ambient temperature



SIEMENS

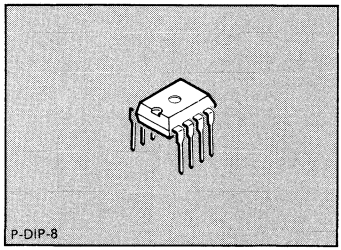
Proximity Switch

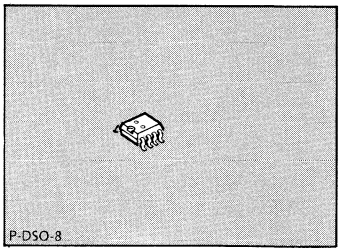
TCA 305
TCA 355

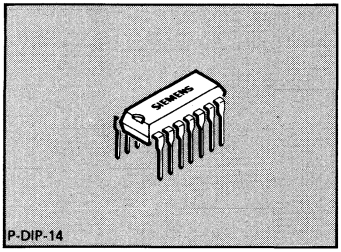
Bipolar IC

Features

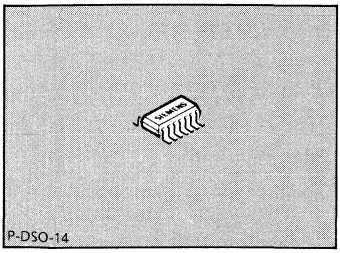
- Lower open-loop current consumption; $I_S < 1$ mA
- Lower output saturation voltage
- The temperature dependence of the switching distance is lower and compensation of the resonant circuit *TC* (temperature coefficient) is easier
- The sensitivity is higher, so that larger switching distances are possible and coils of a lower quality can be used
- The switching hysteresis remains constant as regards temperature, supply voltage and switching distance
- The TCA 305 even functions without external integrating capacitor. With an external capacitor (or with RC combination) good noise immunity can be achieved
- The outputs are temporarily short-circuit proof (approx. 10 s to 1 min depending on package)
- The outputs are disabled when $V_S <$ approx. 4.5 V and are enabled when the oscillator stabilizes (from $V_{S\,min} = 5$ V)
- Higher switching frequencies can be obtained
- Miniature package


P-DIP-8


P-DSO-8



P-DIP-14


P-DSO-14

Type	Ordering Code	Package
TCA 305 A	Q67000-A2291	P-DIP-14
TCA 305 G	Q67000-A2305	P-DSO-14 (SMD)
TCA 355 B	Q67000-A2443	P-DIP-8
TCA 355 G	Q67000-A2444	P-DSO-8 (SMD)

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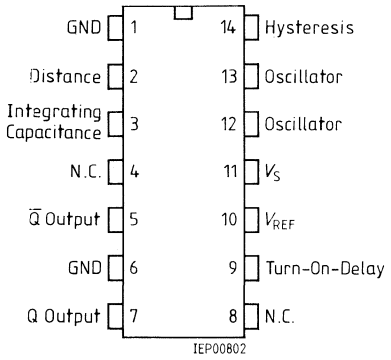
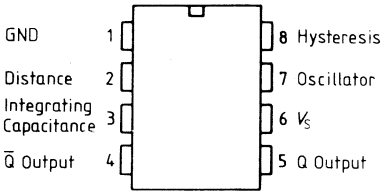
Pin Configurations (top view)

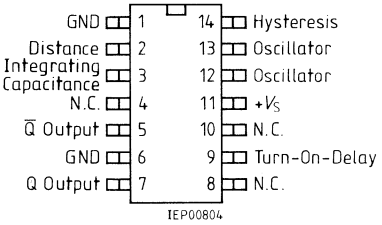
TCA 305 A



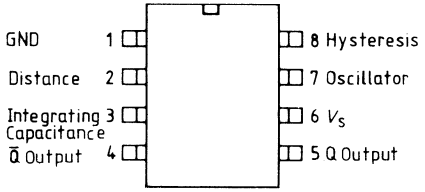
TCA 355 B



TCA 305 G



TCA 355 G



The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

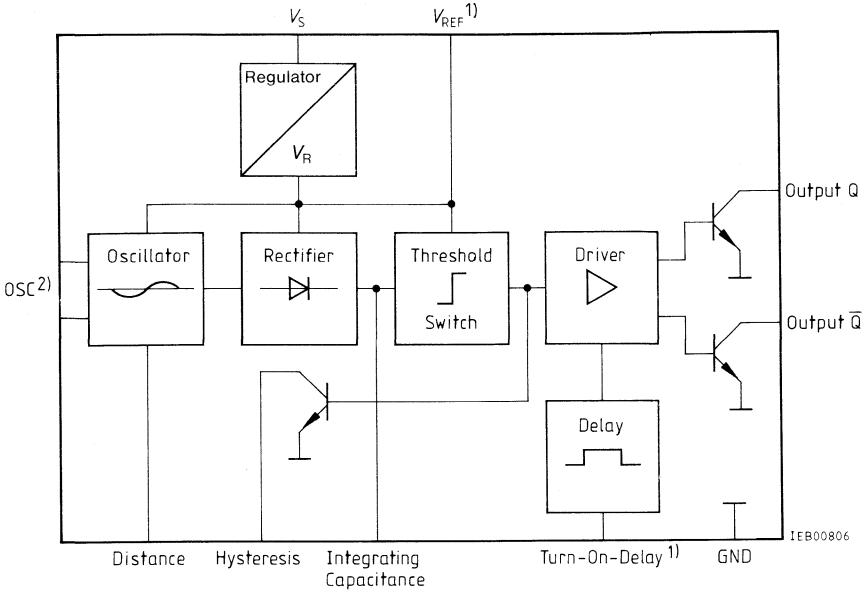
Operation Schematic: see TCA 205

The types TCA 305 and TCA 355 have been developed from the type TCA 205 and are outstanding for the following characteristics:

Logic Functions

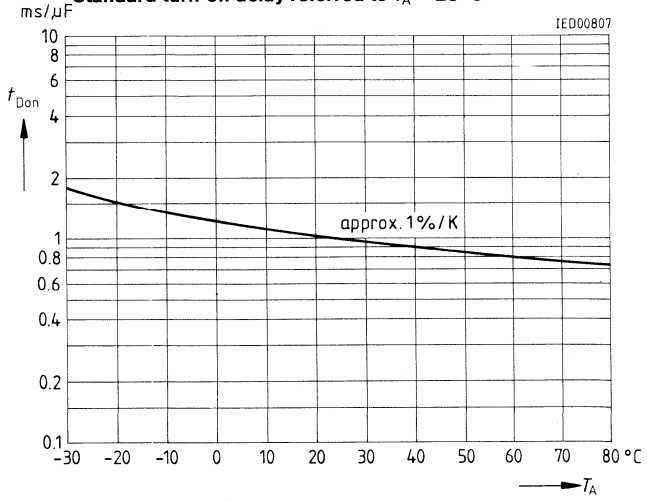
Oscillator	Outputs	
	Q	$\overline{Q}$
not damped	H	L
damped	L	H

Block Diagram



1) TCA 305 only
2) Connected internally in case of TCA 355

Standard turn-on delay referred to $T_A = 25\,°C$



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Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	35	V
Output voltage	V_Q	35	V
Output current	I_Q	50	mA
Distance, hysteresis resistance	R_{DI}, R_{Hy}	0	Ω
Capacitances	C_I, C_D	5	µF
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TCA 305 A	$R_{th\ SA}$	85 (135)[2]	K/W
TCA 305 G	$R_{th\ SA}$	140 (200)[2]	K/W

Operating Range

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	5 to 30[3]	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V, $T_A = -25$ °C to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Open-loop current consumption	I_S		0.6	0.9 (1.0)[2]	mA	outputs open
Reference voltage[1]	V_{REF}		3.2		V	$I_{REF} < 10$ µA
L-output voltage per output	$V_{Q\,L}$		0.04	0.15	V	$I_{Q\,L} = 5$ mA
	$V_{Q\,L}$		0.10	0.35	V	$I_{Q\,L} = 25$ mA
	$V_{Q\,L}$		0.22	0.75	V	$I_{Q\,L} = 50$ mA
H-output current per output	$I_{Q\,H}$			10	µA	$V_{Q\,H} = 30$ V
Threshold at 3	$V_{S\,3}$		2.1		V	
Hysteresis at 3	V_{Hy}	0.4	0.5	0.6	V	
Turn-on delay[1]	$t_{D\,ON}$	−25%	600	−25%	ms/µF	$T_A = 25$ °C
Switching frequency w/o C_I	f_S			5	kHz	

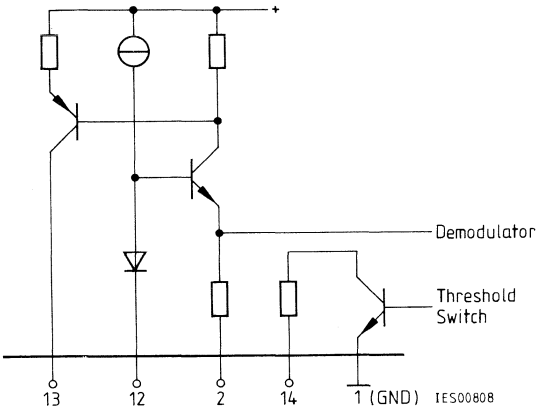
[1] TCA 305 only

[2] Values in parenthesis apply to TCA 355 only

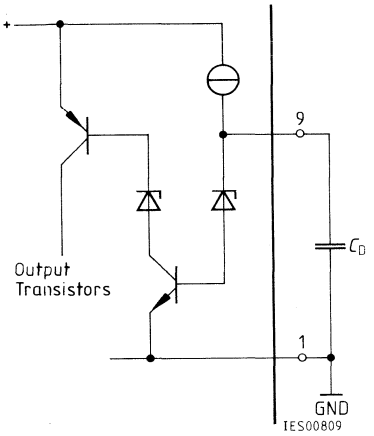
[3] Operation at voltages less than 5 V (between approx. 2.5 and 5 V) is possible, if V_{REF} is connected to V_S. In this case V_{REF} is no longer internally stabilized. Additionally, the pin "turn-on delay" is to be applied as follows: If no turn-on delay is needed, this pin has to be connected to V_S. If, however, a turn-on delay is required, the charge current for D_D has to be adjusted with an external resistor between this pin and V_S (recommended value 390 kΩ).

Schematic Circuit Diagrams

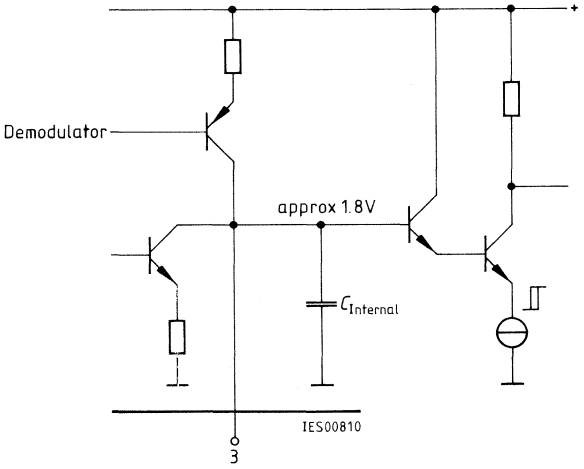
Oscillator



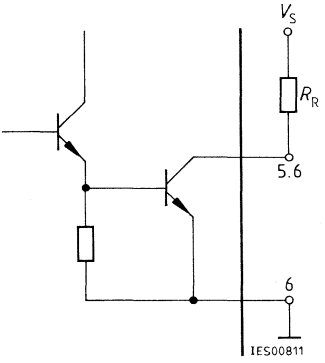
Turn-on delay for TCA 305 A; G



Integrating capacitor



Outputs



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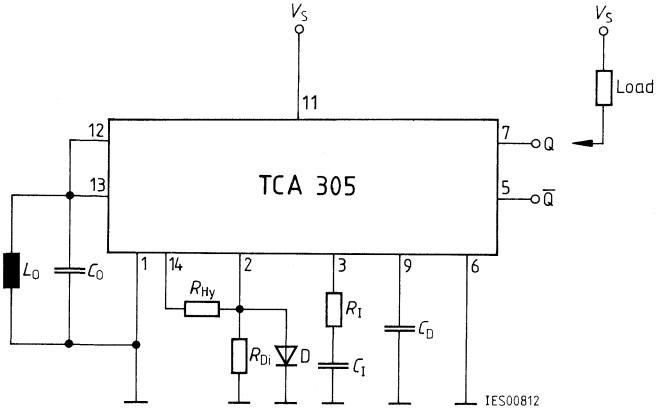
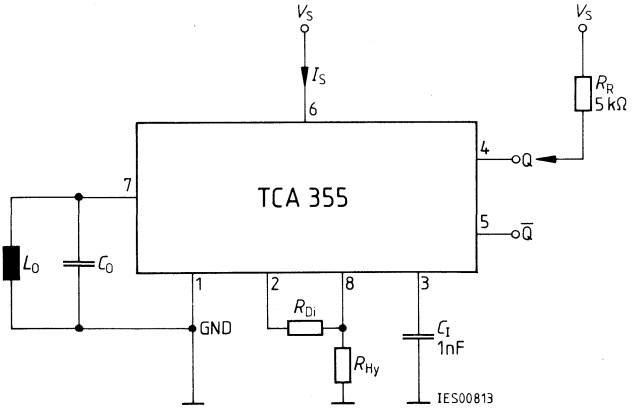
Application Circuits





L_0, C_0	Resonant circuit
R_{Hy}	Hysteresis adjustment
R_{Di}	Distance adjustment
D	Temperature compensation of the resonant circuit; possibly with series resistance for the purpose of adjustment. The diode is not absolutely necessary. Whether it is used or not depends on the temperature coefficient of the resonant circuit.
R_I; C_I	Integration element. At pin 3 (integrating capacitance) we recommend a capacitor of typ. 1 nF. To increase noise immunity this capacitor can be substituted by an RC circuit with, e.g., $R_I = 1$ MΩ and $C_I = 10$ nF.
C_D	Delay capacitor

Dimensioning examples in accordance with CENELEC Standard (flush)

	M 12	M 18	M 30
Ferrite pot core	M33 (7.35x3.6) mm	N22 (14.4x7.5) mm	N22 (25x8.9) mm
Number of turns	100	80	100
Cross section of wire	0.1 CuL	20x0.05	10x0.1
L_0	206 µH	268 µH	585 µH
C_0 (STYROFLEX®)	1000 pF	1.2 nF	3.3 nF
f_{OSC}	appr. 350 kHz	appr. 280 kHz	appr. 115 kHz
Sn	4 mm	8 mm	15 mm
R_A (Metal)	8.2 kΩ + 330 Ω	33 kΩ	22 kΩ + 2.7 kΩ
C_D	100 nF	100 nF	100 nF

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SIEMENS

IC for Inductive Proximity Switches with Short-Circuit Protection

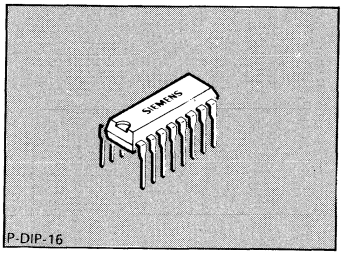
TCA 505

Preliminary Data

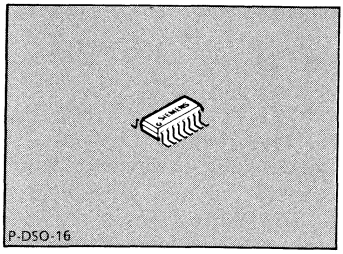
Bipolar IC

Features

- Wide supply voltage of 3.1 to 4.5 V and 4 to 40 V
- Low current consumption of less than 0.8 mA
- Integrated output stage for up to 60 mA output current
- Shortcircuit and overload protection of output stages and external components
- Temperature response of the IC compensates that of the coil
- High noise immunity
- High switching frequencies up to 5 kHz
- Useful extra functions
- Suitable for two-wire AC proximity switches
- Temperature range −40 to 125 °C



P-DIP-16


P-DSO-16

Type	Ordering Code	Package
▼ TCA 505 A	Q67000-A8278	P-DIP-16
▼ TCA 505 G	Q67000-A8279	P-DSO-16 (SMD)

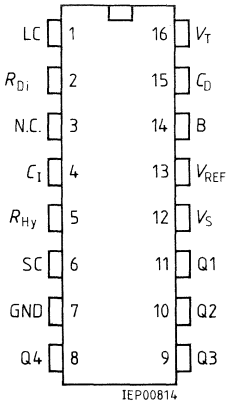
▼ New type

Besides its basic functions (oscillator, demodulator and threshold switch), the bipolar monolithic IC TCA 505 includes a number of useful extra functions that enable high-grade, inductive proximity switches to be designed for an attractive price/performance ratio and with space savings.

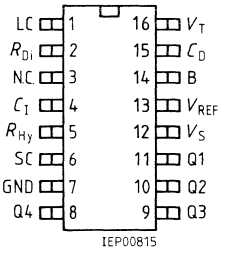
Compared to earlier ICs for inductive proximity switches temperature drift, noise immunity and the switching frequency of the IC have been improved.

Pin Configurations
(top view)

P-DIP-16



P-DSO-16

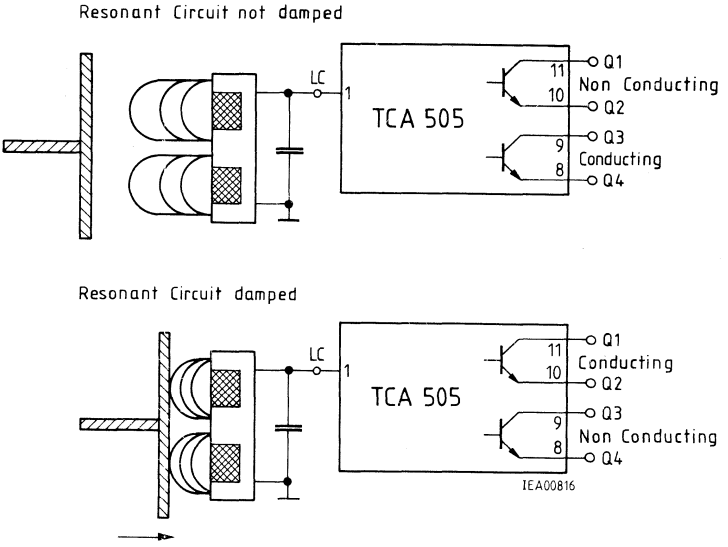


Pin Definitions and Functions

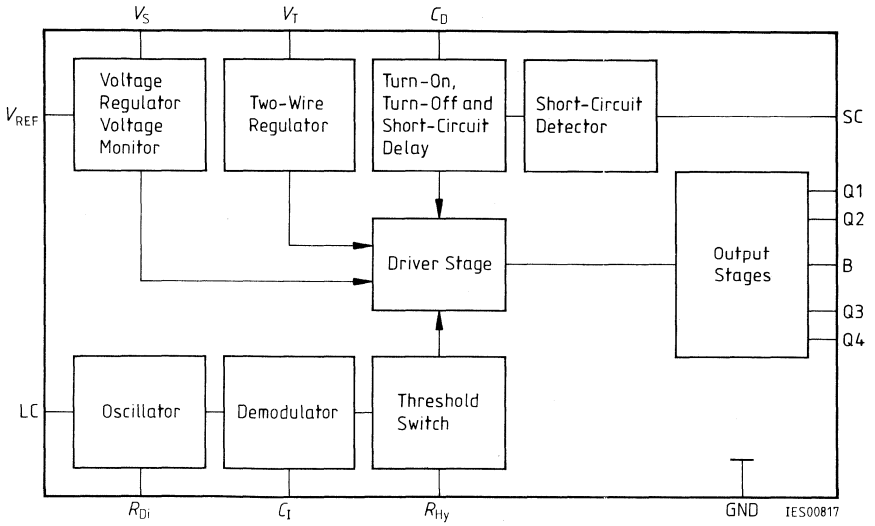
Pin	Symbol	Function
1	LC	Oscillator
2	R_{Di}	Distance
3	N.C.	Not connected
4	C_I	Integrating capacitance
5	R_{Hy}	Hysteresis
6	SC	Short-circuit detector
7	GND	Ground
8	Q4	Output
9	Q3	Output
10	Q2	Output
11	Q1	Output
12	V_S	Supply voltage
13	V_{REF}	Reference voltage
14	B	Base Output Transistors
15	C_D	Turn-on delay / Short-circuit delay
16	V_T	Two-wire regulator

Functional Description and Application

Operation Schematic



Block Diagram



Functional Description

This circuit is used to design inductive proximity switches. The resonant circuit of the LC oscillator is implemented with an open half-pot ferrite and a capacitor in parallel (pin LC). If a metallic target is moved closer to the open side of the half-pot ferrite, energy is drawn from the resonant circuit and the amplitude of the oscillation is reduced accordingly. This change in amplitude is transmitted to a threshold switch by means of a demodulator and triggers the outputs **(see operation schematic)**.

By means of an external distance resistor on the oscillator (pin R_{Di}) it is possible to set the switching distance within wide limits, the optimal distances being 0.1 to 0.6 of the diameter of the half-pot ferrite, although both of these parameters can be exceeded. The circuit also enables the setting of a path hysteresis by switching of the external distance resistor via pin R_{Hy} **(see application circuit 1)**.

There are two antiphase output stages (Q1 / Q2 and Q3 / Q4) for max. 50 mA. The output transistors are driven in a floating state thus providing the user with optimal flexibility for evaluation of the output signals. It is therefore possible to use the output transistors either as emitter follower, open-collector, as a current source or in push-pull operation. When pin B is connected to V_{REF}, Q2 and Q4 can be used between 0 V and V_{REF}. The maximum base voltage of the output transistors can be set on pin B. If B is connected to V_{REF}, any constant current up to 50 mA can be set on the outputs by means of resistors on Q2 or Q4 **(see application circuits 2 and 3)**.

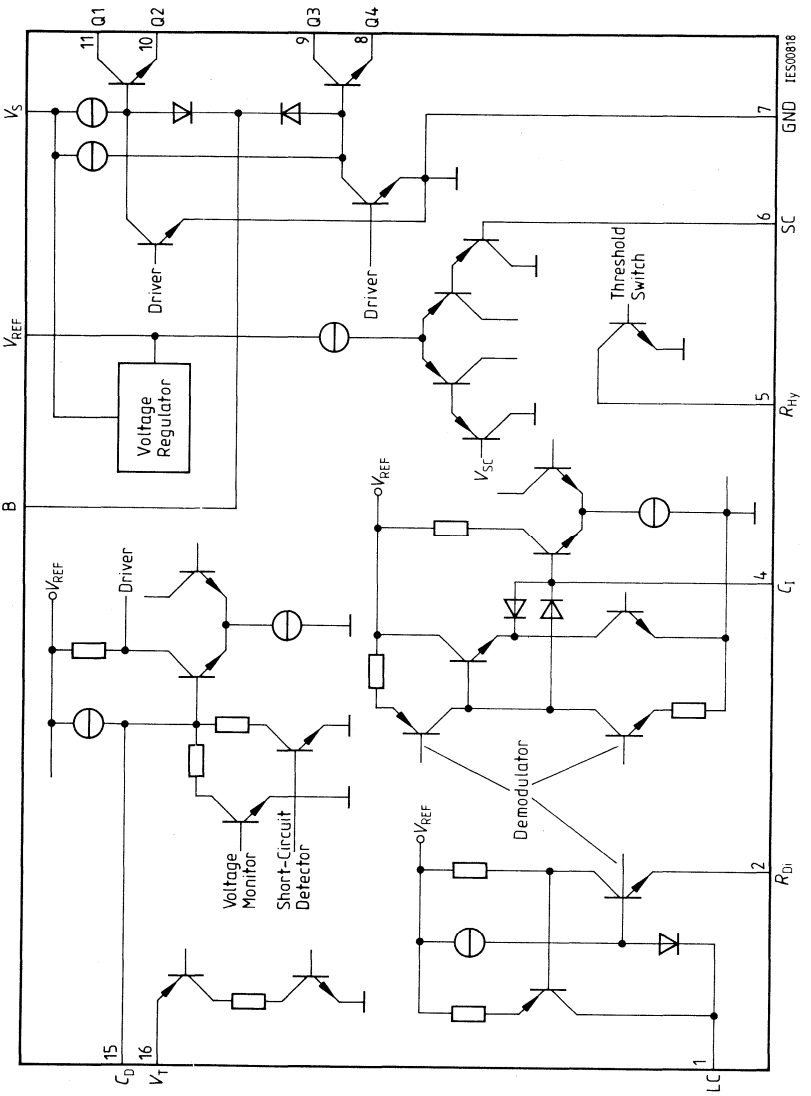
Q1 through Q4 and also additional external output transistors can be protected against destruction by short-circuit or overload. This is the purpose of pin SC which turns off the output transistors periodically in the presence of overload.

By means of a capacitor on C_D it is possible to set the response delay and the turn-off time of short-circuit protection. The same capacitor also defines the turn-on delay of the output stages when the supply voltage is applied, whereby the output stages are inhibited during buildup of the oscillator. Finally C_D produces a turn-off delay of the output stages to prevent the turn-on delay from running its full length at brief voltage dips on V_S.

A switching regulator is incorporated for the voltage supply of the circuit when it is used as a two-wire AC proximity switch, and this is activated when pin V_T is connected to V_S. The circuit has a stabilized voltage of approx. 2.9 V that is brought out on pin V_{REF}.

Supply-voltage range: The operating range in normal operation is between 4 and 40 V. If pin V_{REF} is connected to V_S, the circuit is operating between 3.1 and 4.5 V. In this case, however, V_{REF} is no longer internally stabilized, i.e. the analog IC functions depend on the operating voltage.

Circuit Diagram (simplified)



Pin Functions

Pin 1; LC

The resonant circuit of the proximity switch is connected between LC and ground.

Pin 2; R_{Di}

A resistor between this pin and ground sets the current in the oscillator circuit. The greater the value of the resistor, the smaller is the current feed from the oscillator into the resonant circuit and the greater therefore is the switching distance. The greater the Q of the resonant circuit, the greater is the value of the distance resistor necessary for setting a certain switching distance.

Pin 4; C_I

C_I can remain open; if high noise immunity is to be achieved however, this pin should be provided with a series RC element (R_I, C_I). If pin C_D is not used, a correctly dimensioned RC element on this pin will also prevent any erroneous pulses on the output when the supply voltage is turned on **(see application circuit 1)**.

Pin 5; R_{Hy}

Depending on the status of the circuit, R_{Hy} will be high-impedance or low-impedance to ground (open collector). If the distance resistance (see R_{Di}) is split into two resistors R_{Di} and R_{Hy}, a distance hysteresis can be set by means of R_{Hy}. If series hysteresis is applied, R_{Hy} is connected in series with R_{Di} or shorted. If parallel hysteresis is applied, R_{Hy} is connected in parallel with R_{Di} or made high-impedance **(see application circuit 1)**.

Pin 6; SC

SC serves for short-circuit sensing in the output circuit that is to be protected. The current can be sensed referred to ground or V_S. The current sensing is made by a dedicated resistor in the output circuit. For a voltage drop ≥ 0.3 V across V_S and SC or across ground and SC, all outputs are turned off after the turn-off delay (brief glitches on the outputs or the charging of line capacitances therefore do not trigger the short-circuit protection). After a pause about 200 times the turn-off delay, the outputs turn on again. If the short-circuit is still present, the turn-off cycle will start up anew.

Both the internal output stages and externally connected output stages can be protected against sustained short-circuits or overload.

A limiting of the output current is an externally connected output stage during the turn-off delay must be ensured. Normally the current limiting by the ß of the output transistor is sufficient, meaning that no further circuit devices are called for **(see application circuits)**. The outputs Q1 to Q4 are already internally protected against overcurrent so that, in the case of a short-circuit, the current will not exceed 250 mA.

In order to prevent thermal overloads, the current-conducting output is to be connected to pin SC **(see application circuit 4)**.

Pins 8, 9, 10, 11; Outputs Q1, Q2, Q3, Q4

Q1 is the open collector, Q2 the open emitter of one output transistor, Q3 the open collector and Q4 the open emitter of the second output transistor in antiphase with the first output transistor **(see operation schematic)**. Q1 and Q3 or Q2 and Q4 can be connected in parallel as required. The function of the outputs is ensured when the emitter potential of the output transistors (Q2, Q4) is between 0 V and the voltage on pin B. If B is not connected, the operating range of Q2 and Q4 extends to approx. V_S−2 V. For current setting on the outputs, **see pin B**.

Pin 12; V_S

Outputs Q1 through Q4 are inhibited as long as the voltage on V_S is below approx. 3.6 V. They are enabled between approx 3.6 and 4 V, the basic function of the circuit is then ensured. During the turn-on and turn-off of V_S there are consequently no undesirable static states. The operating data and characteristics apply upwards from 4 V. See pin C_D for the avoidance of erroneous pulses during oscillator buildup.

Pin 13; V_{REF}

The internal stabilized voltage of the IC of approx. 2.9 V appears on this pin. A capacitor can be connected between V_{REF} and ground to improve the noise immunity of the overall circuit function. If V_{REF} is connected to V_S, it is possible to operate the circuit in a supply-voltage range of 3.1 through 4.5 V. In this case V_{REF} is no longer stabilized. The analog functions of the circuit e.g. switching distance, however, are then dependent on the supply voltage.

Pin 14; B

This pin serves for limiting the base voltage of the internal output-stage transistors. If this pin is connected to V_{REF} for example, it is possible to set a constant output current (I_Q = V_{REF} / external resistor) that is independent of the supply voltage by means of an external resistor across Q2 (or Q4) and ground (watch out for power dissipation!).

Pin 15; C_D

A capacitor on this pin delays the activation of the outputs after the supply voltage is applied (turn-on delay). In this way erroneous pulses are prevented on the output during buildup of the oscillator.

If V_S falls to less than 3.6 to 4 V, the outputs are not inhibited until after a turn-off delay time, this also being determined by C_D. In this way the delayed turn-on operation described above is suppressed if there are just short glitches (voltage dips) on V_S. This is of particular advantage for large core diameters, because in such cases a relativity long turn-on delay has to be selected and the delayed twin-on operation would otherwise be activated each time there was a brief voltage dip.

The capacitor C_D also sets the turn-off delay and the pause duration in short-circuit operation. The sample / pause ratio is approx. 1:200 **(see pin SC)**.

If these functions can be dispensed with, C_D can remain open.

Pin 16; V_T

If this pin is connected to $+V_S$, the supply voltage of the IC (when used as a two-wire proximity switch) can be generated by switching the outputs. The quiescent current can then be kept low. This mode is primarily suitable for AC switches with power supply by phase-control.

The switching of the outputs is made in a V_S range of 6 to 8 V. At 8 V the outputs are turned on, until V_S falls to 6 V. At 6 V the outputs are inhibited, until V_S again reaches 8 V. In this mode V_S should not exceed 14 V or fall below 4 V.

Absolute Maximum Ratings

$T_A = -40\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Supply voltage	V_S	−0.3	42	V	
Output voltages B open B connected	V_{Q1}; V_{Q3} V_{Q2}; V_{Q4} V_{Q2}; V_{Q4}	−1 −1 −1	41 V_S+1 V_B	V V V	V_{Q2}; $V_{Q4} \leq V_S$ V_{Q2}; V_{Q1}; V_{Q4} $< V_{Q3}$
Output currents	I_{Q1}; I_{Q3} $-I_{Q2}$; $-I_{Q4}$	0 0	60 60	mA mA	does not apply to shortcircuit
Voltage on V_T	V_T	−0.3	14	V	
Current on V_{REF}	$-I_{REF}$	0	100	µA	
Voltage on SC	V_{SC}	0	V_S	V	
Current from R_{Di}	$-I_{RDi}$	0	2	mA	
Current to R_{Hys}	I_{RHy}	0	2	mA	
Voltage on B	V_{SB}	−0.3	V_S	V	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance (system – air)	$R_{th\ SA}$ $R_{th\ SA}$		81 110	K/W K/W	P-DIP-16 P-DSO-16
Junction temperature	T_j T_j		125 150	°C °C	 max. 70.000 h
Capacitor	C_V		50	nF	applies to short-circuit at the TCA 505 only

Operating Range

Supply voltage	V_S	4 3.1	40 4.5	V V	 $V_{REF} = V_S$
Ambient temperature	T_A	−40	125	°C	
Distance and Hysteresis resistance R_{Di} and R_{Hy} in series R_{Di} and R_{Hy} parallel	 R_{Di} R_{Hy} R_{Di}/R_{Hy}	 300 0 300		 Ω Ω Ω	
Output voltage on Q2, Q4 B open B connected	 V_{Q2}; V_{Q4} V_{Q2}; V_{Q4}	 −0.3 −0.3	 V_S-2 V_B	 V V	

Only the circuitry provided for passive components may be connected to pins LC, R_{Di}, C_I, C_D

Characteristics

4 V ≤ V_S ≤ 40 V; T_A = −40 °C to 125 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Power Supply (V_S)						
Current consumption Normal mode (S1 = S2 = OFF) Two-wire operation S1 = ON, S2 = OFF 4 V ≤ V_S ≤ 12 V	 I_S I_S		 550 600	 750 800	 µA µA	 1 1
Turn-on threshold (outputs active) S1 = OFF	V_{TON1}			4	V	1
Turn-off threshold (outputs disabled) S1 = OFF	V_{TOFF1}	3.0	3.6		V	1
Hysteresis $V_{Ton1} - V_{Toff1}$ S1 = OFF	ΔV_{Hy1}		50		mV	1
Oscillator (LC, R_{Di})						
Oscillator frequency	f_{OSC}			3	MHz	1
Oscillator amplitude	A_{OSC}		0.8		V_{pp}	1
Demodulator, Threshold Switch (C_I, R_{Hy})						
Threshold on C_I	V_{CI}		2		V	1
Hysteresis on C_I	V_{HyCI}		0.8		V	1
Current in C_I	I_{CI}		7		µA	1
Current from C_I	$-I_{CI}$		6		µA	1
Switching frequency C_I < 50 pF	f_S		5		kHz	1 (L = 70 µH)
Reference Voltage (V_{REF}); Base Output Transistors						
Reference voltage I_{REF} = 0 to 100 µA	V_{REF}	2.65	2.9	3.10	V	
Offset voltage $V_B = V_{Q2,4}$ $V_B = V_{REF}$; $I_{Q2,4}$ = 5 mA	V_{OB}		125	160	mV	1

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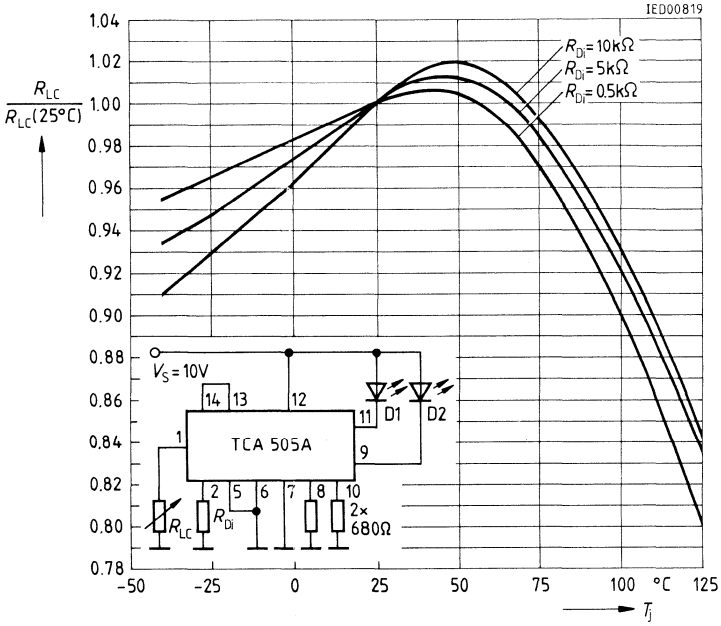
Characteristics (cont'd)

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Circuit
Two-Wire Regulator (V_T)						
Turn-on threshold (outputs active) S1 = ON	V_{TON2}	6.6	8	9.4	V	1
Turn-on threshold (outputs disabled) S1 = ON	V_{TOFF2}	5.0	6	7.0	V	1
Hysteresis $V_{Ton2}-V_{Toff2}$, S1 = ON	ΔHy_2	1.6	2	2.4	V	1
Turn-On, Turn-Off and Short-Circuit Delay (C_D)						
Turn-on delay S1 = OFF	t_{DON}	0.48	0.65	0.82	ms/nF	2
Turn-off delay S1 = OFF; $V_S \geq 3.6$ V	t_{VA}	17.0	25	34.0	µs/nF	2
Shortcircuit turn-off delay S1 = OFF	t_{SC}	1.70	2.5	3.40	µs/nF	2
Shortcircuit pause S1 = OFF	t_P	0.35	0.5	0.65	ms/nF	2
Outputs (Q1, Q2, Q3, Q4)						
Residual voltage Q1-Q2, Q3-Q4 SQ2 0-1 = ON, SQ4 0-1 = ON S1 = OFF	V_{QRes}					
I_Q = 5 mA	V_{QR}		0.10	0.15	V	1
I_Q = 60 mA	V_{QR}		0.5	1.0	V	1
I_Q = 60 mA	V_{QR}	$V_S-2.2$	$V_S-1.8$		V	1
Reverse current on Q1,3	I_{QR}			10	µA	
Residual current on Q2,4*) Q2,4 conducting but Q1,3 open	I_{Qres}			50	µA	1
In case of short-circuit output current	I_{QSC}		200	250	mA	1
Shortcircuit Detector (SC)						
Trigger level ref. to V_S, S1 = OFF	V_{SCS}	0.255	0.3	0.345	V	1
Trigger current S1 = OFF	I_{SCS}			30	µA	1
Trigger level ref. to ground S1 = OFF	V_{SCO}	0.255	0.3	0.345	V	1
Trigger current S1 = OFF	$-I_{SCO}$			6	µA	1

Diagrams

Temperature Response of Switching Point



Resistor R_{LC} is set in each case so that the TCA 505 A just switches from D2 to D1. In this way the TCA 505 A, together with a suitably dimensioned resonant circuit, can form a proximity switch that exhibits a very good temperature coefficient (± 2.5%) over the entire temperature range and without any kind of extra external wiring.

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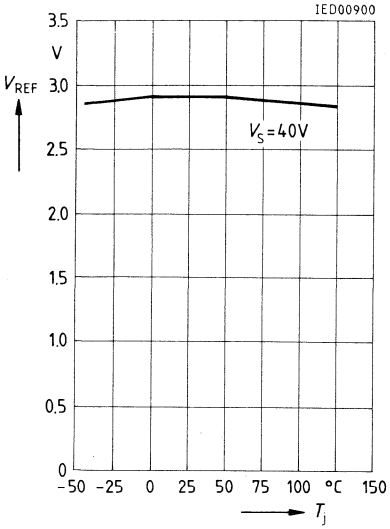
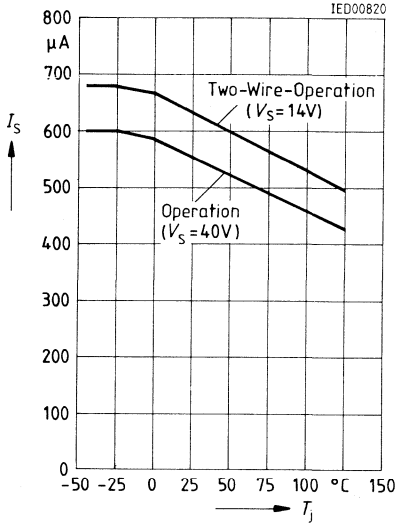
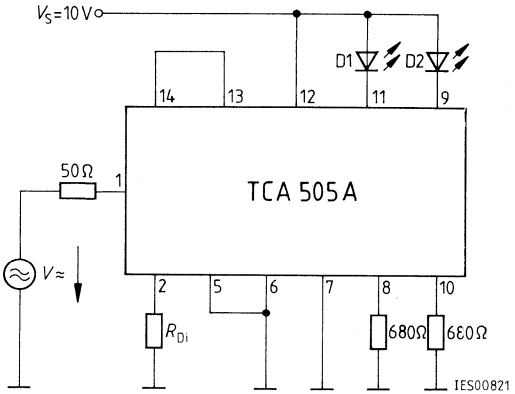
Diagrams

Reference Voltage versus Junction Temperature T_j

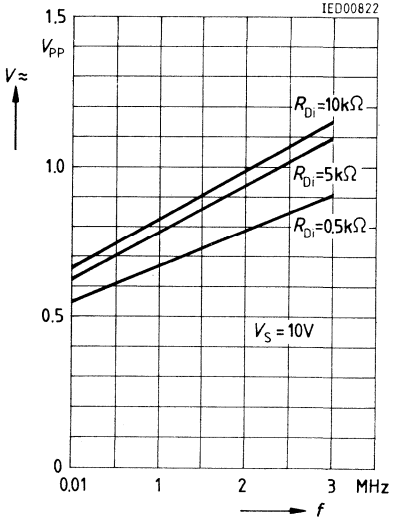


Current Consumption versus Junction Temperature T_j

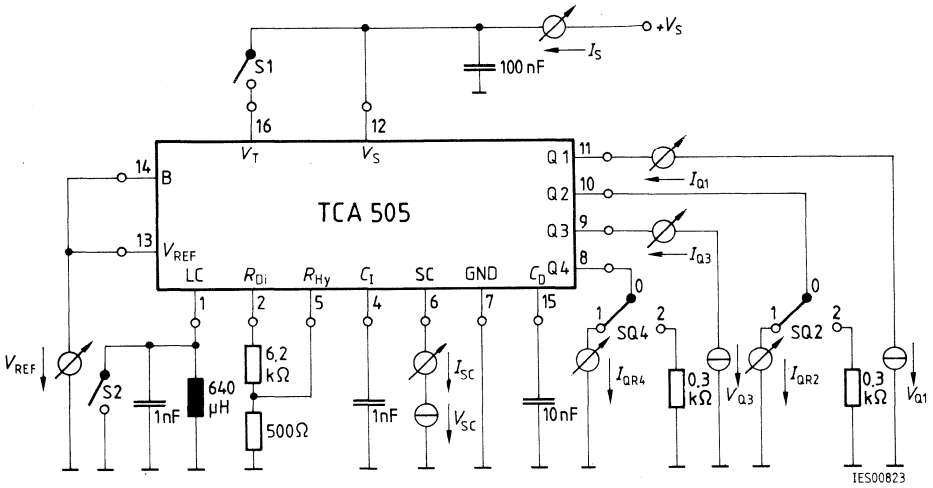




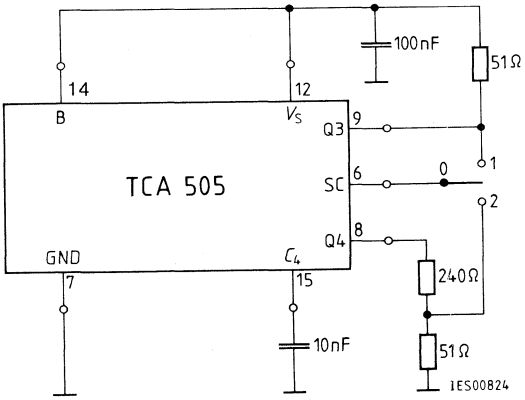
Switching Amplitude versus Frequency f



Test Circuit 1

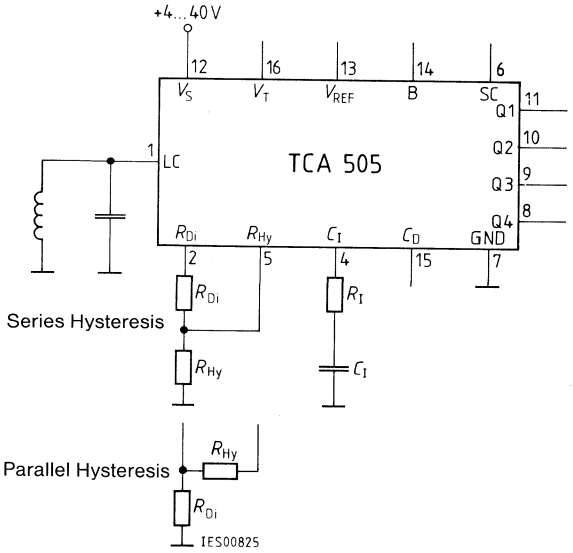


Test Circuit 2



Application Circuit 1

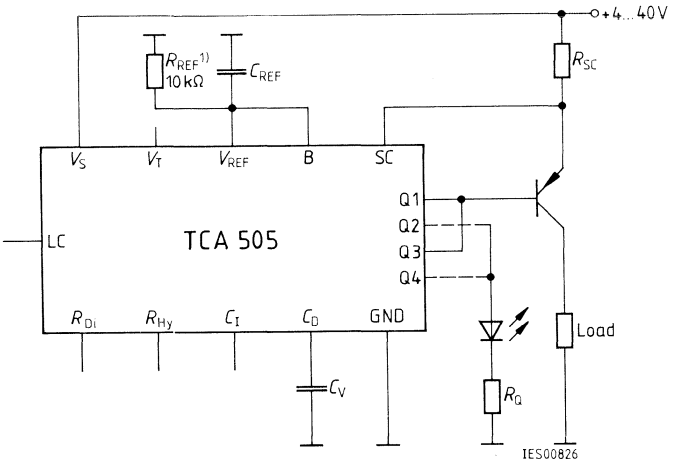
Input Circuitry (Use of pins LC, R_{Di}, R_{Hy}, C_I)



For explanation see under "Pin Functions"

Application Circuit 2

Output Circuitry (Use of pins V_{REF}, B, SC, Q1 through Q4, C_D)



P switch, short-circuit-proof, LED indicator, configurable as normally closed or normally open

Short-circuit-current sampling: $R_{SC} = \dfrac{0.3\ V}{\text{max. load current}}$

Constant base current: [1] $R_Q = \dfrac{2.9\ V - V_{LED}}{\text{max. base current}}$

For dimensioning of C_D **see characteristics.** C_D is usually between 1 and 10 nF. Filtering of V_{REF} is for noise immunity. C_{REF} can be 10 nF for example.

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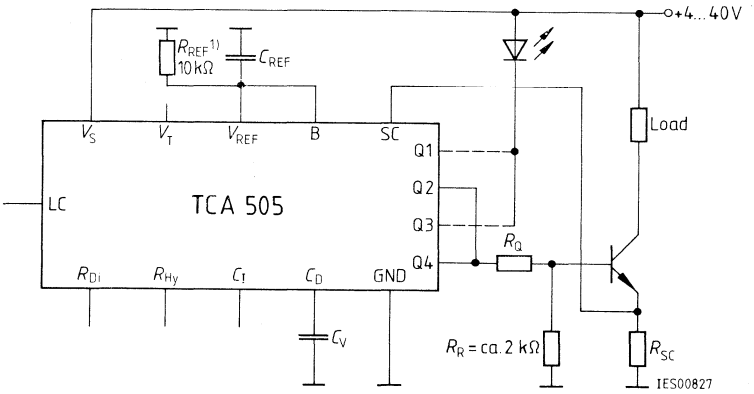
[1] When $I_Q > 10$ mA, a resistor R_{REF} on pin V_{REF} will improve the constant current operation.

Application Circuit 3

Output Circuitry (Use of pins V_{REF}, B, SC, Q1 through Q4, C_D)



N switch, short-circuit-proof, LED indicator, configurable as normally closed or normally open

Short-circuit-current sampling: $$R_{SC} = \frac{0.3\ V}{\text{max. load current}}$$

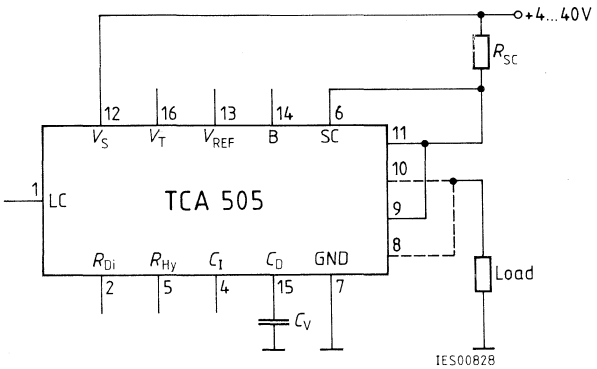
Constant base current:[1]) $$R_Q = \frac{2\ V}{\text{max. base current} + I_{RR}}$$

For dimensioning of C_D **see characteristics.** C_D is usually between 1 and 10 nF. Filtering of V_{REF} is for noise immunity. C_{REF} can be 10 nF for example. R_{REF} serves for discharging residual current of outputs Q2,4.

[1]) When $I_Q > 10$ mA, a resistor R_{REF} on pin V_{REF} will improve the constant current operation.

Application Circuit 4

Output Circuitry (Use of pins SC, Q1 to Q4, C_D)



P switch, short-circuit-proof, configurable as normally closed or normally open

Short-circuit-current sampling: $R_{SC} = \dfrac{0.3\ V}{\text{max. load current}}$

During the sampling time, the short-circuit current within the IC is limited to a maximum of 250 mA. For dimensioning of C_V, **see characteristics**. C_D is usually between 1 and 10 nF.

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Selector Guide

Type	Package	Features	Temperature range	Page
SAE 81C52 P SAE 81C52 G	P-DIP-16 P-DSO-20 (SMD)	Static CMOS RAM 256 x 8 bits SAB 8051-compatible	–40...85 °C	833
SAE 81C54 P	P-DIP-16	Static CMOS RAM 512 x 8 bits SAB 8051-compatible	–40...110 °C	840
SAE 81C80 A	PL-CC-44 (SMD)	Dual Port RAM 504 x 8 bits Multiprocessor system	–40...85 °C	846
SDE 2506 A2	P-DIP-8	EEPROM 128 x 8 3-line bus	–40...110 °C	866
SDE 2526 A2	P-DIP-8	EPPROM 258 x 8 I^2C bus	–40...110 °C	874

256 x 8 Bit Static CMOS RAM NMOS-Compatible

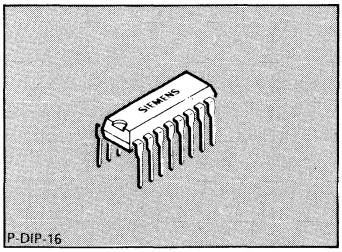
SAE 81C52

Preliminary Data

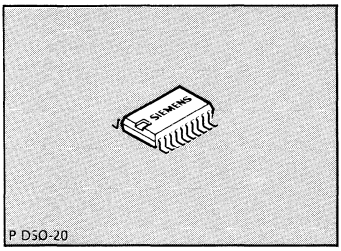
CMOS IC

Features

- 256 x 8-bit organization
- Standby mode
- Compatible with the NMOS and CMOS versions of the microprocessor/microcontroller families SAB 8086, SAB 8051
- Very low power dissipation
- Data retention up to $V_{DD} \geq 1$ V
- Three different chip select inputs for two chip select modes
- No increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range −40 °C to 110 °C



P-DIP-16



P DSO-20

Type	Ordering Code	Package
SAE 81C52 P	Q67100-H9017	P-DIP-16
SAE 81C52 G	Q67100-H9015	P-DSO-20 (SMD)

The SAE 81C52 is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus interfaces directly to 8-bit microprocessors/microcontrollers without any timing or level problems, e.g. the families SAB 8086, SAB 8051.

All inputs and outputs are fully compatible with NMOS circuits, except CS 1. Data retention is ensured up to $V_{DD} \geq 1.0$ V. The SAE 81C52 has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD 0...AD 7) and the control lines ($\overline{WR}$, $\overline{RD}$, ALE, CS2, CS 3), or only the control lines $\overline{RD}$, $\overline{WR}$.

The power consumption is max. 5.5 µW in standby mode and max. 2.75 mW in operation. In standby mode, the power consumption will not increase if the controls inputs are on undefined potential.

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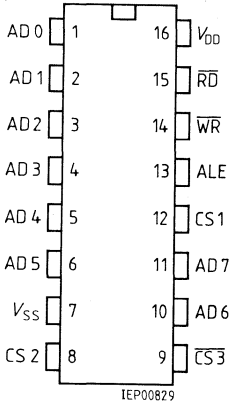
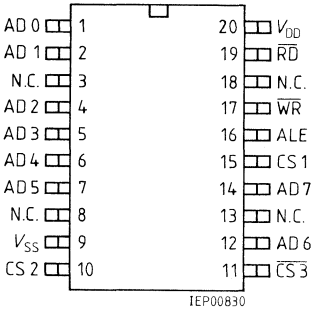
Pin Configurations
(top view)

SAE 81C52 P



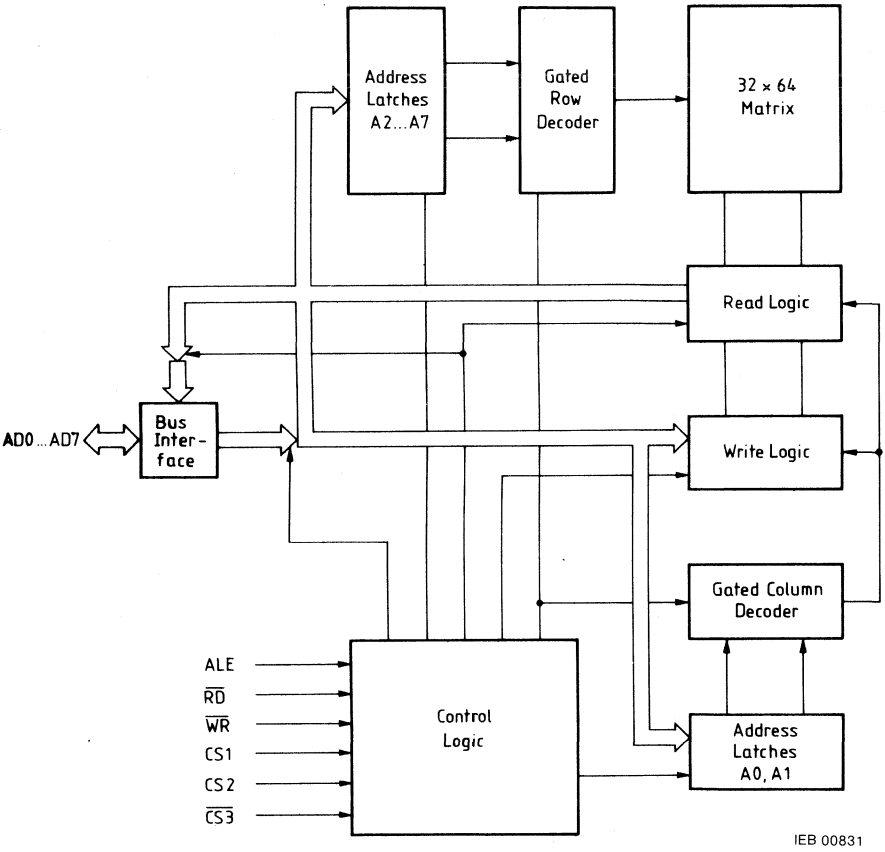
SAE 81C52G



Pin Definitions and Functions

SAE 81C52 G	SAE 81C52 P	Symbol	Function
Pin	**Pin**		
1, 2, 4, 5, 6 7, 12, 14	1...6 10, 11	AD 0...7	Address/data lines
15	12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17	14	$\overline{WR}$	Write enable
19	15	$\overline{RD}$	Read enable
20	16	V_{DD}	Power supply
9	7	V_{SS}	GND (0 V)
10	8	CS 2	Chip select 2; inhibits control inputs $\overline{RD}$, $\overline{WR}$
11	9	$\overline{CS 3}$	Counterpart to CS 2

Block Diagram



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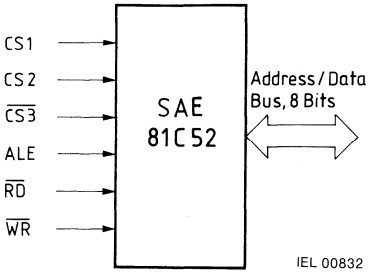
Logic Symbol



Truth Table

CS 1	CS 2	CS 3	ALE	RD	WR	AD 0...AD 7	Function
L	*	*	*	*	*	Floating (tristate)	Standby
H	X	X	H	H	H	Addresses to memory	Store addresses
H	H	L	L	L	H	Data from memory	Read
H	H	L	L	H	L	Data to memory	Write
H	L	X	L	X	X	Floating (tristate)	None
H	X	H	L	X	X	Floating (tristate)	None

*: Level = V_{SS} ... V_{DD}
X: Level = LOW or HIGH

Absolute Maximum Ratings (T_A = −40 to 110 °C)

Parameter	Symbol	Limit Values	Unit
Supply voltage referred to GND (V_{SS})	V_{DD}	0 to 6	V
All input and output voltages	V_{IM}	V_{SS} −0.3 V_{DD} +0.3	V V
Total power dissipation	P_{tot}	250	mW
Power dissipation for each output	P_Q	50	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55 to 125	°C
Thermal resistance			
system – air P-DIP-16	$R_{th\ SA}$	70	K/W
P-DSO-20	$R_{th\ SA}$	95	K/W

Operating Range

Supply voltage	V_{DD}	4.5 to 5.5	V
Ambient temperature	T_A	−40 to 110	°C

DC Characteristics

$T_A = -40\,°C$ to $110\,°C$; $V_{DD} = 4.25$ V to 5.5 V; $V_{SS} = 0$ V

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Standby supply current	I_{DD}		1	µA	$V_{DD} = 5.5$ V; $T_A = 25\,°C$; $V_{CS1} = 0$ V
Supply current	I_{DD}		3	mA	$\Delta t_{cyc} = 1$ µs; $V_{DD} = 5.5$ V; $C_L = 100$ µF
Standby voltage for data retention	V_{DD}	1.0		V	
L-input current (for each input)	I_{IL}		1	µA	$V_I = 0$ to V_{DD}
Output leakage current	I_{QLK}		1	µA	$V_Q = 0$ to V_{DD} tristate
L-input voltage	V_{IL}	V_{SS}	0.8	V	
H-input voltage	V_{IH}	2.2	V_{DD}	V	
L-output voltage	V_{QL}		0.4	V	$I_{QL} = 1$ mA
H-output voltage	V_{QH}	2.6		V	$I_{QH} = 1$ mA
L-input voltage CS1	V_{IL}	V_{SS}	1	V	
H-input voltage CS1	V_{IH}	$V_{DD}-1$	V_{DD}	V	

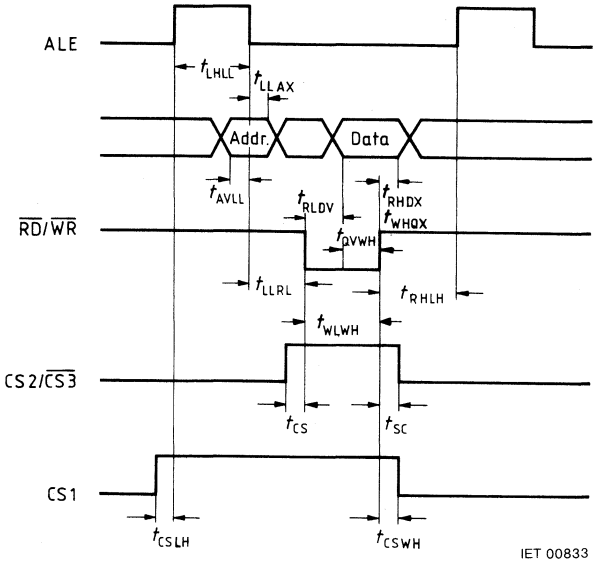
AC Characteristics

$T_A = -40\,°C$ to $85\,°C$[1]; $V_{DD} = 4.5$ V to 5.5 V; $V_{SS} = 0$ V

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
ALE pulse width	t_{LHLL}	100		ns
ALE LOW before $\overline{RD}$ LOW	t_{LLRL}	50		ns
$\overline{RD}$ HIGH before ALE HIGH	t_{RHLH}	18		ns
ALE LOW before $\overline{WR}$ LOW	t_{LLWL}	50		ns
$\overline{WR}$ HIGH before ALE HIGH	t_{WHLH}	18		ns
Address setup before ALE	t_{AVLL}	25		ns
Address hold after ALE	t_{LLAX}	50		ns
$\overline{WR}$ or $\overline{RD}$ pulse width	t_{WLWH}	250		ns
Data setup before $\overline{WR}$	t_{QVWH}	50		ns
Data hold after $\overline{WR}$	t_{WHQX}	30		ns
Data hold after $\overline{RD}$	t_{RHDX}		90	ns
Chip select (2, 3) before $\overline{RD}$, $\overline{WR}$	t_{CS}	50		ns
Chip select (2, 3) after $\overline{RD}$, $\overline{WR}$	t_{SC}	50		ns
Chip select 1 before ALE	t_{CSLH}	20		ns
Chip select 1 after $\overline{RD}$, $\overline{WR}$	t_{CSWH}	50		ns
Output delay time	t_{RLDV}		200	ns
Input capacitance to V_{SS} (for each input)	C_I		10	pF

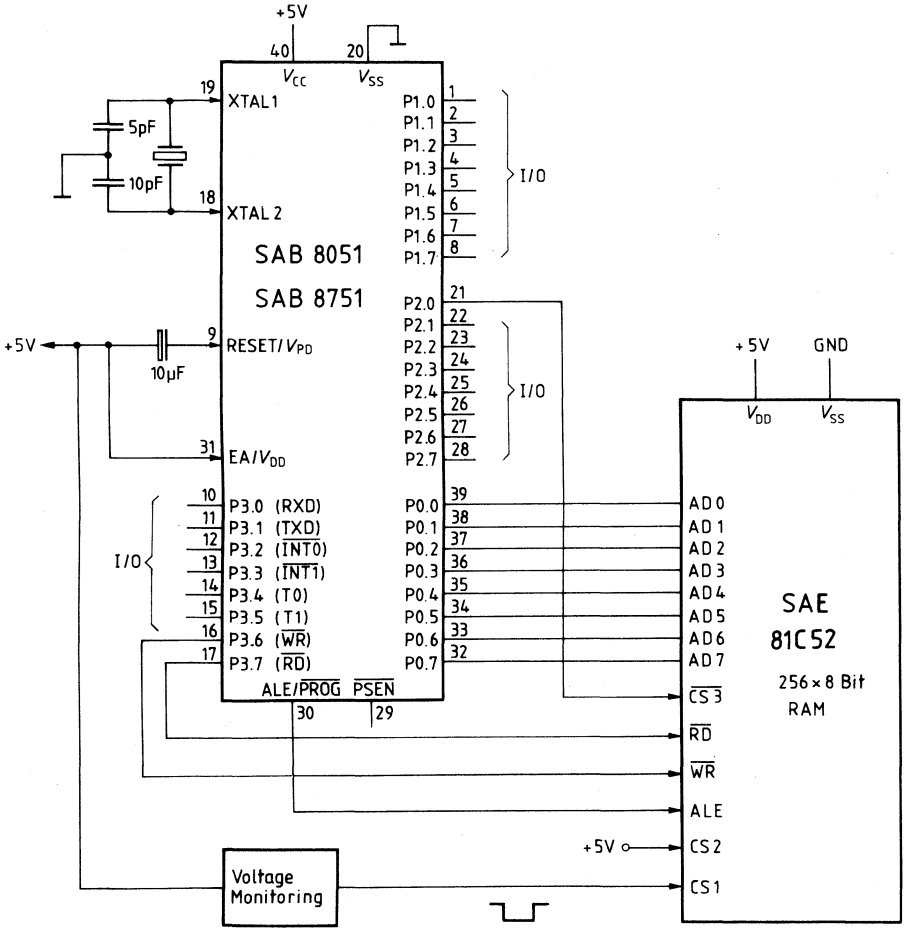
[1]) Values for applications up to 110 °C upon request

Timing Diagram



Application Circuit

SAE 81C52 with the µC SAB 8051

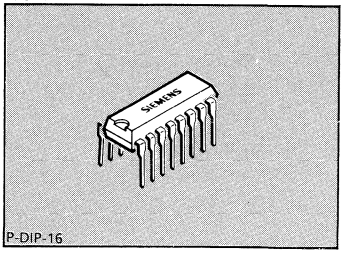


CMOS RAM

Preliminary Data **ACMOS IC**

Features

- 512 x 8 bit-organization
- Multiplexed address and data bus
- Tristate address and data lines
- On-chip address register
- Very low current consumption: 1 µA at 6 V during standby
- Dual chip selection
- Wide supply voltage range from 2.5 V to 6 V
- Fully compatible 5 V ± 10%
- Data retention up to 1.0 V
- Temperature range from −40 °C to 110 °C



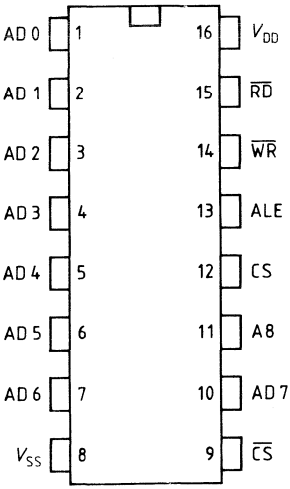
Type	Ordering Code	Package
SAE 81C54 P	Q67100-H8486	P-DIP-16

The SAE 81C54P is a static 4096-bit RAM (512 words by 8 bits) in Advanced CMOS technology. The address and data bus in the multiplex operation allows directly interfaces to 8-bit microprocessors/microcontroller families, e.g. SAB 8086, SAB 8088, SAB 8051. Due to its low power dissipation of less than 1 µA in standby mode this component requires only minimum supply current.

Pin Configurations

(top view)

SAE 81C54P



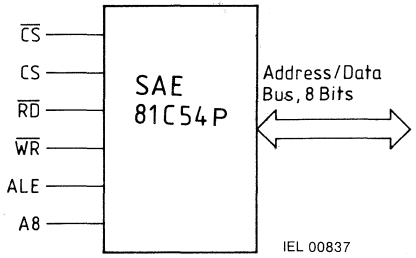
Definitions and Functions

Pin	Symbol	Function
1–7, 10	AD0-7	Address/data lines
8	V_{SS}	Ground
9	$\overline{CS}$	Chip select
11	A8	Address line
12	CS	Chip select
13	ALE	Address signal latch enable
14	$\overline{WR}$	Write enable
15	$\overline{RD}$	Read enable
16	V_{DD}	Supply voltage 2.5 to 6 V

Truth Table for Control and Data Bus Pin Status

$\overline{CS}$	CS	$\overline{RD}$	$\overline{WR}$	AD0-7 during data phase	Function
H	X	X	X	Floating	None
X	L	X	X	Floating	None
L	H	L	H	Data from memory	Read
L	H	H	L	Data to memory	Write

Logic Symbol



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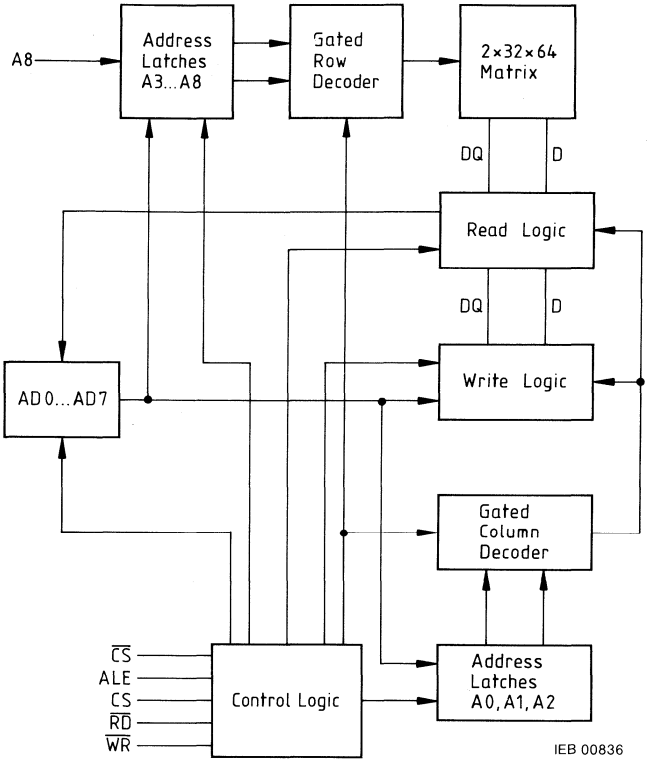
Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature	T_A	−40 to 110	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air P-DIP-16	$R_{th\ SA}$	70	K/W

DC Characteristics

$T_A = -40$ to 85 °C; $V_{DD} = 2.5$ to 6 V; $V_{SS} = 0$ V

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Standby supply current	I_{DD}			1	µA	
Operating supply current	I_{DD}		500		µA	100 kHz ALE
Operating supply voltage	V_{DD}	2.5		6	V	
Standby supply voltage	V_{DD}	1.0		6	V	Data retention
Input current	I_{IL}			1	µA	$V_I = 0$-6 V
Output leakage current	I_{QL}			1	µA	$V_Q = 0$-6 V floating
L-input voltage ($V_{DD} < 4.5$ V)	V_I	−0.8		0.6	V	
L-input voltage ($V_{DD} > 4.5$ V)	V_{IL}	−0.8		0.8	V	
H-input voltage	V_{IH}	$0.6 \times V_{DD}$		$V_{DD}+0.8$	V	
H-input voltage	V_{IH}	2.0		$V_{DD}+0.8$	V	$V_{DD} = 5$ V
L-output voltage ($V_{DD} < 4.5$ V)	V_{QL}			0.4	V	$I_{QL} = 1$ mA
L-output voltage ($V_{DD} > 4.5$ V)	V_{QL}			0.4	V	$I_{QL} = 2$ mA
H-output voltage ($V_{DD} < 4.5$ V)	V_{QH}	$0.75 \times V_{DD}$			V	$I_{QH} = 1$ mA
H-output voltage ($V_{DD} > 4.5$ V)	V_{QH}	$0.75 \times V_{DD}$			V	$I_{QH} = 2$ mA

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AC Characteristics

$T_A = -40$ to 85 °C; $V_{DD} = 4.5$ to 6 V; $V_{SS} = 0$ V

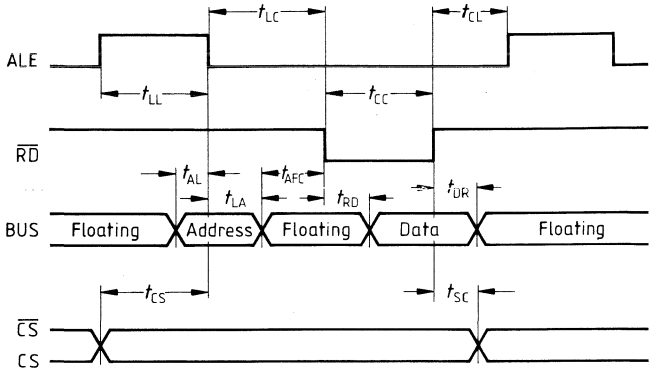
Parameter	Symbol	min.	max.	Unit
ALE pulse width	t_{LL}	40		ns
Address setup before ALE	t_{AL}	25		ns
Address hold after ALE	t_{LA}	25		ns
$\overline{WR}$ pulse width	t_{CC}	60		ns
$\overline{RD}$ pulse width	t_{CW}	130		ns
Data setup before $\overline{WR}$	t_{DW}	70		ns
Data hold after $\overline{WR}$	t_{WD}	20		ns
Data hold after $\overline{RD}$	t_{DR}		30	ns
Access time $\overline{RD}$ to data output	t_{RD}		130	ns
Address floating to $\overline{RD}$	t_{AFC}	0		ns
CS before ALE	t_{CS}	30		ns
CS after $\overline{WR}$ or $\overline{RD}$	t_{SC}	10		ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	35		ns
RD or $\overline{WR}$ to ALE = High	t_{CL}	25		ns

$T_A = -40$ to 85 °C; $V_{DD} = 2.5$ to 6 V; $V_{SS} = 0$ V

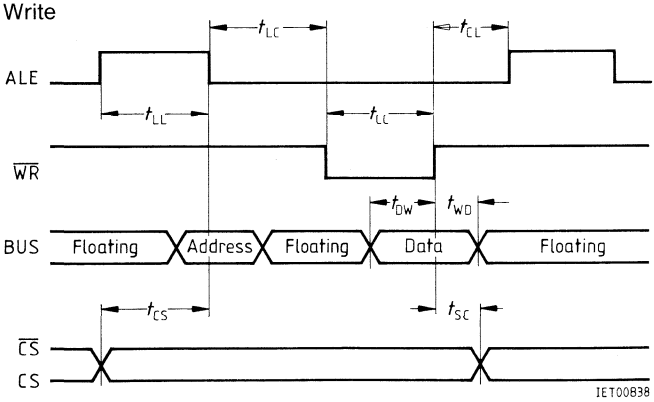
ALE pulse width	t_{LL}	60		ns
Address setup before ALE	t_{AL}	40		ns
Address hold after ALE	t_{LA}	60		ns
$\overline{WR}$ pulse width	t_{CC}	200		ns
$\overline{RD}$ pulse width	t_{CW}	350		ns
Data setup before $\overline{WR}$	t_{DW}	200		ns
Data hold after $\overline{WR}$	t_{WD}	60		ns
Data hold after $\overline{RD}$	t_{DR}		95	ns
Access time $\overline{RD}$ to data output	t_{RD}		350	ns
Address floating to $\overline{RD}$	t_{AFC}	0		ns
CS before ALE	t_{CS}	80		ns
CS after $\overline{WR}$ or $\overline{RD}$	t_{SC}	30		ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	60		ns
RD or $\overline{WR}$ to ALE = High	t_{CL}	30		ns

Diagrams

Read



Write



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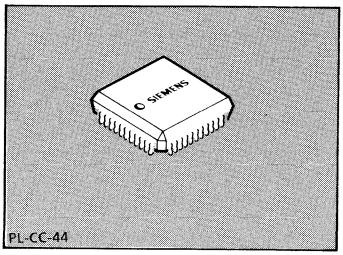
SIEMENS

CMOS Dual-Port RAM

SAE 81C80 A

Preliminary Data

CMOS IC



Features

- Processing interface with address and data bus plus signals $\overline{ALE}$, $\overline{WR}$, RD
- 8051-, 8096-compatible timing
- Memory capacity 504 bytes
- All functions fully static (excl. oscillator watchdog)
- Standby operation
- On-chip oscillator with separate clock output
- Eight scheduling registers
- Three loadable timers for processor monitoring or applicable as longterm timers
- Monitoring of internal oscillator (hardware watchdog)
- Three outputs for interrupt triggering (can be set on the bus)
- Fully asynchronous operation of two processors possible
- Data retention down to 1 V
- PL-CC-44 (SMD) package
- Extended temperature range from −40 through 85 °C
- CMOS technology

Type	Ordering Code	Package
▼SAE 81C80 A	Q67000-H8706	PL-CC-44 (SMD)

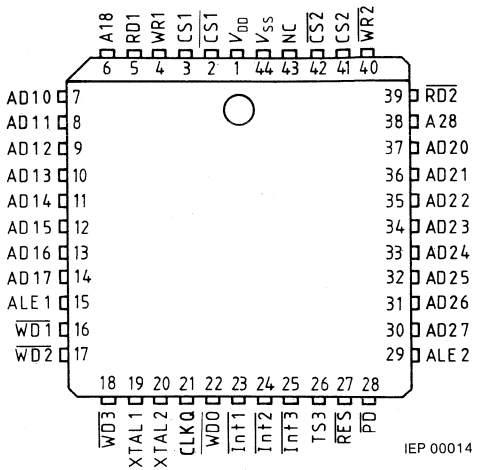
▼ New type

The SAE 81C80 A dual-port RAM (DPR) is a CMOS memory IC with a capacity of 504 bytes **(figure 1)**.

A very notable feature of this DPR is that it can be used by two microcontrollers (MCs) simultaneously and fully asynchronously. Each microcontroller uses the DPR like a normal static RAM. Thus, when comparing the circuit development of this DPR with that of standard memory, no extra effort is required. Access collisions are excluded, which is the prerequisite for fast communication between the two MCs.

The SAE 81C80 A DPR is ideally suited for multi-processor/multi-controller applications like master/slave configurations or controls where one controller acquires measured data and a second one controls the actuators (e.g. in motors, etc.). (See **figures 2 and 3)**.

Pin Configuration
(top view)



Pin Description and Function

Pin	Symbol	Function
7 8 9 10 11 12 13 14	AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17	Data and address bus port 1
6	A18	Address 8 port 1
37 36 35 34 33 32 31 30	AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27	Data and address bus port 2
38	A28	Address 8 port 2
15 29	ALE1 ALE2	Address latch enable port 1 Address latch enable port 2 These signals are for separating data and addresses on the bus. The address is stored on the falling edge of the signal.

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Pin Description and Function (cont'd)

Pin	Symbol	Function
5 39	$\overline{RD1}$ $\overline{RD2}$	Read signal port 1 (active low) Read signal port 2 (active low)
4 40	$\overline{WR1}$ $\overline{WR2}$	Write signal port 1 (active low) Write signal port 2 (active low)
3 2	CS1 $\overline{CS1}$	Chip select port 1 Chip select port 1 (active low)
41 42	CS2 $\overline{CS2}$	Chip select port 2 Chip select port 2 (active low) The chip-select inputs select a port when the two associated inputs are on active level.
27	$\overline{RES}$	Reset input Resets the IC to a defined initial state when $\overline{RES}$ is low. At the same time the outputs $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$ are switched low for the duration of the reset pulse. The oscillator continues to operate.
28	$\overline{PD}$	Power-down Disables all other inputs and the oscillator when $\overline{PD}$ is low.
44 1	V_{SS} V_{DD}	Negative supply voltage Positive supply voltage
43	NC	Not connected
19	XTAL1	Pin for crystal (must remain open for external clock supply).
20	XTAL2	Pin for crystal or applying external clock
21	CLKQ	Clock output
22	$\overline{WDO}$	Oscillator watchdog (open-drain output) High indicates that the oscillator is working.
16 17 18	$\overline{WD1}$ $\overline{WD2}$ $\overline{WD3}$	Open-drain outputs of three timers
26	TS3	Hardware signal to start timer 3.
23 24 25	$\overline{Int1}$ $\overline{Int2}$ $\overline{Int3}$	Open-drain outputs Outputs that can be controlled via the port for triggering an interrupt on a processor for example.

Block Diagram

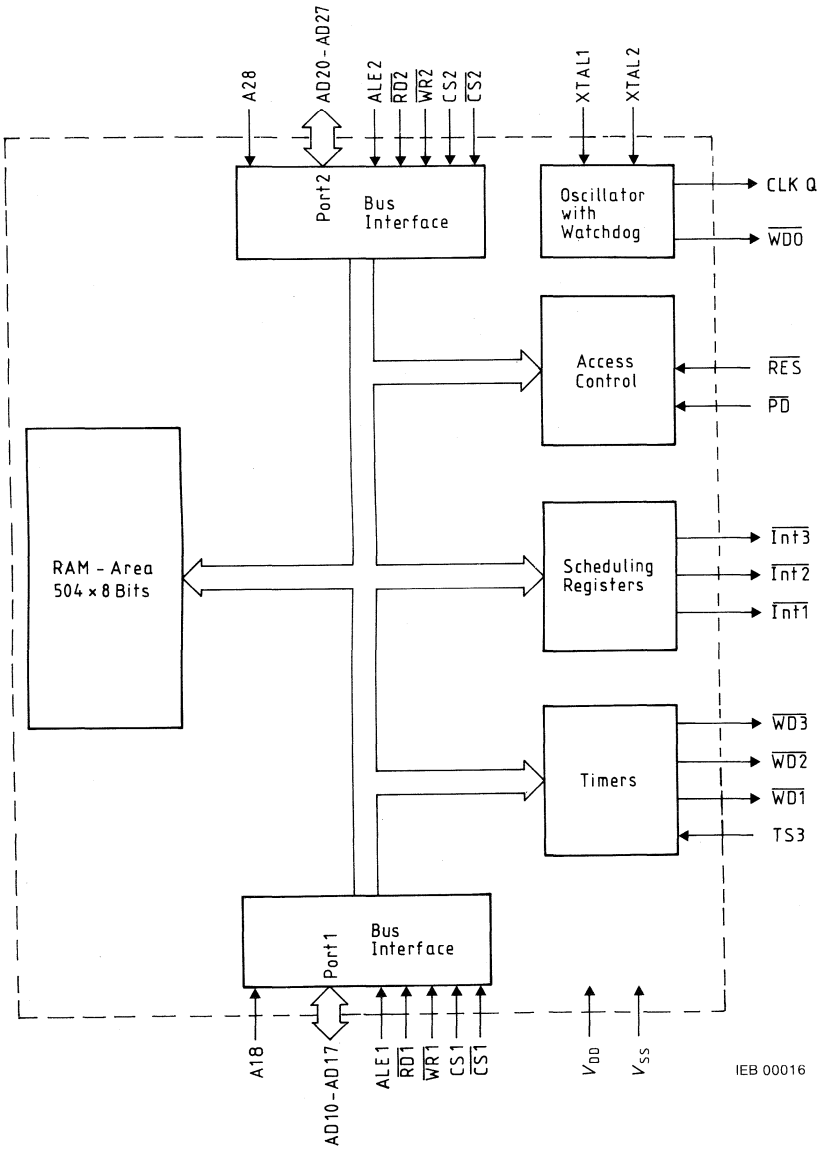

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Figure 1
Principle of the Dual-Port RAM (DPR)

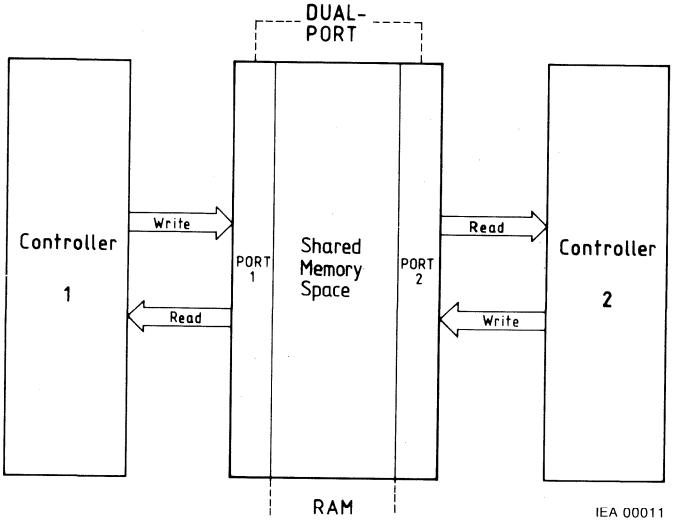


Figure 2
Interfacing Master and Slave Processors by DPRs

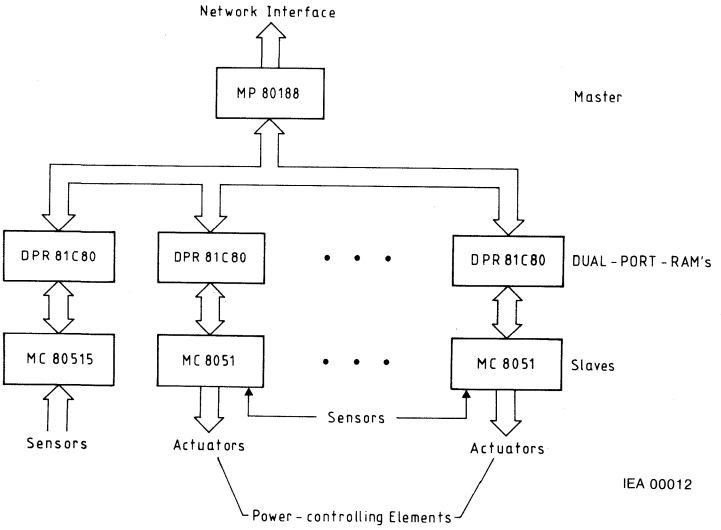
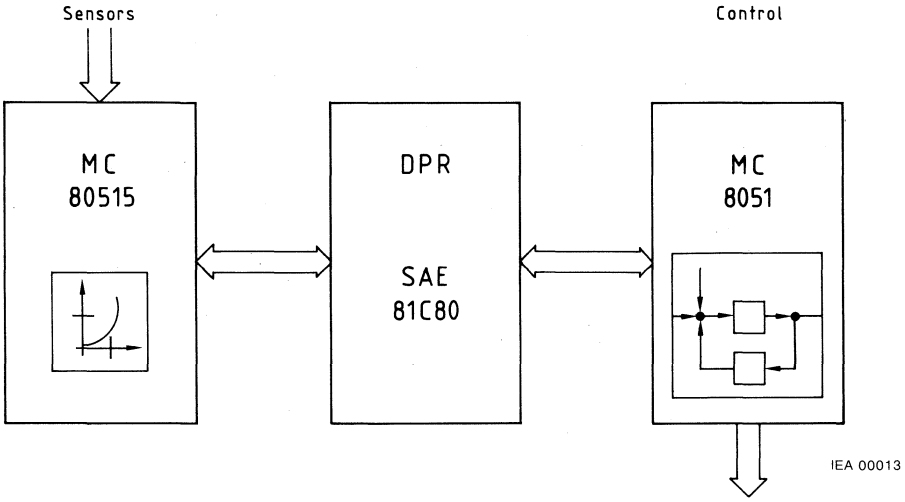


Figure 3
Dual-Port RAM used between Measured-Data Acquisition and the Actuators



Functional Decription

Dual-Port RAM

The SAE 81C80A is a 504-byte static RAM simultaneously accessible by two microcontrollers. The memory locations are selected via a multiplexed address/data bus and two chip-select inputs. The direction of data transfer is determined by the $\overline{RD}$ and $\overline{WR}$ inputs.

There will be no undefined states when a memory location is concurrently accessed by two processors, even if they write simultaneously to the same memory location. Depending on the internal state of the access control and the actual physical sequence, the value of one of the two ports will be stored. Also, if one memory location is read and written to at the same time, the data will not be mixed, i.e. either the original data or the new data are read out.

Chip-Select Inputs

The chip-select inputs affect signals $\overline{WR}$ and $\overline{RD}$, but not the ALE input. Therefore, the ALE signal on the DPR (even if the DPR is not selected) must correspond to the specified values. To eliminate selection, it is sufficient if one of the two chip-select inputs becomes inactive when the falling edge of $\overline{WR}$ or $\overline{RD}$ appears.

Reset

The reset is necessary for setting the control units of the DPR to a defined initial state. It initializes the timer-mode registers with the values $0000XXX0_B$ (timers 1 and 2) and $00000XX0_B$ (timer 3). The $\overline{INT}$ outputs are set to 0.

The reset input is a TTL input without Schmitt-trigger response. For this reason, neither an ALE nor a $\overline{WR}$ signal may be applied to the DPR if the voltage on the reset input is below V_{IH}.

When the reset input is low, outputs $\overline{WD1}$, $\overline{WD2}$ and $\overline{WD3}$ are set to low. After a reset these outputs are high. The scheduling registers are set to state 1 by reset.

A reset is also necessary if the DPR is reactivated from power-down, while the contents of the RAM and oscillator remain unaffected.

Power-Down Mode

When the power-down mode ($\overline{PD}$) is activated, all inputs (except $\overline{PD}$ and XTAL1, XTAL2) plus the oscillator are disabled. This means that any levels are possible on the remaining inputs.

An active level on $\overline{PD}$ also produces an internal reset. Nevertheless, to ensure proper operation after deactivation of the power-down mode, an external reset should be made to bridge the time required by the oscillator for buildup. The outputs of the ports go high-impedance, while outputs CLKO, $\overline{WDO}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{INT1}$, $\overline{INT2}$ and $\overline{INT3}$ are set to low. The $\overline{PD}$ input shows a Schmitt-trigger response. This allows V_{DD} to be evaluated directly, for example **(see application circuit).**

Interrupt Outputs

The DPR has three interrupt outputs that can be set and reset directly by writing to an address **(see table 1)**. The outputs are located in the same address range as the scheduling registers. However, only bits 2 and 3 are relevant for the interrupt outputs. At least one of bits 0 and 1 should be other than 1 to prevent the scheduling registers from being affected. The functions of the outputs are shown in the following table:

RES	Bit 3	Bit 2	Output
1	0	0	no change
1	0	1	1
1	1	0	0
1	1	1	undefined
0	–	–	0

Oscillator Watchdog

This part of the circuit is a fail-save mechanism for the oscillator. If the frequency of the clock is missing, the output switches to $\overline{WDO}$ low. The circuit works like an analog integrator. Below approx. 100 kHz, low pulses are produced on the output. The pulse width depends on the clock frequency. This part of the circuit should not be used at operating frequencies of less than 500 kHz.

Supply Voltage

To prevent any interference, the supply voltage of the DPR should be blocked as close as possible to the pins with a capacitor of approx. 100 nF **(see application circuit)**.

Timers

The three timers are 24-bit counters with a clock frequency of $f_{OSC}/6$. Each of the counters can be set by writing to three specific RAM addresses. The value is then simultaneously stored in the RAM and a buffer register of the timer. When the low byte is written, all three bytes are parallely stored in the reload register. The value in the reload register is kept in all operating modes until the associated low byte is written again.

The counters are down-counters. They can be started by setting bit 7 in the associated timer-mode register (TMR). Counter 3 can also be started by an external trigger signal (TS3). Each counter can be configured by a TMR. The bits of the TMRs have the following function:

Bit 0: This bit provides overwrite protection for the reload register.

Use: After writing to the reload registers and starting of the timer – by writing to the associated protection bit – the adjacent RAM area can be used without affecting the reload register (reset state = 0).

Bit 4: It serves for switching the polarity of the output signal (reset state = 0).

Bit 4 = 0; idle state 1, active 0
Bit 4 = 1; idle state 0, active 1

Bit 5: This bit switches the operating mode (reset state = 0).

Bit 5 = 0 single-shot, i.e. when the counter is started, the output signal becomes active. After reaching zero, the output signal is reset. The timer has to be restarted to trigger another count cycle. The values from the reload register are then loaded into the counter.

Bit 5 = 1 auto reload, i.e. when the counter is started, the value of the reload register is loaded into it. When zero is reached, the counter issues a pulse (≈ 4 µs at 12 MHz), automatically reloads the original value and the entire operation starts again. In this way a frequency can be set with a resolution of 24 bits. Because of the pulse width of eight timer clock pulses, however, the shortest period is limited to nine timer clock pulses (t_{OSX} x 6). If a new start pulse appears in the count cycle (even without "STOP"), no pulse is issued and the counter is reloaded.

Bit 6: In the reload mode the timer can be halted by setting this bit and resetting bit 5. (In a new start the contents of the counter are lost and that of the reload registers remain unaffected.)

Bit 7: Setting this bit starts the counter.

Only for the registers of timers 1 and 2

Bit 1-3: These are used together with bit 0 for switching the watchdog mode on and off.

Only for the register of timer 3

Bit 1-2: Reserved (should always be 0 for correct operation).

Bit 3: Switches **all three timers** to test mode, i.e. only the upper twelve bits are used to generate the output signal (reset state = 0).

External Timer Start Input TS 3

The prerequisite for several consecutive starts is a timer overflow. Subsequent triggering via TS 3 is only possible if the TS 3 pulse occurs more than 12 oscillator clocks prior to timer overflow. Between write to reload register and start of external timer there must be at least 15 oscillator clocks. For the time the stop bit is set, starting of the timer is impeded.

Watchdog Mode

For timers 1 and 2 a special mode was implemented which can be used to monitor the two processors. In this mode there is a control register (CR) for each timer **(see table 1** for addresses). The watchdog mode is set by loading the TMR with the value $101X1111_B$, the polarity of the output signal being freely selectable with bit 4. This mode works similarly to the auto-reload mode, but neither the reload register nor the TMR can be altered.

In the watchdog mode, the timer can only be restarted (and the output pulse suppressed) if the values 055_H and $0AA_H$ are successively written into the control register. The time between these two write operations is random, but the sequence must be completed before the timer has run down, i.e. the output pulse is generated. No value may be written into either the TMR or CR between the two write operations, otherwise the sequence has to be started again.

To reset the timer to the normal mode, first the value 055_H has to be written into the CR, then the value $010X0000_B$ into the TMR, and finally the value $0AA_H$ into the CR. Here, too, if any other value is written into either of the two registers during the sequence, the entire operation has to be started again. The time between the accesses is random.

The timer operation in watchdog mode is illustrated in the appendix in an 8051 example program.

Figure 4

Bit Assignment of Timer-Mode Registers for Timer 1 and 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1, single-shot = 0)	Polarity of output pulse (High = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Protection (= 1) against overwriting of reload register

Figure 5

Bit Assignment of Timer-Mode Register for Timer 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1, single-shot = 0	Polarity of output pulse (High = 0)	Test (= 1) switches timer to test mode	Reserved (normal mode = 0)	Reserved (normal mode = 0)	Protection (= 1) against overwriting of reload register

Access Collisions

With a RAM which can be written to or read simultaneously by two controllers, different kinds of access collision are possible:

1. Simultaneous read access to the same memory location from both ports;
2. One port reads the same memory location which the other port writes to concurrently
3. Concurrent write access to the same memory location from both ports;
4. Read access to a logically linked data block by one port, while the other port modifies the same data block.

The SAE 81C80 A dual-port RAM avoids the first three types of access collision by hardware. The fourth problem can be solved by user software.

The standard solution for the access collisions described above would be as follows: **before** accessing the memory area, an additional memory location must be established by setting an access flag (semaphore). This would necessitate three memory operations:

- First access: read the flag and check whether the dara area is free.
- Second access: write the flag with the data for reservation.
- Third access: read the flag and make sure that your own reservation has not been overwritten by the other port.

Only after this sequence would a microcontroller be priviledged for access and could write or read to the data area without the risk of contention.

With the SAE 81C80 A dual-port RAM this access routine is simplified using scheduling registers.

Scheduling Registers

Note: The assignment of a memory area to a scheduling register is defined by the user software of both controllers

With the scheduling registers synchronization can be done with only one access because the reservation is performed during reading. The other port cannot overwrite it.

This means that a scheduling register is **written by reading,** unless it was occupied.

The description above shows that these registers are no ordinary RAM locations. They are formed by a finite state machine (FSM), which can assume the following four states **(see figure 6):**

- State 1: port 1 was the previous owner and the register is free.
- State 2: port 1 occupies the register.
- State 3: port 2 was the previous owner and the register is free.
- State 4: port 2 occupies the register.

The state of a register can be read out from the particular address, but causes also a change in the state of the FSM (arrows in **figure 6)**. Reading produces 2-bit information:

- Bit 0 is the owner bit. It is set when the reading port is or was the owner of a register.
- Bit 1 is the occupied bit. It is set when a register has been reserved by a port.
- Bit 2 through 7 are always 0.

Reserving is done by reading a register and enabling by writing to it $XXXXXX11_B$ (pay attention to the interrupt outputs of bits 2 and 3!). Thus a correct protocol using the scheduling registers takes the following form:

1. Read the scheduling register.
2. Check whether the occupied bit is set and the owner bit is not set (i.e. the other port has reserved). If so, go back to 1, otherwise continue.
3. Process the data area.
4. Enable the scheduling register by writing 03_H to the address of the register
5. End

In cases where accessing of a data area requires prior reading of or writing to this data area by the second processor, a separate evaluation of the occupied bit and owner bit can be done in step 2:

2a. Owner bit self? If so, continue to 2c, otherwise to 2b.

2b. Occupied bit self? If so, continue to 2c, otherwise to 3.

2c. Enable the scheduling register by writing 03_H to the address of the register (continue with 1).

The following applies only to the scheduling registers:

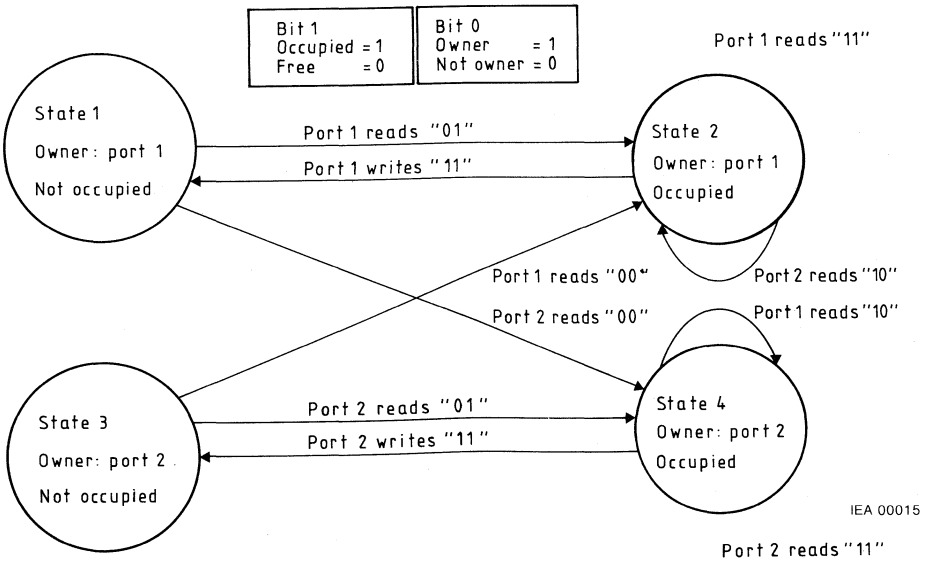
Usually, in the case of a concurrent access by both processors, writing has priority over reading. However, a simultaneous read or write access from the two ports means that port 1 has priority over port 2.

The addresses of the scheduling registers are listed in **table 1**.

The assignment of scheduling registers to specific data areas is made by the user. The software (of both controllers) should be configured so that, prior to accessing a logically related data area, the associated scheduling register is accessed first (according to the above sequence).

So the assignment of the various dual-port RAM address spaces to scheduling registers will depend solely on the structure of the user software.

Figure 6
Diagram Showing the Various States of the Scheduling Registers



Only the two least significant bits of the data are shown (in converted commas).

Notes:

1) The owner bit indicates the last owner of a register
2) Only if the port is owner of the register will writing change the state.
3) The reset state is state 1.
4) The FSM is symmetrical. Therefore, the two processors can use the same program.

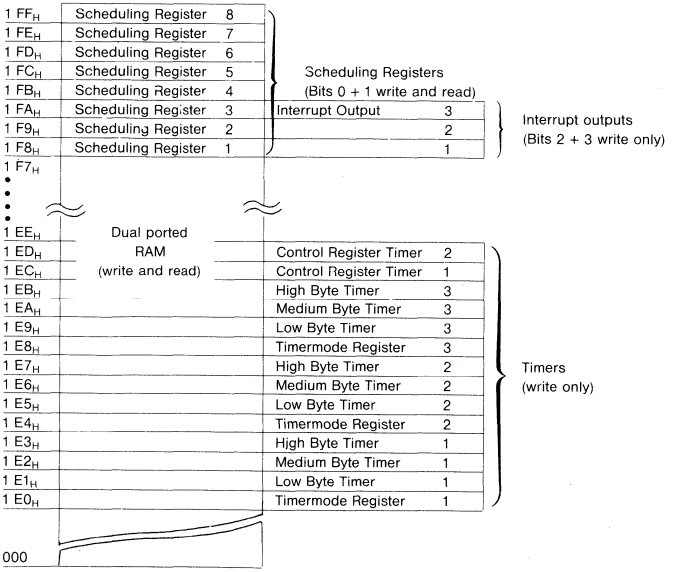
Table 1

Address Assignment of DPR Registers

Register	Address	Register	Address
Scheduling register 1	$1F8_H$	High-byte timer 2	$1E7_H$
Scheduling register 2	$1F9_H$	Medium-byte timer 2	$1E6_H$
Scheduling register 3	$1FA_A$	Low-byte timer 2	$1E5_H$
Scheduling register 4	$1FB_H$		
Scheduling register 5	$1FC_H$	High-byte timer 3	$1EB_H$
Scheduling register 6	$1FD_H$	Medium-byte timer 3	$1EA_H$
Scheduling register 7	$1FE_H$	Low-byte timer 3	$1E9_H$
Scheduling register 8	$1FF_H$		
Timer-mode register 1	$1E0_H$	Control-register timer 1	$1EC_H$
Timer-mode register 2	$1E4_H$	Control-register timer 2	$1ED_H$
Timer-mode register 3	$1E8_H$		
High-byte timer 1	$1E3_H$	Interrupt output 1	$1F8_H$
Medium-byte timer 1	$1E2_H$	Interrupt output 2	$1F9_H$
Low-byte timer 1	$1E1_H$	Interrupt output 3	$1FA_A$

Figure 7

Memory Map



Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Absolute Maximum Ratings ($T_A = -40\,°C$ to $85\,°C$; all voltages referred to V_{SS})					
Storage temperature	T_{stg}	−50		125	°C
Total power dissipation	P_{tot}			500	mW
Power dissipation per output	P_Q			50	mW
Input voltage	V_I	−0.5		$V_{DD}+0.5$	V
Supply voltage	V_{DD}	−0.5		6	V
Operating Range					
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (w/o loading of outputs)	I_{DD}			20	mA
Operating frequency	f_s			12	MHz
Ambient temperature*)	T_A	−40		85	°C
Standby current	I_{DD}			1	µA
Data-retention voltage	V_{DH}	1			V

*) Specification for −40 to 110 °C on request.

DC Characteristics ($T_A = 25\,°C$; all voltages referred to V_{SS})

Parameter	Symbol	Limit Values min.	max.	Unit	Test Conditions
All input signals except XTAL2 and $\overline{PD}$					
H-input voltage	V_{IH}	2.2	V_{DD}	V	
L-input voltage	V_{IL}	0	0.8	V	
Input capacitance	C_I		10	pF	
Input current	I_I		1	µA	
XTAL2 (as external clock input)					
H-input voltage	V_{IH}	3.5	V_{DD}	V	
L-input voltage	V_{IL}	0	0.5	V	
Input capacitance	C_I		10	pF	
$\overline{PD}$ (Schmitt-trigger characteristics)					
H-input voltage	V_{IH}	$V_{DD}-1$	V_{DD}	V	
L-input voltage	V_{IL}	0	1.0	V	
Input capacitance	C_I		10	pF	
Output signals AD10-17, AD20-27					
H-output voltage	V_{QH}	2.4	V_{DD}	V	$I_Q = 0.5$ mA
L-output voltage	V_{QL}		0.4	V	$I_Q = 1.6$ mA

DC Characteristics ($V_A = 25\,°C$; all voltages referred to V_{SS})

Parameter	Symbol	Limit Values			Test Conditions
		min.	max.	Unit	
Output signals $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{WD0}$ (open drain, weak pullup)					
L-output voltage	V_{QL}		0.4	V	$I_Q = 1.6$ mA
Output signal clock out					
H-output voltage	V_{QH}	2.4		V	$I_Q = 0.5$ mA
L-output voltage	V_{QL}		0.4	V	$I_Q = 1.6$ mA
Load capacitance	C_L		80	pF	

AC Characteristics

The AC characteristics apply throughout the operating range $T_A = 25\,°C$.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Read cycle time	t_{CYR}	$300 + t_{LHLL}$		ns
Write cycle time	t_{CYW}	$440 + t_{LHLL}$		ns
ALE pulse width	t_{LHLL}	40		ns
Address setup to ALE low	t_{AVLL}	30		ns
Address hold after ALE low	t_{LLAX}	40		ns
$\overline{RD}$ pulse width	t_{RLRH}	120		ns
$\overline{WR}$ pulse width	t_{WLWH}	120		ns
ALE low to $\overline{RD}$ or $\overline{WR}$ active	t_{LLWL}	30		ns
Data hold after $\overline{RD}$ high	t_{RHDX}	0	30	ns
ALE low to valid data out	t_{LLDV}		270	ns
$\overline{RD}$ low to data valid (only scheduling registers)	t_{RLDV}		$2\,t_{OSC} + 20$	ns
Valid data in after $\overline{WR}$ low	t_{DVWL}		30	ns
$\overline{WR}$ low to ALE high	t_{WLLH}	150		ns
Data setup before $\overline{WR}$ high	t_{QVWH}	30		ns
Data hold after $\overline{WR}$ high	t_{WHQX}	30		ns
Delay $\overline{RD}$ low to both chip select active	t_{RLCH}		20	ns
Delay $\overline{WR}$ low to both chip select active	t_{WLCH}		20	ns

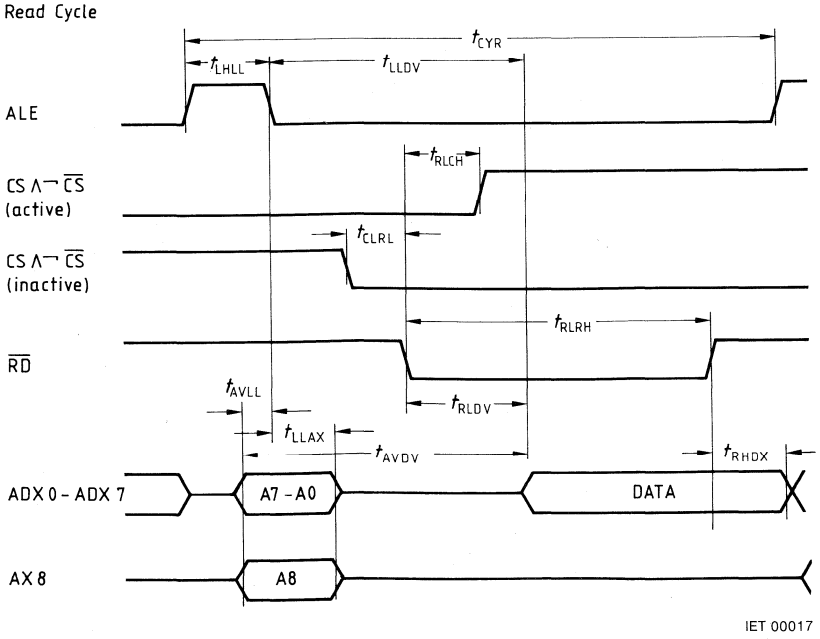
AC Characteristics

The AC characteristics apply throughout the operating range
$T_A = 25\,°C$.

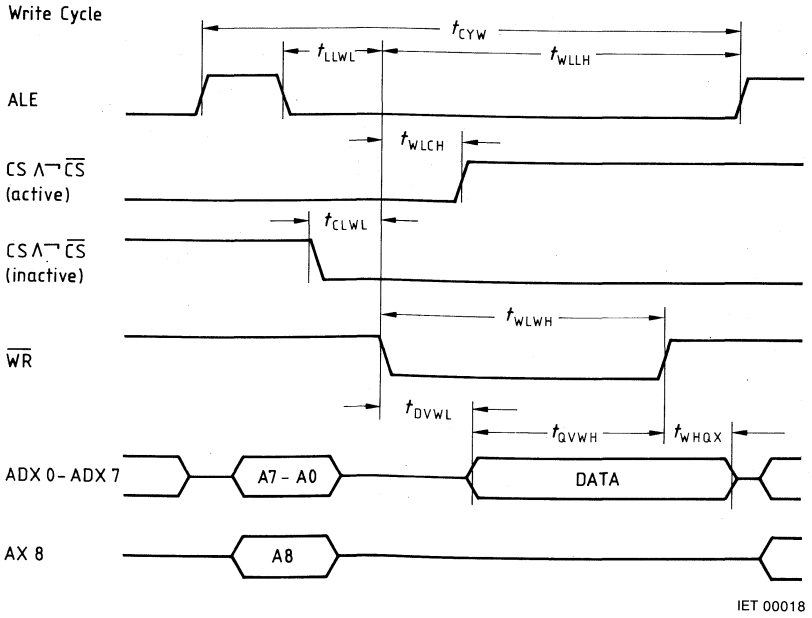
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Setup of chip select to $\overline{RD}$*)	t_{CLRL}	0		ns
Setup of chip select to $\overline{WR}$*)	t_{CLWL}	0		ns
Active pulse length of timer outputs	t_{ACT}	48 t_{OSC}	48 t_{OSC}	ns
Pulse width of TS3	t_{THTL}	2 t_{OSC}		ns
Oscillator period	t_{OSC}	83		ns
High time	t_{OSCH}	35		ns
Low time	t_{OSCL}	35		ns

*) For deselection

Pulse Diagram 1

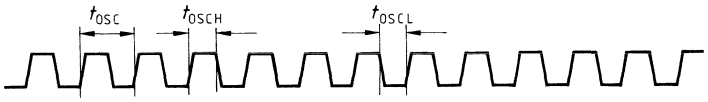


Pulse Diagram 2



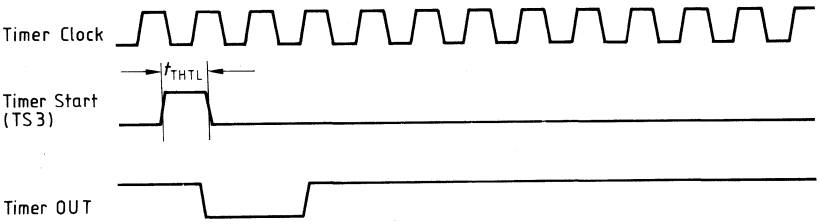
Pulse Diagram 3

Oscillator

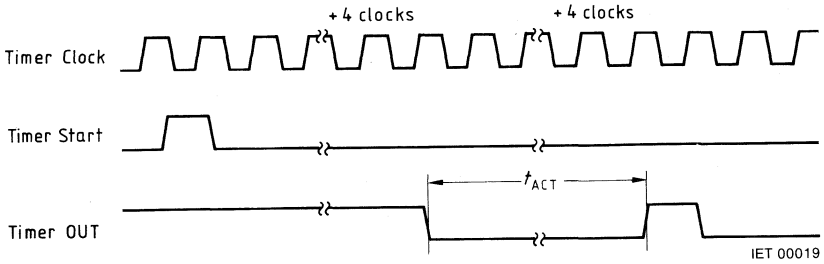


Timer

Single-shot mode (TMR = 80_H, High byte = Medium byte = 00_H, Low byte = 02_H)



Auto reload mode (TMR = $A0_H$, High byte = Medium byte = 00_H, Low byte = 09_H)



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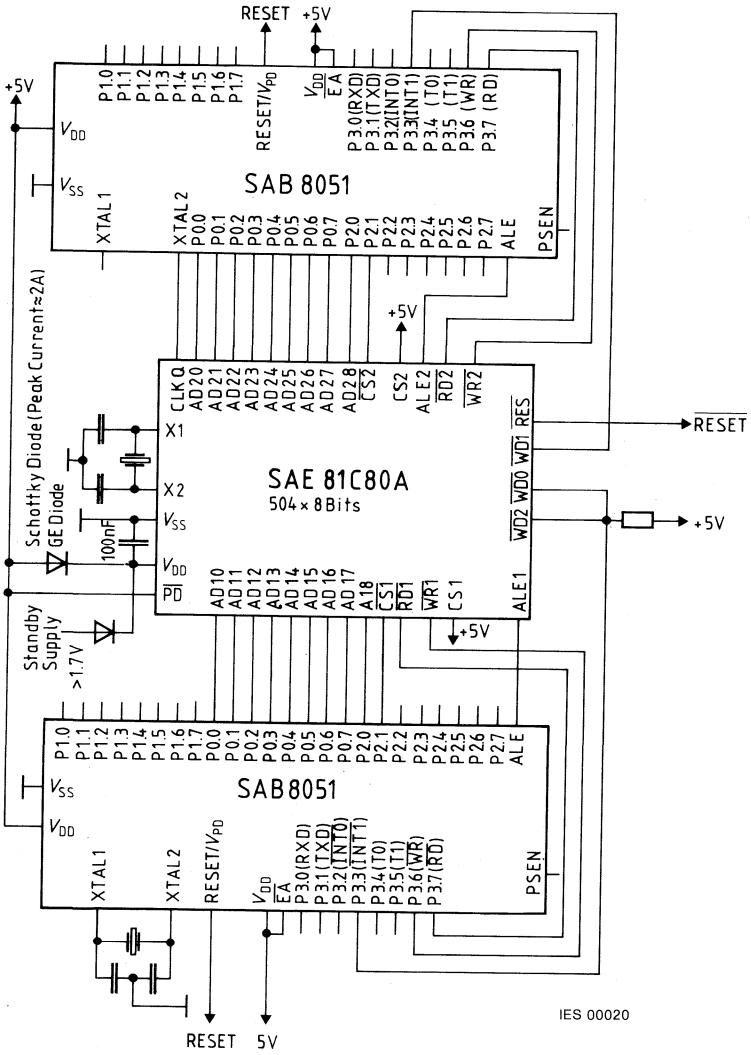
Example of an Application Circuit[1)]



1) Design proposal (non-obligatory)

Appendix

8051 Program for Timer Operation in Watchdog Mode

```
HBYTE   EQU   1E3H    ; Address high byte reload register
TMR     EQU   1E0H    ; Address timer-mode register
CR      EQU   1ECH    ; Address control register
REST1   EQU   055H    ; 1st value to restart timer
REST2   EQU   0AAH    ; 2nd value to restart timer
WDOFF   EQU   040H    ; Value to switch off watchdog mode

; Load reload register

MOV     DPTR,#HBYTE
CLR     A
MOVX    @DPTR,A
DEC     DPL
MOV     A,#0FFH
MOVX    @DPTR,A
DEC     DPL
MOVX    @DPTR,A

; Set watchdog mode and start timer

MOV     A,#0AFH
DEC     DPL
MOVX    @DPTR,A

; Reset timer

MOV     DPTR,#KR
MOV     A,#REST1
MOVX    @DPTR,A
MOV     A,#REST2
MOVX    @DPTR,A

; Switch off watchdog mode and halt timer

MOV     DPTR,#KR
MOV     A,#REST1
MOVX    @DPTR,A
MOV     A,#WDOFF
MOV     DPTR,#TMR
MOVX    @DPTR,A
MOV     A,#REST2
MOV     DPTR,#KR
MOVX    @DPTR,A

;
END
```

SIEMENS

Nonvolatile Memory 1-Kbit E²PROM

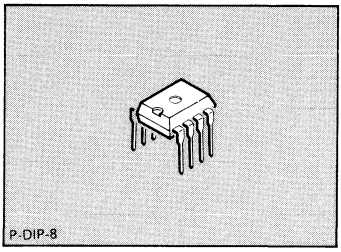
SDE 2506 A2

Preliminary Data

MOS IC

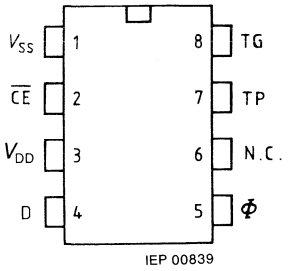
Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 x 8-bit organization
- 5 V supply voltage
- 3 lines between processor and E²PROM for data transfer and chip control
- Data input (8 bits), address input (7 bits), control information input (1 bit) and data output are serial
- More than 10^5 reprogramming cycles per address
- Data retention longer than 10 years (operating temperature range)
- Unlimited number of read-out operations without refresh
- 5 ms erase/write cycle
- Extended temperature range from −40 °C to 110 °C



Type	Ordering Code	Package
SDE 2506 A2	Q67100-H9018	P-DIP-8

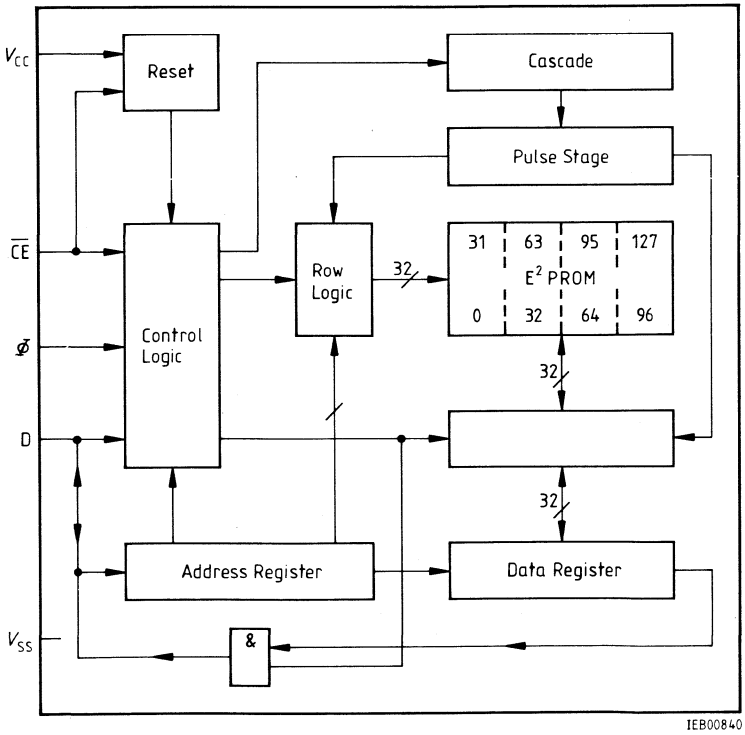
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE}$ = 1 for data input/output, $\overline{CE}$ = 0 for reprogramming
3	V_{DD}	+5 V supply voltage
4	D	Data input/output bidirectional data line For reprogramming D = 1 erase, D = 0 write
5	Φ	Clock
6	N.C.	Not connected
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open

Block Diagram



Circuit Description

Data Transfer and Chip Control

Three lines having several functions each are required for data transfer between control processor and E²PROM memory.

a) Data line D
   - bidirectional serial data transfer
   - serial address input
   - clocked input of a control information
   - direct control input

b) Clock line Φ
   - data input, address input and control bit input
   - data output
   - start read-out with takeover of data from memory in shift register or start data-change during reprogramming

c) Chip enable line $\overline{EC}$
   - chip reset and data input (active high)
   - chip enable (active low)

Prior to activating the chip, the data, address and control information is clocked in via the bidirectional data bus. These data are maintained in the shift register during reprogramming and read-out up to the second clock pulse. The following data formats have to be input:

a) Memory read-out: one 8-bit control word, consisting of
   - 7 address bits A0 to A6 (at first A0 being LSB)
   - 1 control bit, SB = "0", after A6

b) Memory reprogramming (erasure and/or writing) 16-bit input information, consisting of
   - 8 bits D0 to D7 new memory information (at first D0 being LSB)
   - 7 bits A0 to A6 address information (at first A0 being LSB after D7)
   - 1 bit control information, SB = "1", after A6

Memory Read-Out

After data input and with SB = "0" the read-out operation of the selected word address is started by the transition of $\overline{CE}$ from "1" to "0". The information being on the data line during chip enable is of no influence.

With the first clock pulse after $\overline{CE}$ = "0" the data word is taken over from the selected memory address into the shift register. After termination of the first Φ pulse the data output is in the low impedance state. With every following clock pulse another data bit is pushed to the output. Through the transition of $\overline{CE}$ from "0" to "1" the data line returns to the high impedance state.

Reprogramming

In general, a full reprogramming operation consists of an erasure operation and a subsequent writing operation. During erase all bits of the selected word are set into the uniform "1" state, during writing "0" states are produced according to the information in the shift register.

A reprogramming operation is started when after data input and due to chip activation an information SB = "1" is in the relevant cell. Whether an erase or a writing operation is then taking place depends on the information that is on data line D during chip enable.

For erasure in state "1", a "1" must be present at the data input during transition of $\overline{CE}$ to low. If, however, a writing process is to be started in state "0", a "0" has to be present at the data line during chip enable.

Afterwards, a start pulse at the clock input Φ is required for the programming start. The control information has to remain stable at D until the leading edge of the start pulse is reached. The active data change starts with the trailing edge of this start pulse. The programming process is terminated by suppression of the chip enable, i.e. by CE.

The reprogramming of a word is initiated with start and followed by an erase procedure. $\overline{CE}$ = "1" stops erasure. The control bit SB = "1" (in the shift register), which is also necessary for the write process, remains stable even after the termination of erasure. Thus, for writing the selected word, only the data line D has to be changed from "1" to "0", the chip has to be enabled again by $\overline{CE}$ = "0" and the data change has to be started by the start pulse.

An erase and a write process can also be executed separately. In order to obtain a safe "1" in all 8 bits of the selected memory address by the erase process, a data word is, however, to be entered with 8 times "1" before erasure. During the writing of a word which has not been erased before, the "0" states of the previous and the actual information are added.

Test Mode – Total Erasure

The test mode is activated, if the input TP (pin 7) is set from 0 V to 5 V = V_{DD}. To erase the entire memory, the test mode is to be turned on and the address 0 (A0 to A6) together with the control bit SB = 1 is to be entered. The subsequent programm sequence is identical to the erasure of address 0. As soon as the erase procedure has terminated due to $\overline{CE}$ changing from 0 to 1, the test mode is to be turned off.

RESET

A memory which has not been selected is automatically in reset state by state $\overline{CE}$ = "1". All flipflops of the sequence control are reset. However, the information in the shift register is maintained and will only be changed by shifting the data. The reset state is also set in the case of the turning-on of the memory (power-on) by an on-chip circuit.

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Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage Input voltage	V_{DD} V_I	−0.3 −0.3	6 6	V V
Power dissipation	P_D		40	mW
Storage temperature Junction temperature	T_{stg} T_j	−55	125 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$		100	K/W

Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	−40	110	°C

Characteristics

$T_A = 25\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
Supply voltage	V_{DD}	4.75	5	5.25	V	
Supply current	I_{CC}			3	mA	($V_{DD} = 5.25$ V)
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L			0.8	V	
Input voltage (D, Φ, $\overline{CE}$)	V_H	2.4			V	
Input current (D, Φ, $\overline{CE}$)	I_H			10	µA	($V_H = 5.25$)
Data Output D (open drain)						
L-output current	I_L			0.5	mA	($V_L = 0.8$ V)
H-output current	I_H			10	µA	($V_H = 5.25$ V)

Characteristics

$T_A = 25\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Clock Pulse Φ						
Clock High period	t_H	2.5		60	µs	
Clock Low period	t_L	5			µs	
Edge spacing $\overline{CE}$ to D	Δt	2.5			µs	
Edge spacing $\overline{CE}$ to Φ	t_{AKT}	5			µs	
Data hold time (before/after Φ trailing edge	t_{HD}	2.5			µs	
Data delay time (after Φ trailing edge)	t_{DD}	2.5			µs	
Rise time	t_r			1	µs	
Fall time	t_f			1	µs	
Chip erase duration	t_{er}	5		20	ms	
Write duration	t_{wr}	5		20	ms	
Full erasure duration	$t_{tot\ er}$	20		25	ms	

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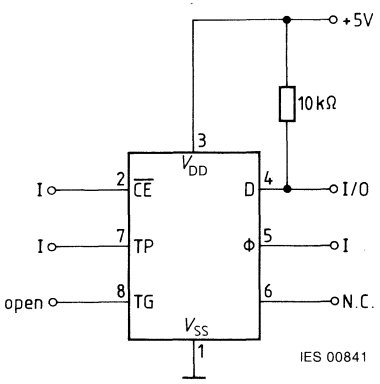
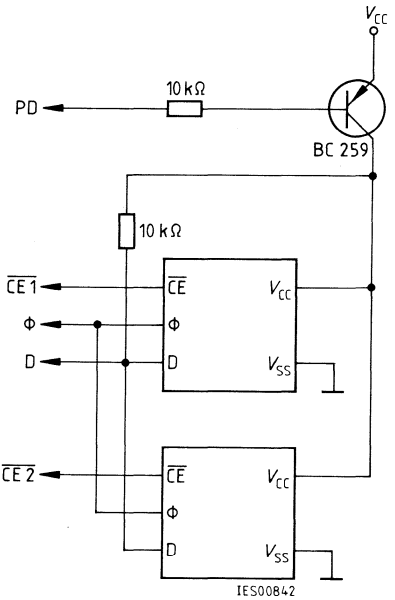
Test Circuit

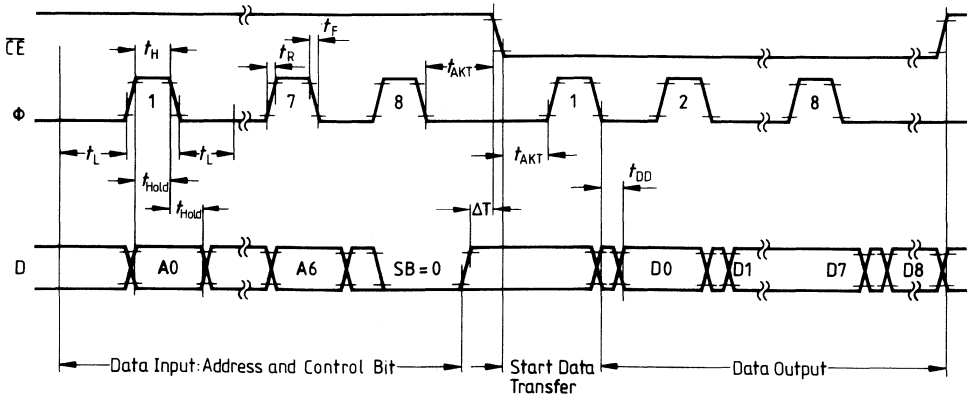


Application Circuit



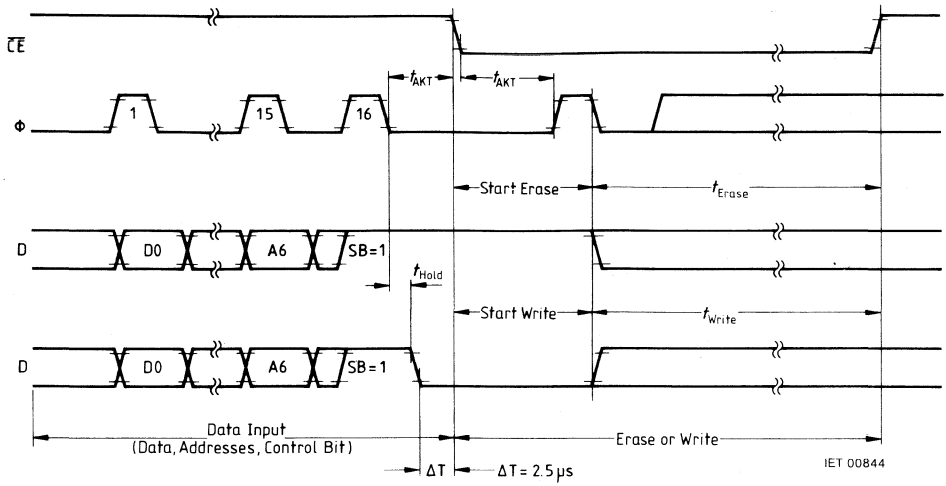
Diagrams

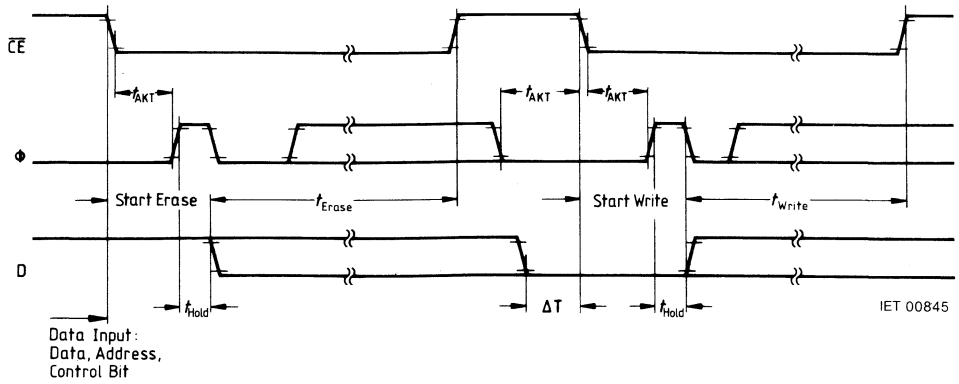
Read



t_{AKT} = 5 µs; t_R = t_F = 1 µs
t_{Hold} = 2.5 µs; t_L = 5 µs
t_{DD} = 2.5 µs; t_H = 2.5 µs
ΔT = 2.5 µs

Diagram
Reprogramming





12

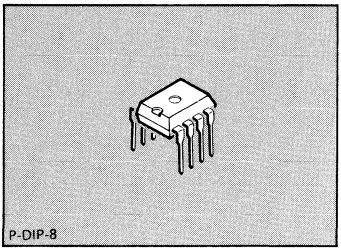
SIEMENS

Nonvolatile Memory
2-KBit E²PROM with I²C Bus Interface

SDE 2526 A2

Preliminary Data

MOS IC

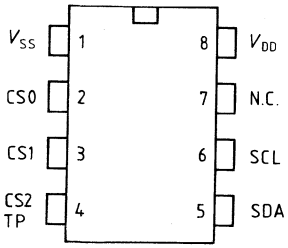


Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 x 8-bit organization
- +5 V supply voltage
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, typ. 15 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Data retention longer than 10 years
- More than 10^5 reprogramming cycles per address
- Extended temperature range from −40 °C to 110 °C

Type	Ordering Code	Package
SDE 2526 A2	Q67100-H9020	P-DIP-8

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select input
3	CS1	Chip select input
4	CS2/TP	Test operation control
5	SDA	Data line } I²C bus
6	SCL	Clock line } I²C bus
7	N.C.	Not connected
8	V_{DD}	Supply voltage

Control Word Input Key

CS/E CS/A	Chip select for data input to memory Chip select for data output from memory
WA	Memory word address
DE DA	Data word for memory Data word read out from memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

I²C Bus Interface (Figure 1 and 2)

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the device can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the 8th transmission pulse and a 9th acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in **figure 2** (high-speed mode).

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Control Functions of the I²C Bus

The device is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the

data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memories connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three selct inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 255, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 30 ms, or typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-On Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in the high-impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Test Mode – Chip Erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". Input CS2/TP, however, is connected from 0 V to +12 V immediately before the stop condition is generated. The subsequent stop condition initiates the chip erase procedure. The control word has to be entered under the device address 0 (CS0 = L, CS1 = L, CS2 = L). After the full erase has been terminated, input CS2/TP must again be connected to 0 V.

Absolute Maximum Ratings[1])

Parameter	Symbol	Limit Values	Unit
Supply voltage Input voltage	V_{DD} V_I	−0.3 to 6 −0.3 to 6	V V
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	−40 to 110	°C

DC Characteristics

		Limit Values			
Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{DD}	4.75		5.25	V
Supply current	I_{DD}			20	mA
Inputs SCL/SDA					
Low level High level	V_{IL} V_{IH}	 3.0		1.5 V_{DD}	V V
High current $V_{IH} = V_{DD\ max}$	I_H			10	µA
Output SDA					
Low current $V_{QL} = 0.4$ V	I_{QL}			3.0	mA
Leakage current $V_{QL} = V_{DD\ max}$	I_{QH}			10	µA
Inputs CSO, CS1, CS2/TP					
Low level High level	V_{IL} V_{IH}	 4.5		0.2 V_{DD}	V V
High current	I_{IH}			100	µA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erase and write)	t_{prog}		10	20	ms
Input capacitance	C_I			10	pF
Full erase duration (test mode full erase)	t_{er}			20	ms

[1]) does not apply to the input CS2/TP in "test mode – full erasure" operation

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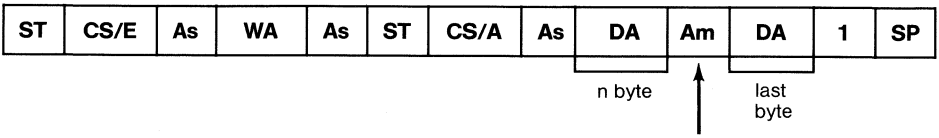
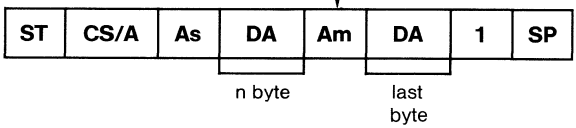
Control Word Input Read

a) complete (with word address input)

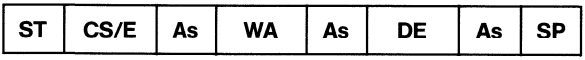


Automatic incrementation of the word address

b) shortened (read out starts with last used word address)



Control Word Input Programming



(Reprogramming starts after this stop condition)

Control Word Table

Clock N	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Diagrams

Figure 1
Operational States of the I²C Bus

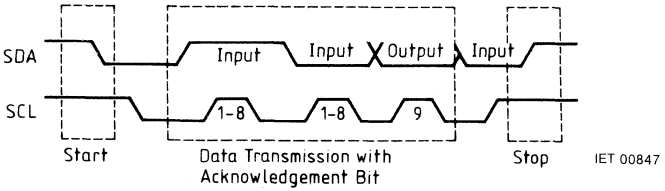
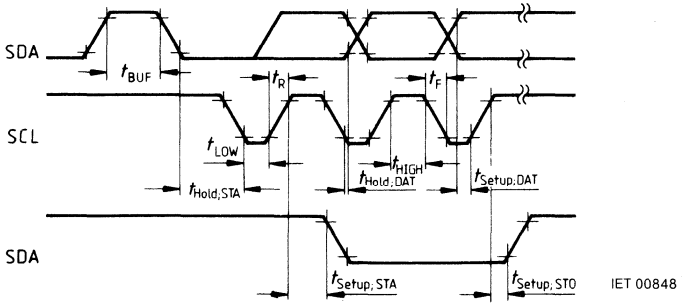


Figure 2
Timing Conditions for the I²C Bus (high-speed mode)



Parameter	Symbol	Limit Values
The minimum time the bus must be free before a new transmission can start	t_{BUF}	$t > t_{LOWmin}$
Start condition hold time	$t_{Hold;\ STA}$	$t > t_{HIGHmin}$
Clock LOW period	t_{LOWmin}	4, 7 µs
Clock HIGH period	$t_{HIGHmin}$	4 µs
Start condition setup time, only valid for repeated start code	$t_{Setup;\ STA}$	$t > t_{LOWmin}$
Data hold time[1])	$t_{Hold;\ DAT}$	$t > 0$ µs
Data setup time	$t_{Setup;\ DAT}$	$t > 250$ ns
Rise time of both the SDA and SCL line	t_r	$t < 1$ µs
Fall time of both the SDA and SCL line	t_f	$t < 300$ ns
Stop condition setup time	$t_{Setup;\ STO}$	$t > t_{LOWmin}$

Note
All values refer to V_{IH} and V_{IL} level

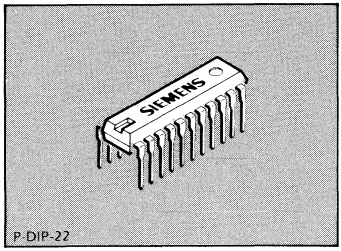
[1]) Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

Video-Pulse Generator

TBB 278 A

Preliminary Data

CMOS



Features

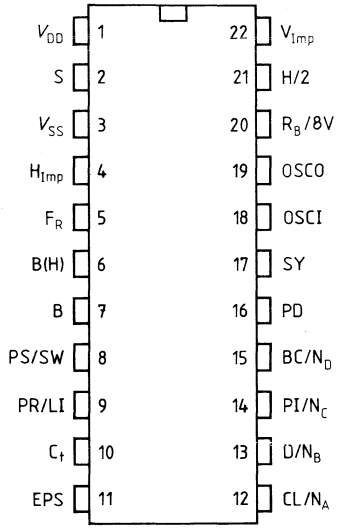
- Free-running or external synchronization
- External synchronization optionally with S signal and PLL or with basic timing signal t_0 and frame reset signal
- Parallel or serial programming
- Line interlacing can be disabled
- Parallel programming:
  - 16 systems with firmly assigned line numbers and pulse widths (CCIR 624-3, EIA RS 343 A, CCIR AZ 11, HDTV and others)
- Serial programming:
  - Line number per field selectable between 1 and 4095
  - Pulse widths selectable in steps
  - Identification signals for PAL, PAL-M, SECAM and NTSC color systems
  - Equalizing signals and V_{sync}-interruptors can be disabled
  - TLL-compatible serial interface
  - Power-on reset on PAL system

Type	Ordering Code	Package
▼ TBB 278 A	Q67100-H8705	P-DIP-22

▼ New type

The TBB 278 A video-pulse generator is an LSI circuit generating the sync, control and color-subcarrier-window signals that are necessary for controlling cameras, monitors, mixing consoles and similar items of equipment. Up to 4095 lines and the pulse widths of output signals can be serially programmed. Alternatively to serial programming, 16 standards or systems based on standards can be selected on a parallel interface or by switches or hardwiring.

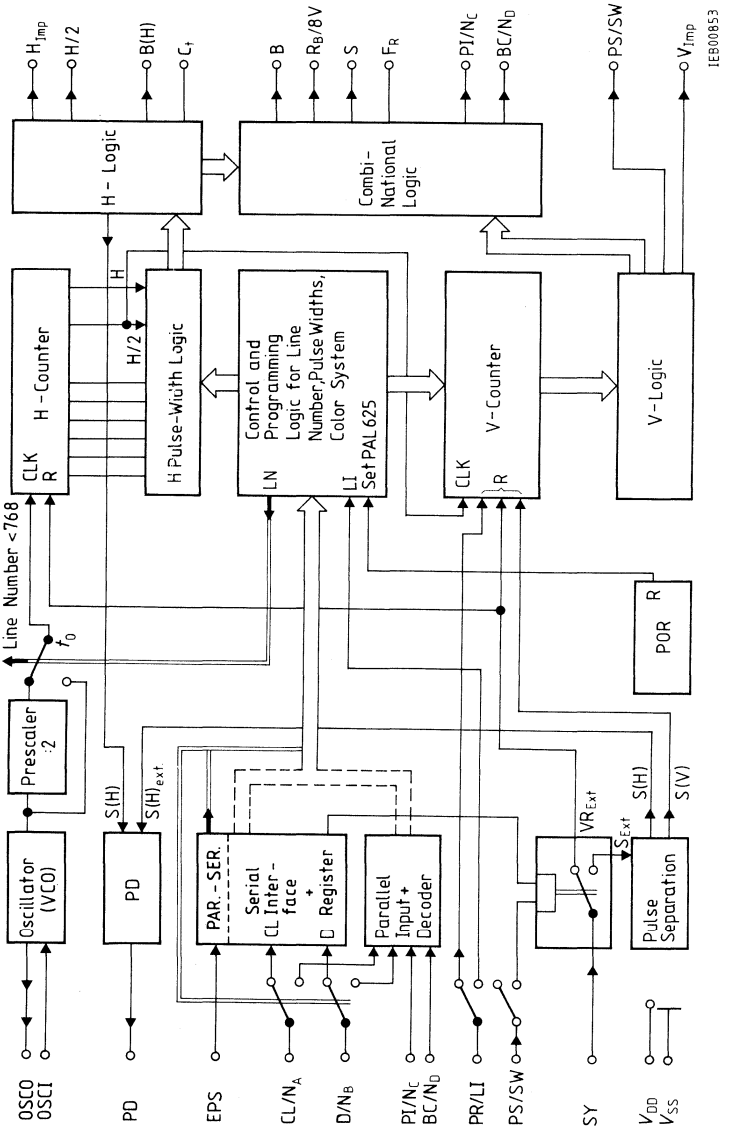
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	Supply voltage
3	V_{SS}	Ground
19	OSCO	Crystal connection/ext. clock
18	OSCI	Crystal connection
16	PD	PLL output
12	CL/N_A	Clock/parallel programm. input
13	D/N_B	Data/parallel programm. input
11	EPS	Parallel/serial programming switchover, transfer to serial latch
17	SY	Ext. sync signal input
4	H_{Imp}	Horizontal pulse (line freq.)
21	H/2	Double line frequency
6	B(H)	Horizontal blanking pulse
10	C_t	Clamping pulse
7	B	Blanking signal
20	R_B/8 V	Vidicon blanking signal output/ output for color-subcarrier-phase identification signal
2	S	Sync signal
5	F_R	Frame reset signal
22	V_{Imp}	Vertical pulse
14	PI/N_C	Output for PAL identification pulse or SECAM identification/ parallel programming input
15	BC/N_D	Burst window output (PAL, PAL-M, NTSC), color-subcarrier blanking-window output (SECAM)/ parallel programming input
8	PS/SW	PAL squarewave output/input for external sync selection
9	PR/LI	Reset input for PAL square on 1st field, set input for S9, S10 on 4th field/ disactivate line interlacing

Block Diagram



Functional Description

The block diagram illustrates the basic design of the circuit.

The TBB 278 A is parallelly or serially programmed according to the level on pin EPS. Pins with names separated by a slash have a different function for parallel and serial programming.

Parallel programming (EPS = High)

16 systems can be selected with firmly assigned numbers of lines and pulse widths **(see tables 1 and 2)**.

Pins CL/N_A, D/N_B, PI/N_C, BC/N_D, PS/SW and PR/LI are activated as parallel programming inputs. In addition to the PS/SW selection of the sync mode, the line interlacing PR/LI can also be freely selected for all 16 programs (**see table 1**). In systems S9 and S10 four fields have the standard line numbers 1023 and 1249, respectively. (Because of the odd number of lines the fourth field has a different number of lines to the preceeding three fields.)

Apart from the input signal PS/SW, which is effective immediately, parallel systems newly programmed with PR/LI, CL/N_A, etc are not adopted until the following (internal) F_R pulse occurs, i.e. the TBB 278 A does not start to operate according to the new system until the beginning of the next frame.

The sync input signals SY and PR/LI (PR only for S9, S10) are effective immediately **(see figure 1)**.

Serial programming (EPS = Low)

It is possible to design systems with any line numbers and pulse widths **(see table 3)**. Pins CL/N_A and D/N_B are activated as serial programming inputs, PI/N_C, BC/N_D, PS/SW and R_B/8V as color-identification signal outputs and PR/LI as a PAL square reset input.

The power-on reset automatically programs the serial register to the PAL-system with 625 lines/frame. Another system can be written in with shift clock CL/N_A and data D/N_B, and transfer by the following (internal) F_R pulse can be activated with a short high-pulse on pin EPS. (A high pulse that is substantially longer than 5 µs will switch the TBB 278 A to "parallel", but the information in the shift register will not be lost.) As in the parallel mode, the TBB 278 A does not start to operate according to the new system until the beginning of the next frame.

Only the sync selection bit # 1 is effective immediately with the EPS high edge, and likewise of course the sync input signals SY and PR/LI **(see figure 3)**.

Serial coding comprises a total of 71 bits:

12 bits	2^0 thru 2^{11}	for line number per field, 1-4095
3 bits		for selecting color system
47 bits		for flexible setting of pulse widths and delays of horizontal and vertical output signals as multiples of oscillator basic timing t_0 or of line period H.
6 bits		number of equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without line interlacing
1 bit		for selecting synchronization mode
		N_B: for external timing = master timing, the internal oscillator is disabled

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Functional Description

Systems Selectable on Parallel Interface

System	Lines/Frame	Field/Frame Freq.	Standard
S1	625	50/25	CCIR report 624-3
S2	525	60/30	CCIR report 624-3
S3	735	60/30	Based on EIA RS 343 A
S4	875	50/25	Based on CCIR
S5	1125	60/30	HDTV Japan
S6	1023	60/30	EIA RS 343 A
S7	1249	50/25	Based on EIA RS 343 A
S8	1249	80/40	Flickerfree monitors
S9	3 x 256 1 x 255	120	Progressive scanning
S10	3 x 312 1 x 313	100	Progressive scanning
S11	1023	30	Progressive scanning
S12	1249	25	Progressive scanning
S13	2046	3	High-definition progressive scanning
S14	2498	2.5	High-definition progressive scanning
S15	1251	50/25	Based on EIA RS 343 A
S16	1125	60/30	CCIR report AZ 11

Absolute Maximum Ratings

$T_A = -25$ to 75 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input voltage	V_I	−0.3	V_{DD} + 0.3	V
Supply voltage	V_{DD}	−0.3	6	V
Storage temperature	T_{stg}	−50	125	°C
Total power dissipation	P_{tot}		500	mW
Power dissipation per output	P_Q		50	mW

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output load)	I_{DD}			5	mA
Operating frequency	f_{OSC}			15	MHz
Ambient temperature	T_A	−25		75	°C

DC Characteristics

$T_A = 25\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Inputs						
PI/N_C, BC/N_D						(OSCO for
SY, PS/SW, OSCI, OSCO						ext. clock)
H-input voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		0.3 V_{DD}	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Inputs (TTL-compatible)						
EPS, CL/N_A, D/N_B						
H-input signal	V_{IH}	2		V_{DD}	V	
L-input signal	V_{IL}	V_{SS}		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Outputs						
H/2, B(H), C_t, B						
PI/N_C, BC/N_D, PS/SW, R_B/8V						
H-output voltage	V_{QH}	4.5		V_{DD}	V	$I_{QH} = 2.5$ mA
L-output voltage	V_{QL}	0		0.5	V	$I_{QL} = 2.5$ mA
PD						
H-output voltage	V_{QH}	4		V_{DD}	V	$I_{QH} = 100$ µA
L-output voltage	V_{QL}	0		1	V	$I_{QL} = 100$ µA
OSCO						
H-output voltage	V_{QH}	4		V_{DD}	V	$I_{QH} = 200$ µA
L-output voltage	V_{QL}	0		1	V	$I_{QL} = 200$ µA
H_{Imp}, S, F_R; V_{Imp}						
H-output voltage	V_{QH}	4.5		V_{DD}	V	$I_{QH} = 5$ mA
L-output voltage	V_{QL}	0		0.5	V	$I_{QL} = 5$ mA

AC Characteristics

$T_A = 25\,°C$

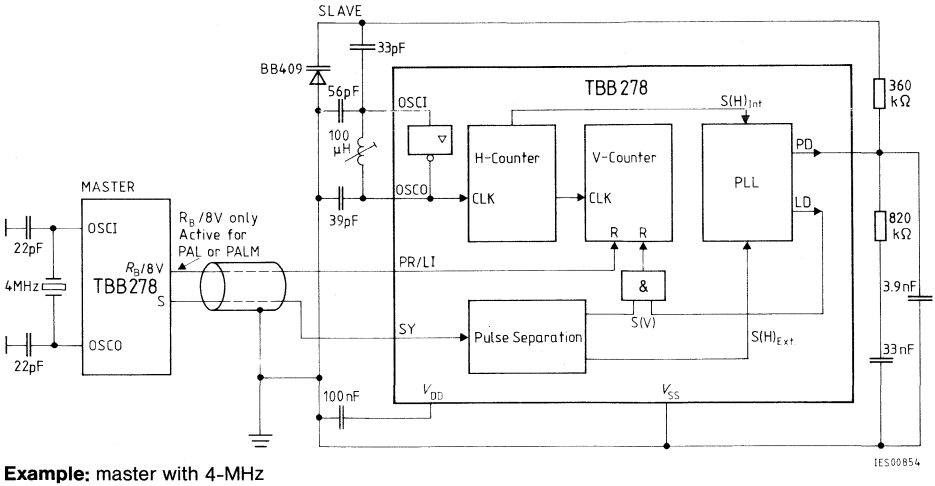
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Inputs						
CL/N_A						
Clock period	t_{CL}	1			µs	
D/N_B						
Data setup	t_{SD}	50			ns	
Data hold	t_{HD}	50			ns	
EPS						
Transfer pulse, duration	t_L			2	µs	
Propagation time	t_P			50	ns	OSCO clock edge to signal o/p
PR/LI						
PAL square reset, duration	t_{PR}	100			ns	
Outputs						
H_{Imp}, S, F_R						
Rise time	t_{LH}			15	ns	$C_L = 20$ pF
Fall time	t_{HL}			5	ns	$C_L = 20$ pF
H/2, B(H), C_t, B, V_{Imp}						
PI/N_C, BC/N_D, PS/SW, $R_B/8V$						
Rise time	t_{LH}			50	ns	$C_L = 20$ pF
Fall time	t_{HL}			20	ns	$C_L = 20$ pF

Synchronization

(applies to parallel and serial programming)

Synchronization of Slave with Combined S Signal

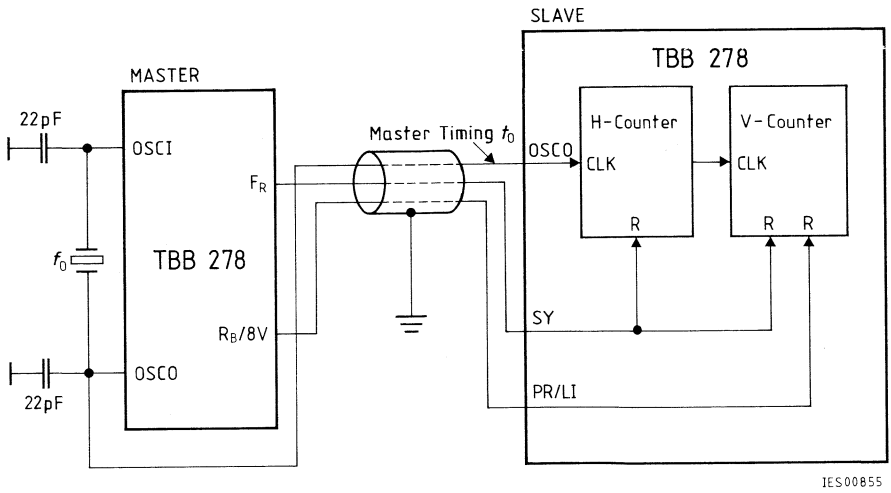
A PLL compares the phase of the internal and external S (H) pulses and adjusts the oscillator frequency accordingly. The S(V) signal resets the V counter to the beginning of the field if the phase difference between the external and internal S(H) pulse is smaller than $\pm 8\ t_0$ (see Lock Detect LD). Master and slave must be programmed for the same system (same number of lines and equalizing signals). V_{Imp}, F_R and B will not appear on the slaves' outputs if the line number of the master is smaller than that of the slave, the S(V) signal will be shortened by one V_{sync} pulse.



Example: master with 4-MHz crystal oscillator for PAL 625. slave with LC oscillator and PD filter.

Synchronization with Master Timing and F_R Reset

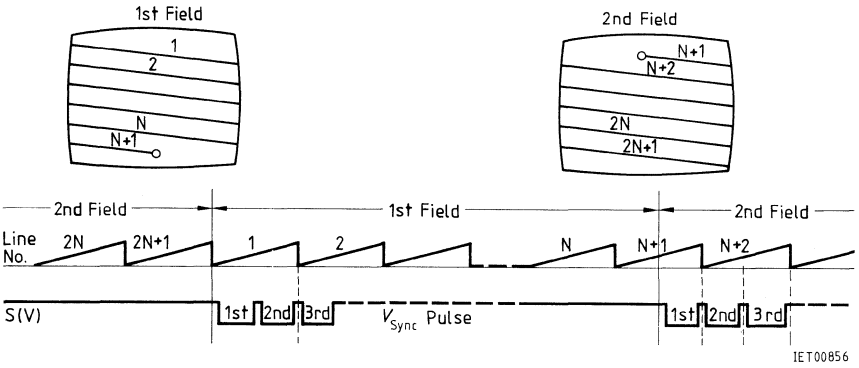
Same timing: master and slave are synchronous. After any disturbance the next falling edge of F_R resets the V counter to the beginning of the frame and the H counter to the beginning of the line. The supply to the oscillator inverter is disabled and thus OSCI too.



This kind of synchronization is advisable for high-definition systems because less jitter is produced than with the PLL.

Line Interlacing
(applies to even and odd numbers of equalizing pulses)

Systems with Line Interlacing



The 1st field begins with a whole line and ends after a half.

The 2nd fields begins with a half line and ends with a whole one, so it is automatically written into the spaces between the lines of the 1st field.

Both fields are initiated by the 1st V_{sync} pulse, each have (N + 1/2) lines and produce a frame of (2N + 1) lines.
(NB: Because of the finite picture flyback time the first lines of a field are not as visible as illustrated above).

Systems without Line Interlacing

The same field is written each time, into the same raster as the previous one. The field begins and ends with a whole line.

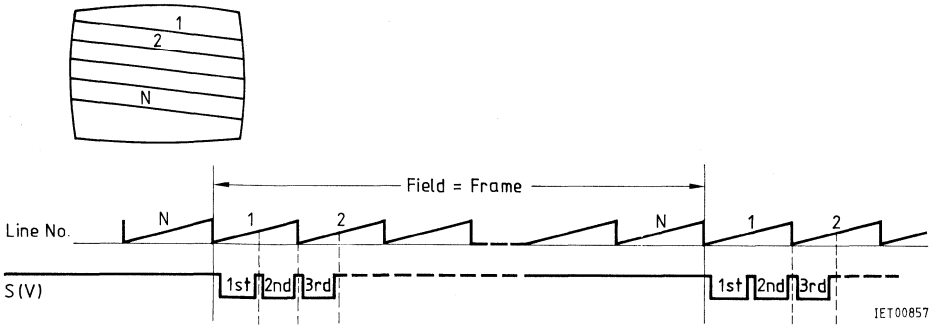


Figure 1
Timing Diagram for PR/LI Signal

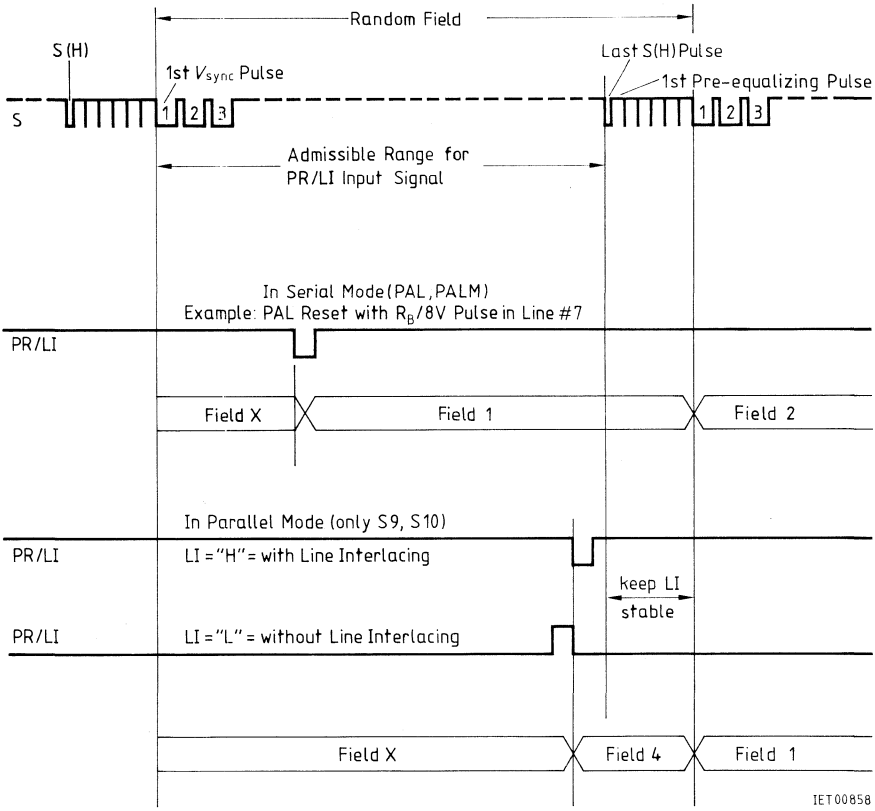


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Figure 2
Pulse Diagram for Parallel Programming

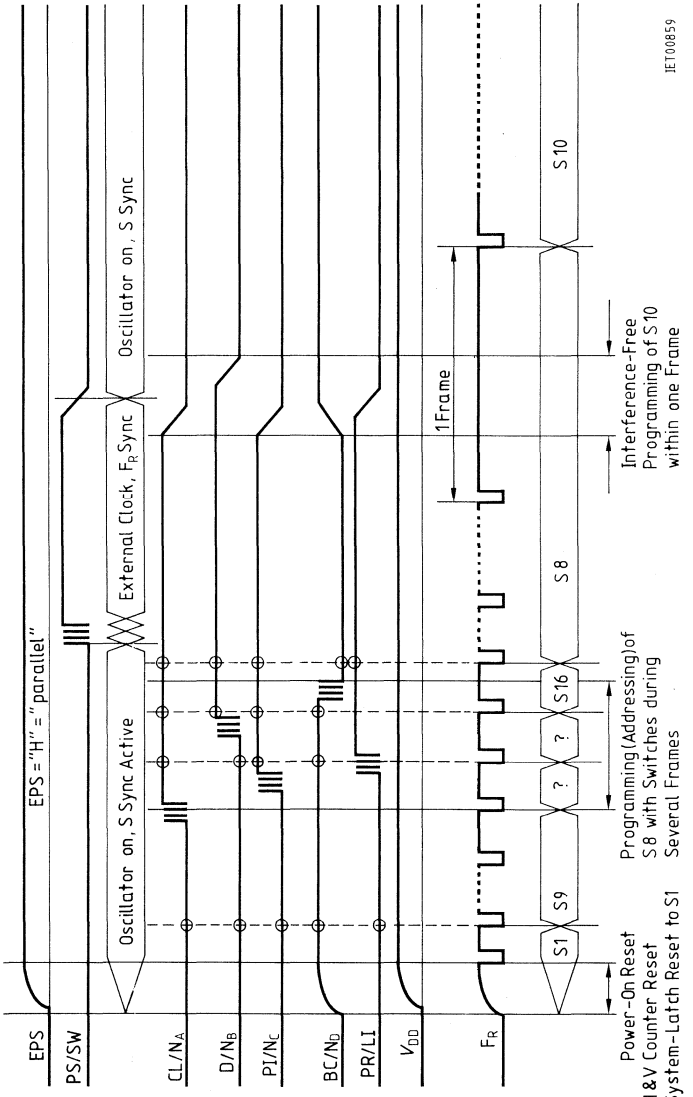

Table 1
Parallel Programming

System	Lines per frame	Lines per field	Picture Frequency/Hz frame	field	No. of Equ. & Int.	f_{OSC} /MHz	f_O /µs	remarks	Coding EPS	PR/ LI	BC/ N_D	PI/ N_C	D/ N_B	CL/ N_A	PS/ SW
S1	625	312 1/2	25	50	5	4.000	0.5	**For LI = "L":** Number of lines/field is reduced by 1/2 to eliminate line interlacing.	H	H	L	L	L	L	**"H"** external clock with f_R-synchronization
S2	525	262 1/2	30	60	6	4.032	0.49603		H	H	L	L	L	H	
S3	735	367 1/2	30	60	6	5.6448	0.3543		H	H	L	L	H	L	
S4	875	437 1/2	25	50	5	5.600	0.3571		H	H	L	L	H	H	
S5	1125	562 1/2	30	60	10	8.640	0.23148	**For LI = "L":** Frame frequency is doubled	H	H	L	H	L	L	**or "L"** Oscillator mode with S-synchronization
S6	1023	511 1/2	30	60	6	3.92832	0.2546		H	H	L	H	L	H	
S7	1249	624 1/2	25	50	6	3.9968	0.2502		H	H	L	H	H	L	
S8	1249	624 1/2	40	80	none	12.7898	0.1564		H	H	L	H	H	H	
S9	3x256, 1x255			120	6	3.92832	0.2556	**for LI = "H":** Number of lines/field is reduced by 1/2	H	L*)	H	L	L	L	
S10	3x312, 1x313			100	6	3.9968	0.2502		H	L*)	H	L	L	H	
S11	1023			30	12	3.9283	0.2546	**for LI = "H":** Number of lines/field is increased by 1/2 to produce line interlacing	H	L	H	L	H	L	
S12	1249			25	12	3.9968	0.2502		H	L	H	L	H	H	
S13	2046			3	24	0.785664	1.2728		H	L	H	H	L	L	
S14	2498			2.5	24	0.79936	1.251		H	L	H	H	L	H	
S15	1251	625 1/2	25	50	6	3.9968	0.2502	**for LI = "L":** like in S1 thru S8	H	H	H	H	H	L	
S16	1125	562 1/2	30	60	10	8.64	0.23148		H	H	H	H	H	H	

*) PR/LI: falling edge sets TBB 278A to 1rst field

Table 2
Pulse Widths for Systems Selectable in Parallel Mode

Parallel system / Output signals		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Lines/frame		625	525	735	875	1125	1023	1249	1249	3x256 1x255	3x312	1023	1249	2046 1x313	2498	1251	1125
Frame frequency	/Hz	25	30	30	25	30	30	25	40	120	100	30	25	3	2.5	25	30
field frequency	/Hz	50	60	60	50	60	60	50	80	-	-	-	-	-	-	50	60
H line period	/µs	64	63.492	43.35	45.71	-	32.78	32.02	-	32.58	32.02	32.583	32.025	162.92	160.12	32.026	29.629
Line frequency	/KHz	15.625	15.750	22.05	21.877	33.75	30.69	37.224	49.95	30.69	31.22	30.69	31.226	6.138	6.245	33.75	33.75
t_o = H/128 = $1/f_o$	/µs	.500	.49603	.3543	.3571	23148	.2546	.2502	.1564	.2556	.2502	.2546	.2502	1.2728	1.251	.02502	23148
t_{OSC}	/MHz	4.000	4.032	5.6448	5.600	8.64	3.92832	3.9968	12.7898	3.92832	3.9968	3.9283	3.9968	0.785664	0.79936	3.9968	8.64
$t_{OSC} = 1/f_{OSC}$ [1]		0.5 to	0.5 to	0.5 to	0.5 to	0.5 to	to	to	0.5 to	to	to	to	to	to	to	to	0.5 to
Blanking signal	B(H)	24 to	22 to	20 to	24 to	26 to	28 to	24 to	34 to	28 to	24 to	28 to	24 to	28 to	24 to	24 to	16 to
	B(V)	25 H	20 H	30 H	30 H	42 H		39 H	40 H		20 H		80 H		160 H	39 H	45 H
Vidicon blanking	RB(H)	19 to	19 to	19 to	19 to	-		19 to	-	-	-	-	-	-	-	19 to	-
signal	RB(V)	15 H	15 H	20 H	20 H	-		30 H	-	-	-	-	-	-	-	30 H	-
Front porch	D	3 to	3 to	3 to	3 to	3 to		3 to	3 to	3 to		3 to		3 to		3 to	3 to
H-pulse		14 to	13 to	14 to	14 to	10 to		10 to	10 to	10 to		10 to		10 to		10 to	10 to
V-pulse		10 H	9.5 H	14.5 H	15 H	5 H		20 H	20 H	10 H		40 H		80 H		20 H	20 H
Clamping pulse	C_t	2 to	3 to	2 to	2 to	3 to		3 to	-	3 to		3 to		3 to		3 to	2 to
C_t delay	DC_t	17 to	16 to	17 to	17 to	13 to		20 to	-	20 to		20 to		20 to		20 to	12 to
S signal	S(H)	9.5 to	9.5 to	7 to	7 to	10 to		11 to	10 to	10 to		10 to		10 to		11 to	2.5 to
Equalizing pulse	Equ.	4.5 to	4.5 to	4 to	4 to	5 to		5 to	-	4 to		4 to		4 to		5 to	2.5 to
V_{sync} interrupt	Int.	9.5 to	9.5 to	7 to	7 to	9 to		8 to	10 to[2]	7 to		7 to		7 to		8 to	3.5 to
No. of Equ. & Int. or DV_{imp}		5	6	6	5	10		6	-	6		12		24		6	10
		2.5 H	3 H	3 H	2.5 H	5 H		3 H	5 H	3 H		6 H		12 H		3 H	5 H

$f_o = 1/t_o = 128$ x line number (frame) x frame frequency

1) t_{OSC} = oscillator or external clock period. Prescaler is bypassed for $t_{OSC} = t_o$ (Systems S6, S7, S9 thru S14)

2) No Equ. & Int. in middle of line. Int. corresponds to S(H) shifted. **See figures 4 and 5.**

Figure 3
Pulse Diagram for Serial Programming

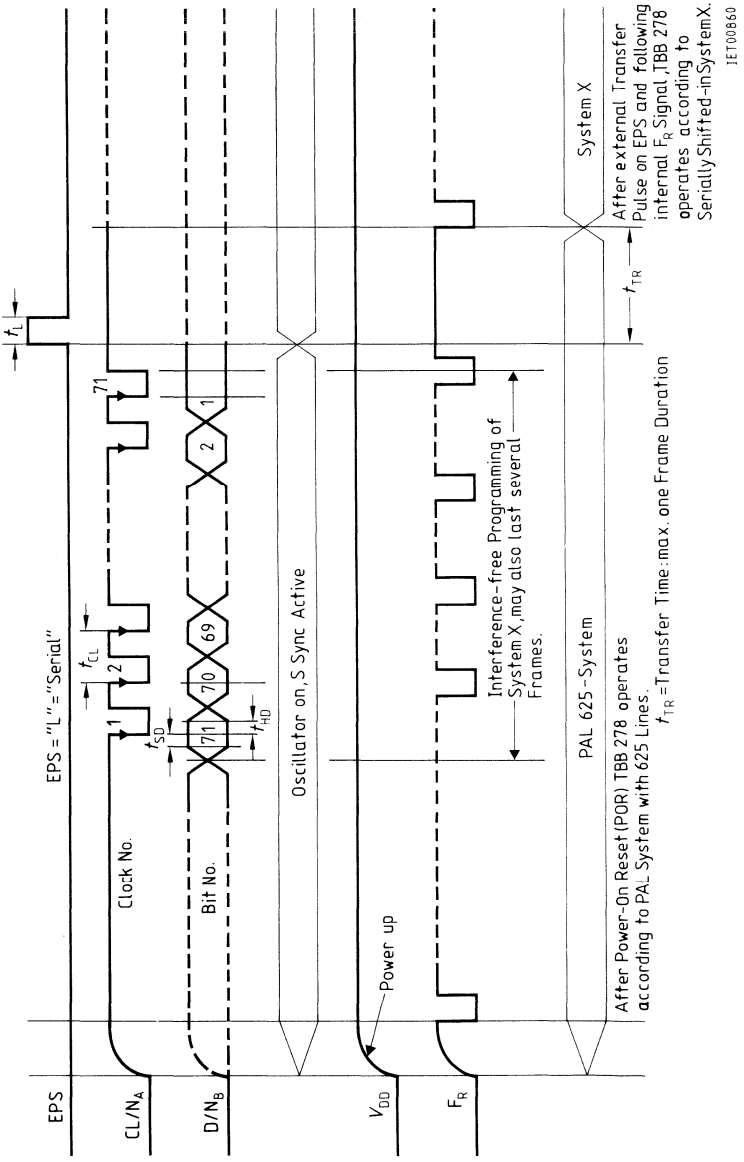

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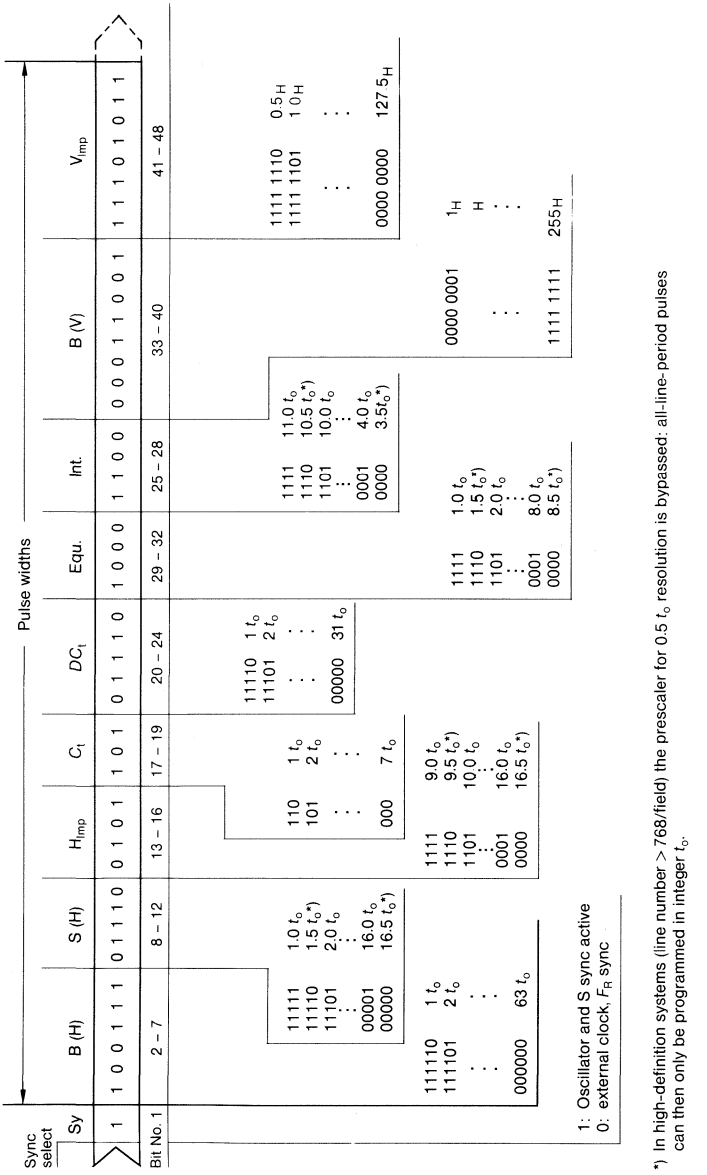
Table 3

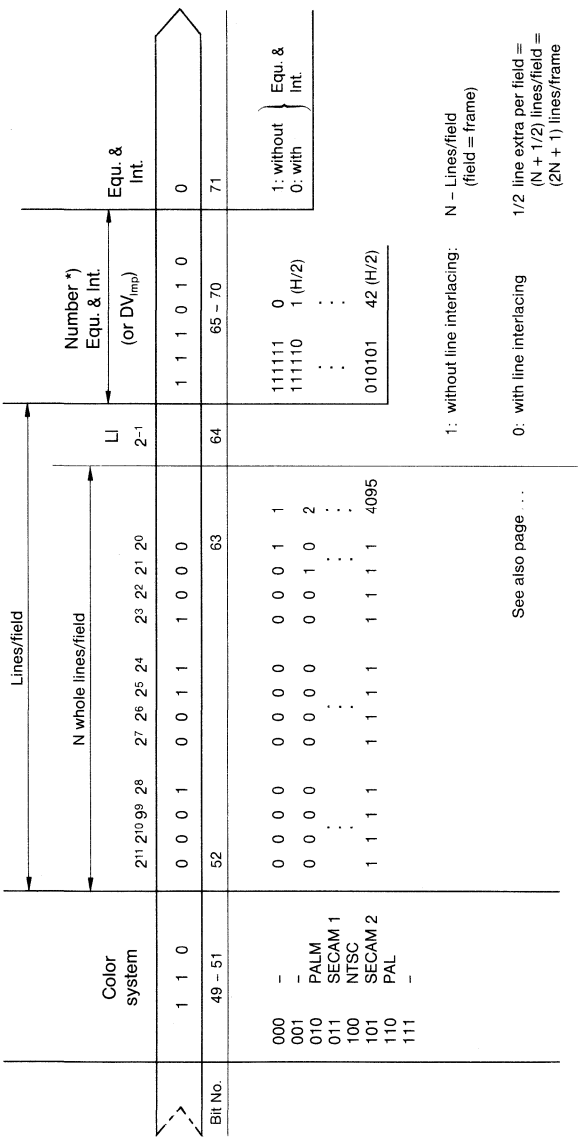
Coding for Serial Programming

As an example the PAL system with 625 lines is entered in the register, which is written in automatically at power-on reset.



*) In high-definition systems (line number > 768/field) the prescaler for 0.5 t_o resolution is bypassed: all-line-period pulses can then only be programmed in integer t_o.

Table 3 (continued)
Coding for Serial Programming



*) Number Equ. & Int. = number of pre-equalizing pulses = number of V_{sync} pulses = number of post-equalizing pulses. Different numbers of equalizing and V_{sync} pulses cannot be programmed.

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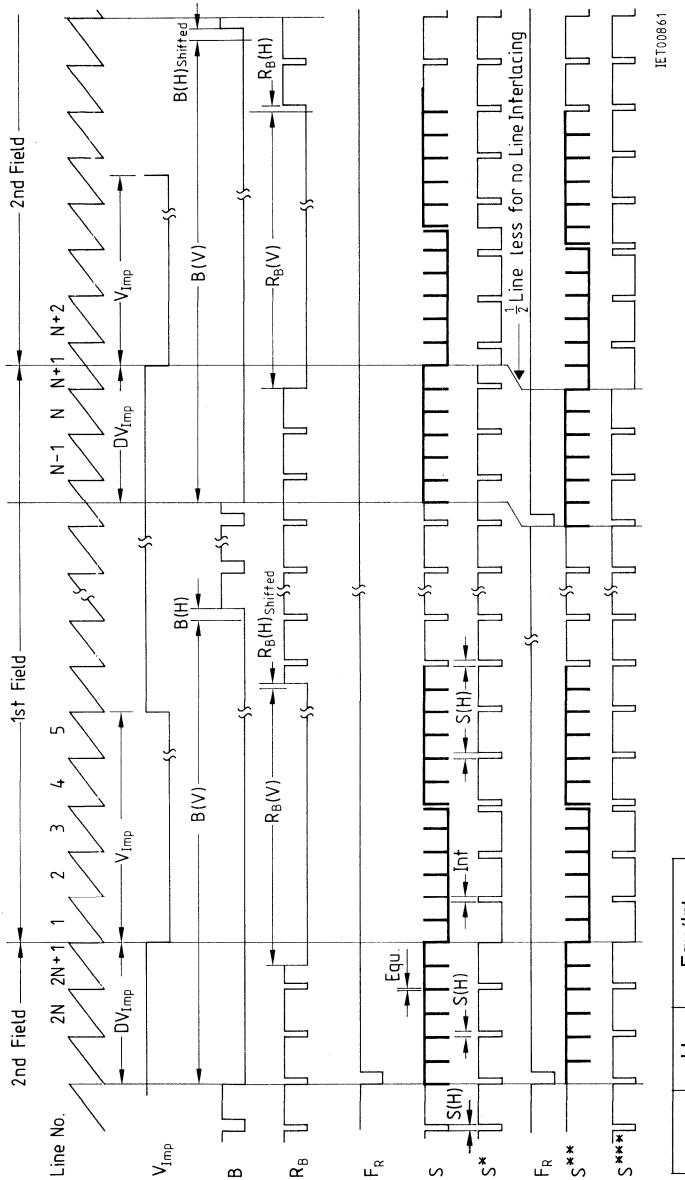
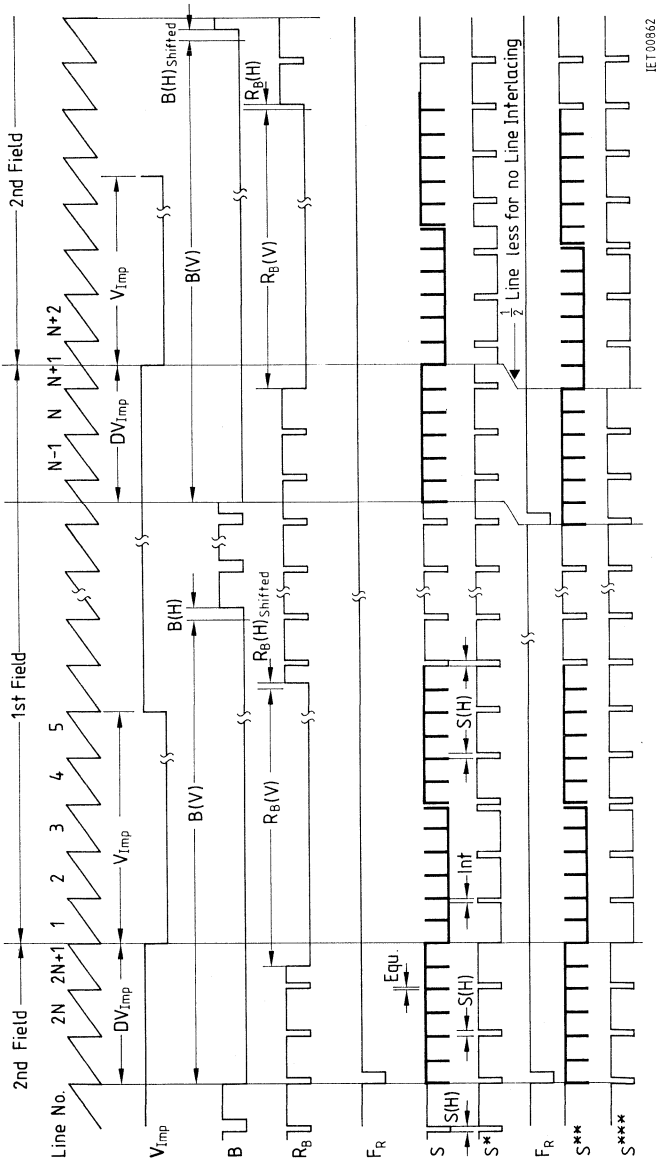
Figure 4
Composite Frame Signals for Even Number of Equalizing Pulses



	LI	Equ/Int
S	x	x
S*	x	—
S**	—	x
S***	—	—

Figure 5
Composite Frame Signals for Odd Number of Equalizing Pulses



	LI	Equ/Int
S	x	x
S*	x	—
S**	—	x
S***	—	—

Figure 6
Line-Period Output Signals

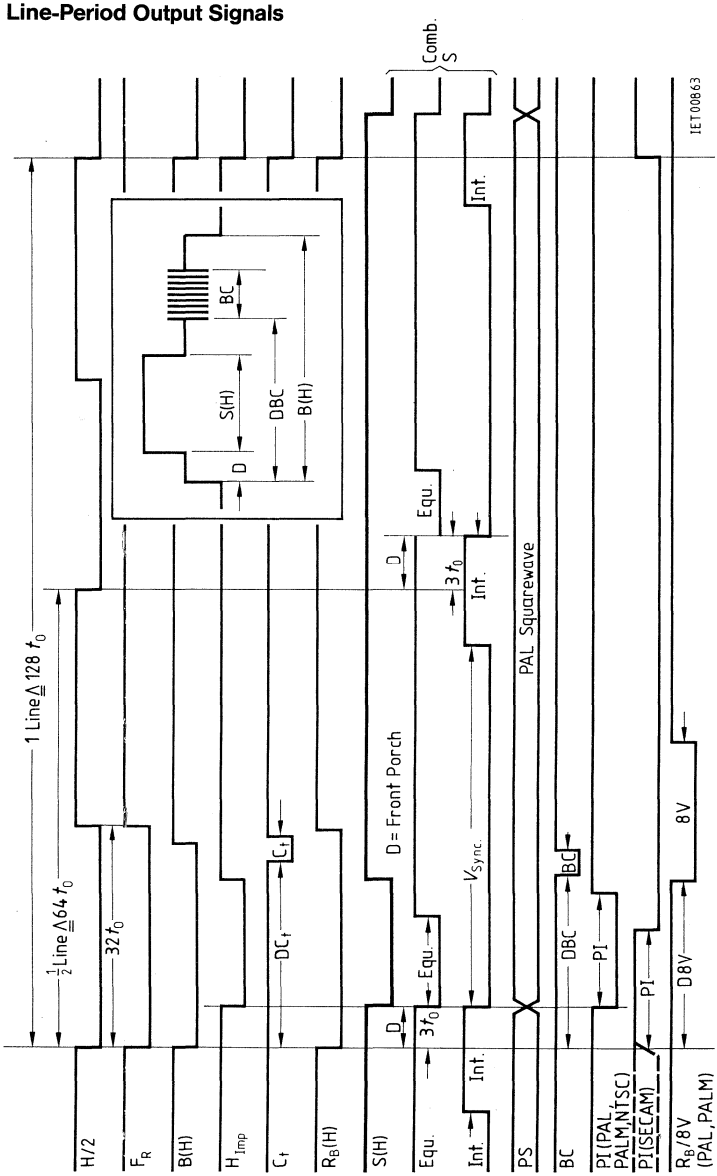


Table 4
Pulse Widths for Auxiliary Color Signals

	PAL	SECAM	NTSC	PAL-M
S, H_{imp}, V_{imp}, V_R, B, B(H), C_t	refer to parallel system S1		refer to parallel system S2	
t_o	0.5 µs	0.5 µs	0.4965 µs	0.4965 µs
BC	2.25 µs 4.5 t_o	7.00 µs 14.0 t_o	2.5 µs 5 t_o	2.5 µs 5 t_o
DBC	7.00 µs 14.0 t_o	0	6.75 µs 13.5 t_o	7.25 µs 14.5 t_o
PI	4.75 µs 9.5 t_o	12.00 µs 24 t_o	–	4.75 µs 9.5 t_o
RB/8V	10 µs 20. t_o	–	–	10 µs 20 t_o
D8V	13.5 µs 27.0 t_o	–	–	13.5 µs 27.0 t_o
Field:		BC suppression (line number)*)		
4-1	623 ... 6	622.5 ... 22	523 ... 6	523 ... 8
1-2	310 ... 318	311. ... 335	261 ... 269	260 ... 270
2-3	622 ... 5	622.5 ... 22	523 ... 6	522 ... 7
3-4	311 ... 319	311. ... 335 **)	261 ... 269	259 ... 269

*) Assumption: line # 1 begins in all systems with the first V_{sync} pulse
**) In SECAM 1 BC appears during lines 7-15 and 320-328

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Figure 7
Color Identification Signals in PAL

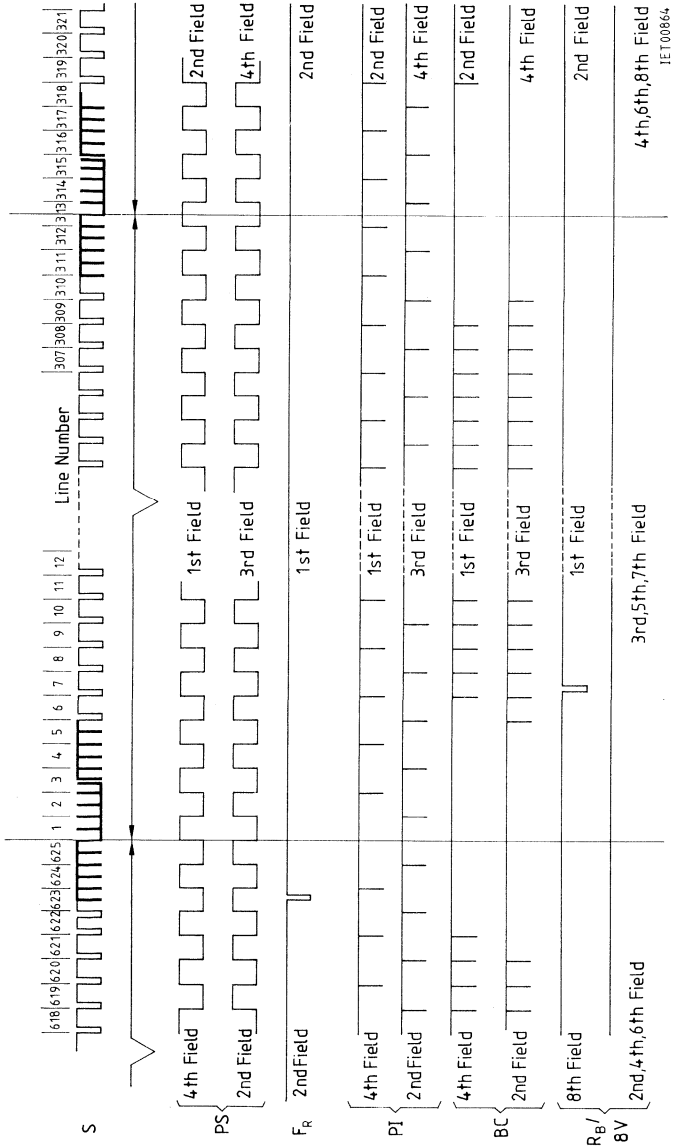


Figure 8
Color Identification Signals in SECAM

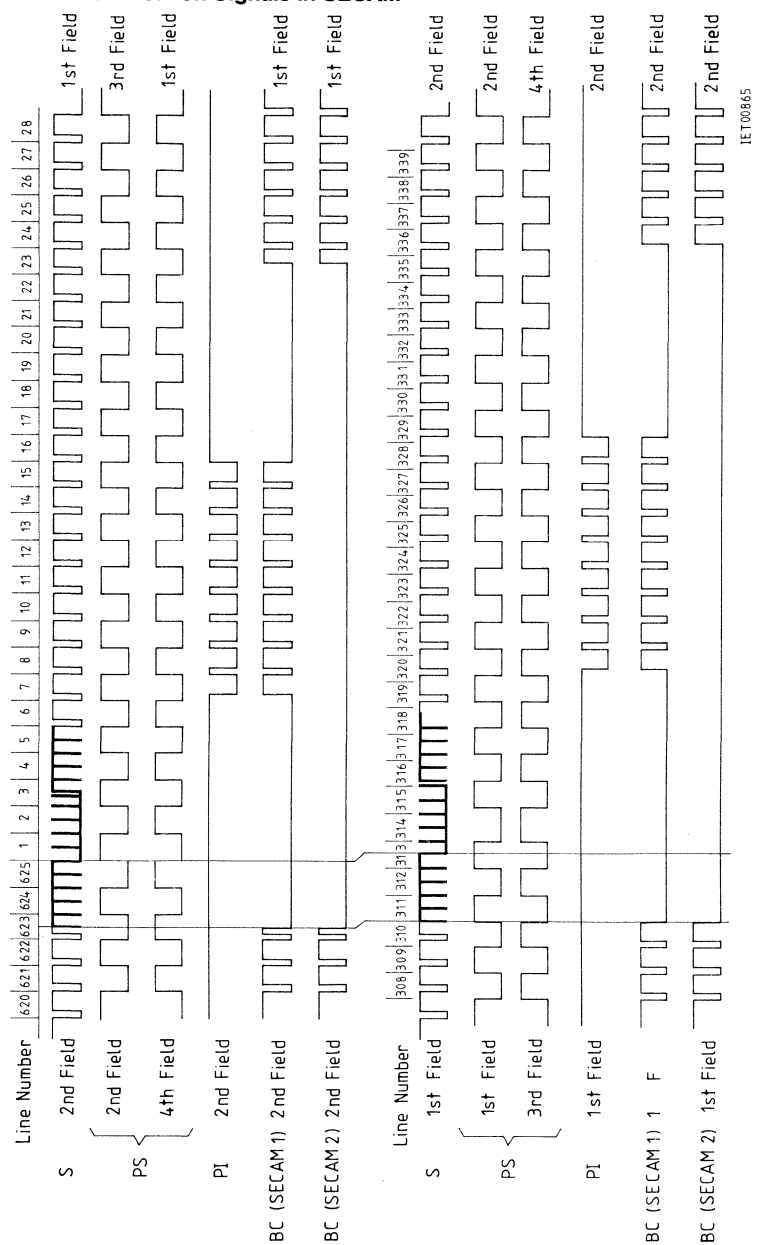
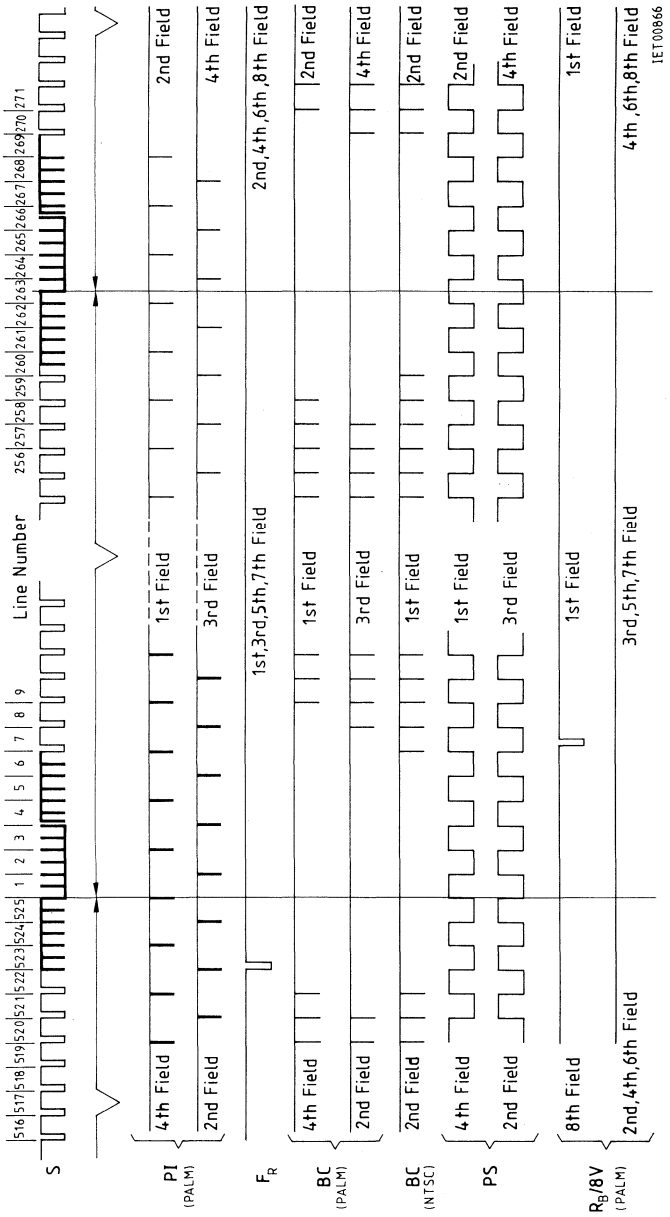
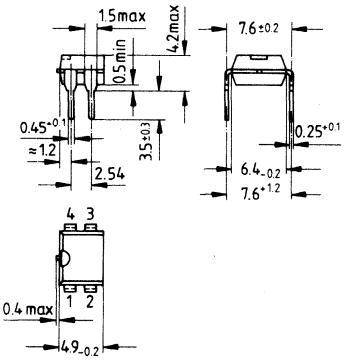


Figure 9
Color Identification Signals in NTSC and PAL-M



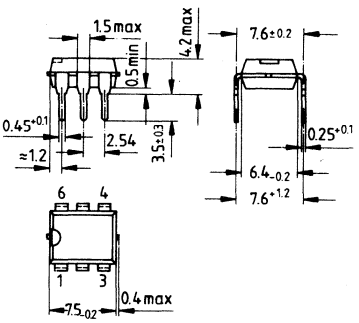
Package Outlines

Plastic Dual-in Line Package, P-DIP-4
20 A 4 DIN 41866



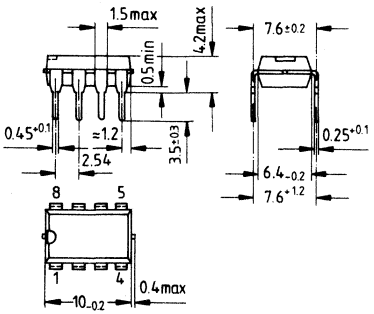
Approx. weight 0.5 g

Plastic Dual-in-Line Package, P-DIP-6
20 A 6 DIN 41866



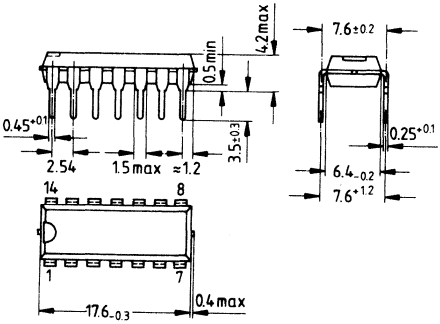
Approx. weight 0.7 g

Plastic Dual-in-Line Package, P-DIP-8
20 A 8 DIN 41870 T9



Approx. weight 0.7 g

Plastic Dual-in-Line Package, P-DIP-14
20 A 14 DIN 41870 T9

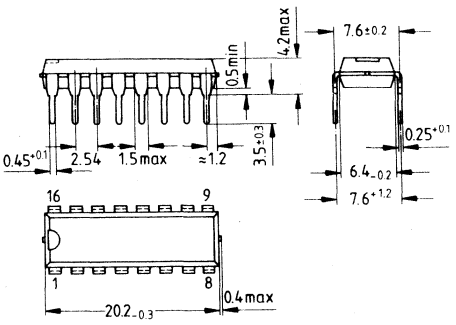


Approx. weight 1.1 g

Dimensions in mm

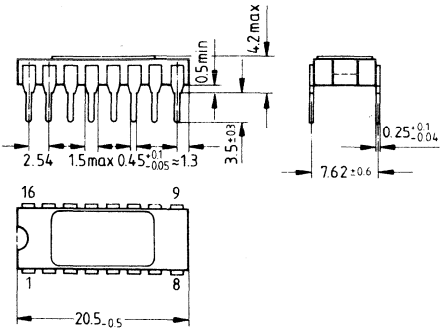
Note: Packages not listed here are on request.

Plastic Dual-in-Line Package, P-DIP-16
20 A 16 DIN 41870 T9



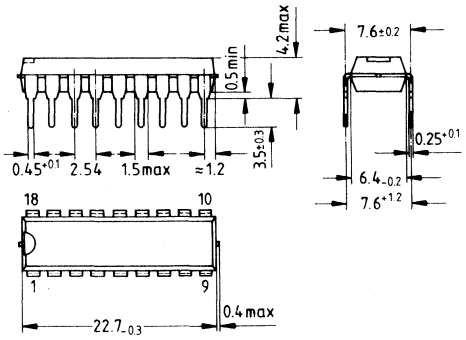
Approx. weight 1.2 g

Ceramic Dual-in-Line Package, C-DIP-16
20 A 16 DIN 41870 T9



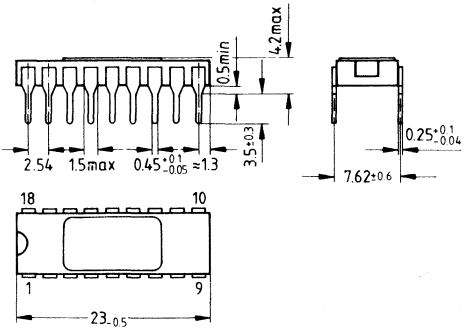
Approx. weight 1.4 g

Plastic Dual-in-Line Package, P-DIP-18
20 A 18 DIN 41870 T9



Approx. weight 1.3 g

Ceramic Dual-in-Line Package, C-DIP-18
20 A 18 DIN 41870 T9



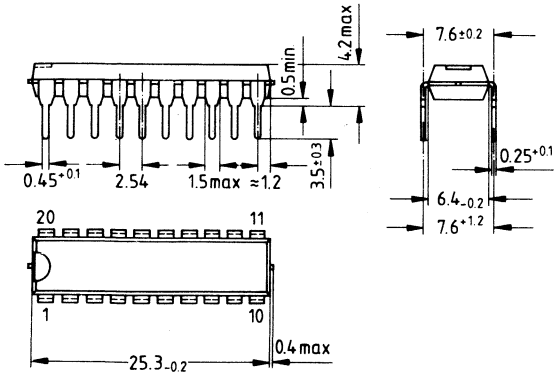
Approx. weight 1.7 g

Dimensions in mm

Note: Packages not listed here are on request.

Package Outlines

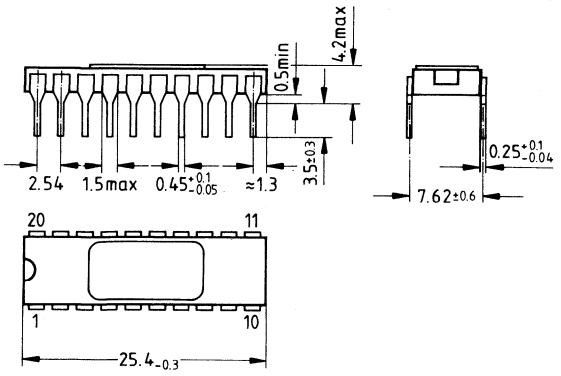
Plastic Dual-in-Line Package, P-DIP-20
20 A 20 DIN 41870 T9



Approx. weight 1.5 g

Ceramic Dual-in-Line Package, C-DIP-20
20 A 20 DIN 41870 T9

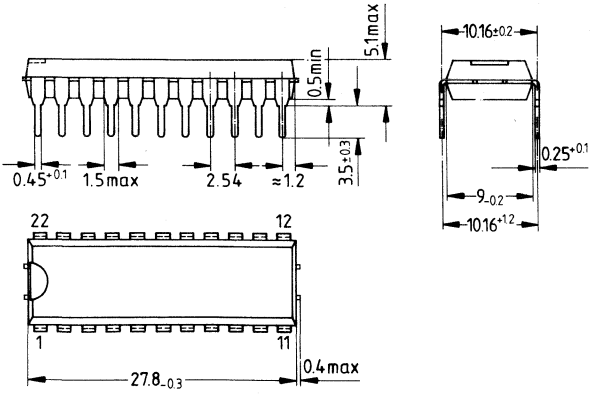
Dimensions in mm



Approx. weight 1.7 g

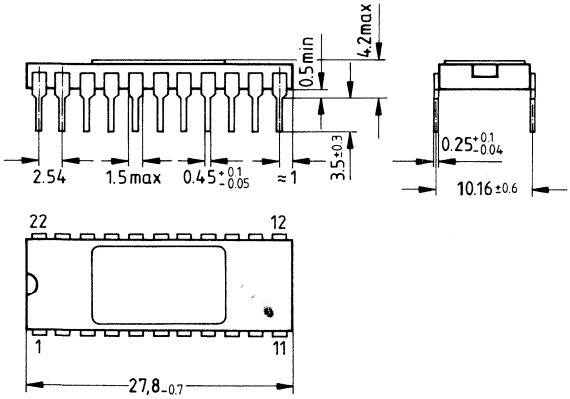
Note: Packages not listed here are on request.

Plastic Dual-in-Line Package, P-DIP-22
20 D 22 DIN 41870 T11



Approx. weight 2.1 g

Ceramic Dual-in-Line Package, C-DIP-22
20 D 22 DIN 41870 T11



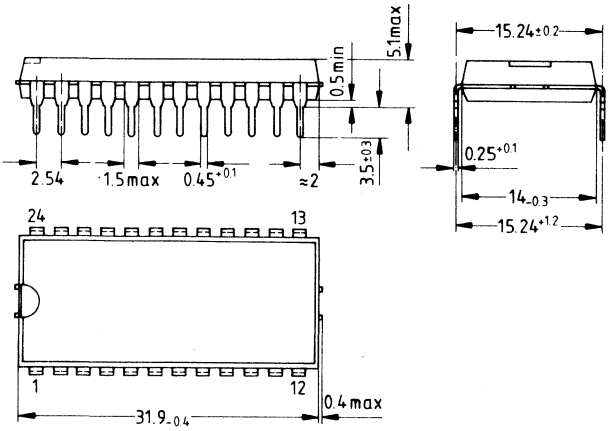
Approx. weight 2.5 g

Dimensions in mm

Note: Packages not listed here are on request.

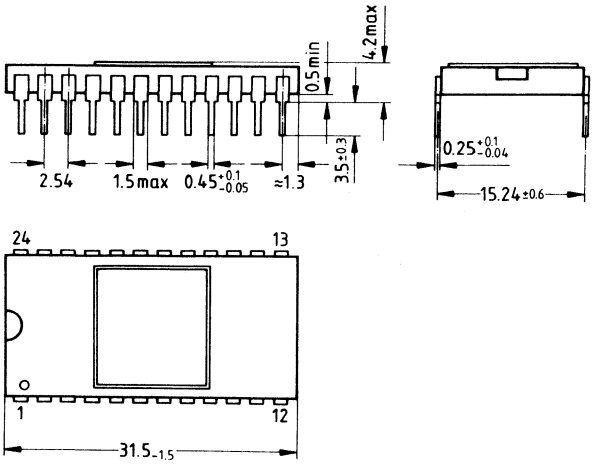
Package Outlines

Plastic Dual-in-Line Package, P-DIP-24
20 B 24 DIN 41870 T10



Approx. weight 2.5 g

Ceramic Dual-in-Line Package, C-DIP-24
20 B 24 DIN 41870 T10

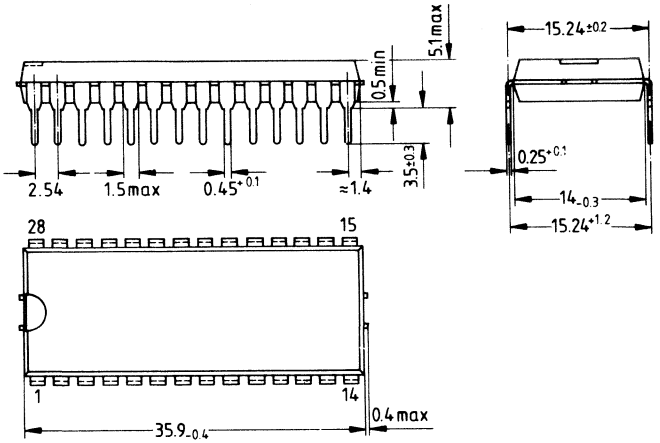


Dimensions in mm

Approx. weight 3 g

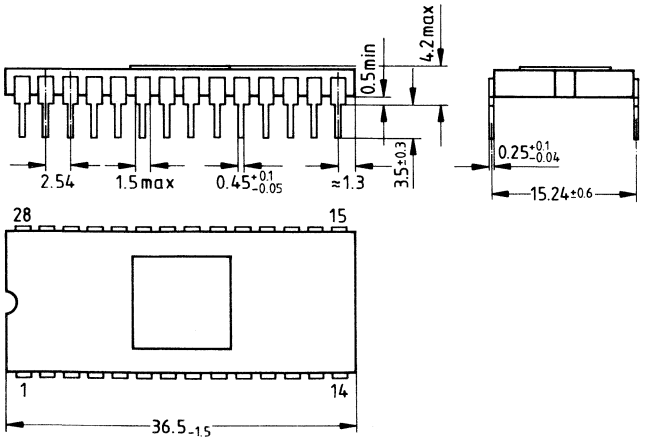
Note: Packages not listed here are on request.

Plastic Dual-in-Line Package, P-DIP-28
20 B 28 DIN 41870 T10



Approx. weight 3 g

Ceramic Dual-in-Line Package, C-DIP-28
20 B 28 DIN 41870 T10



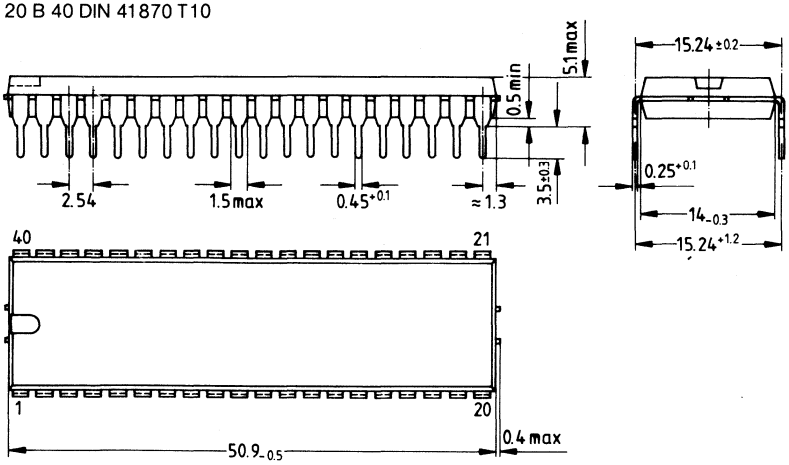
Approx. weight 3.5 g

Dimensions in mm

Note: Packages not listed here are on request.

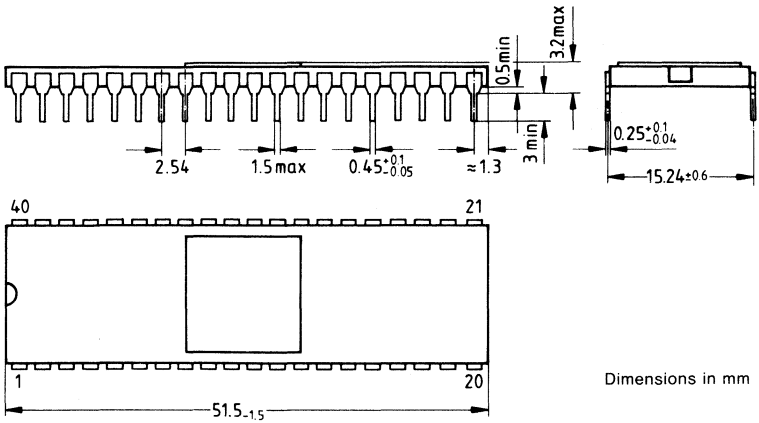
Package Outlines

Plastic Dual-in-Line Package, P-DIP-40
20 B 40 DIN 41870 T10



Approx. weight 5.9 g

Ceramic Dual-in-Line Package, C-DIP-40
20 B 40 DIN 41870 T10

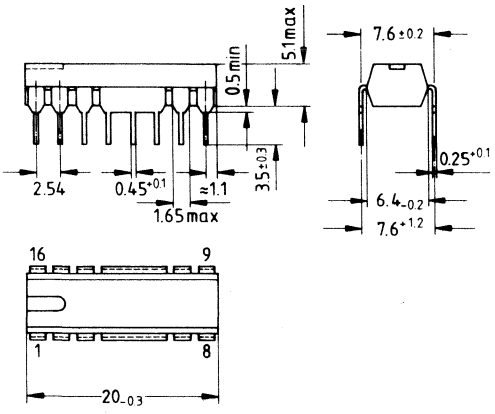


Dimensions in mm

Approx. weight 6.8 g

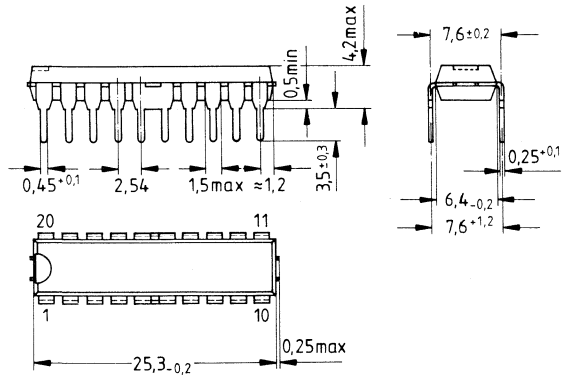
Note: Packages not listed here are on request.

Plastic Dual-in-Line Package for Power Applications, P-DIP-16-L-10
20 A 16 DIN 41870 T9



Approx. weight 1.1 g

Plastic Dual-in-Line Package, P-DIP-20-L-16
20 A 20 DIN 41870 T9



Note: Packages not listed here are on request.

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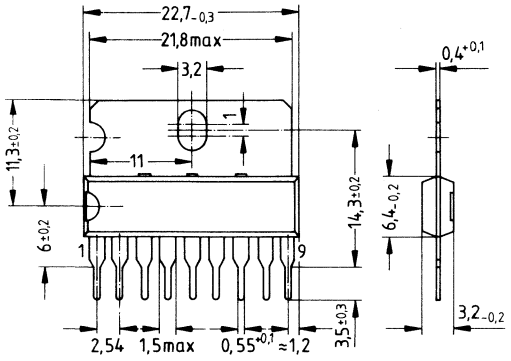
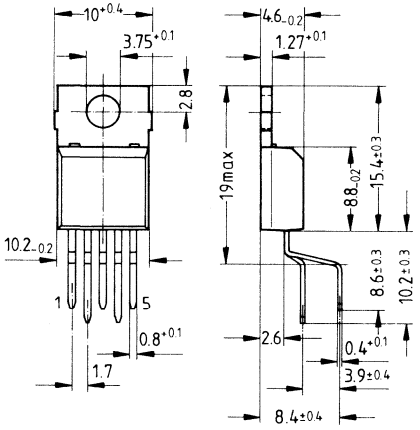
Package Outlines

Plastic Single-in-Line Package, P-SIP-9



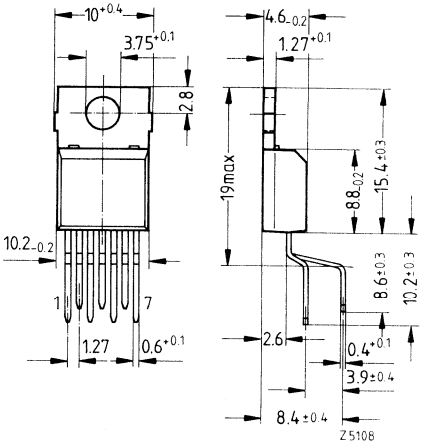
Gewicht etwa 1,9 g

Plastic Power Package, P-T66-5-H
(similar to TO-220)



Approx. weight 2.1 g

Plastic Power Package, P-T66-7-H
(similar to TO-220)

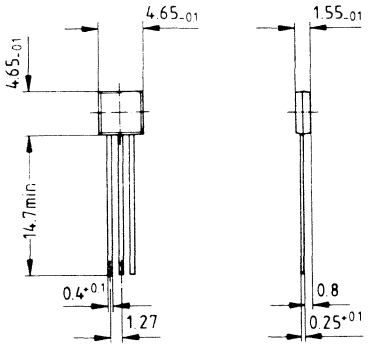


Dimensions in mm

Note: Packages not listed here are on request.

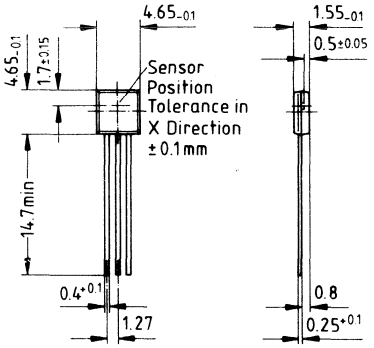
Package Outlines

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4303F/4304)



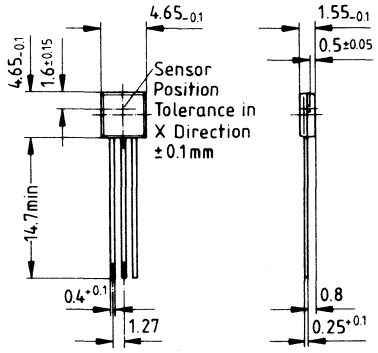
Approx. weight 0.1 g

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4901 F)



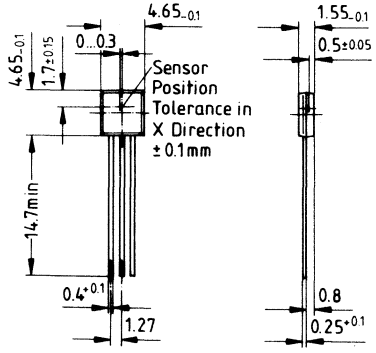
Approx. weight 0.1 g

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4902 F)



Approx. weight 0.1 g

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4903 F)



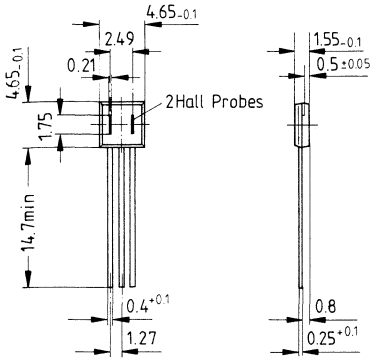
Approx. weight 0.1 g

Dimensions in mm

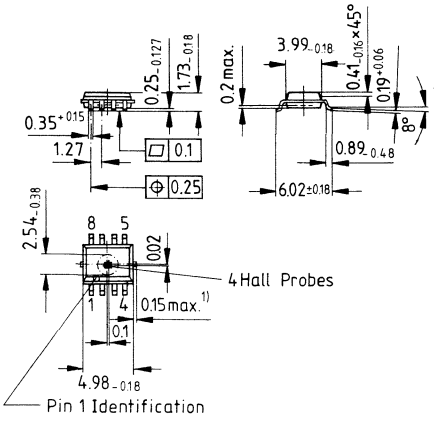
Note: Packages not listed here are on request.

Package Outlines

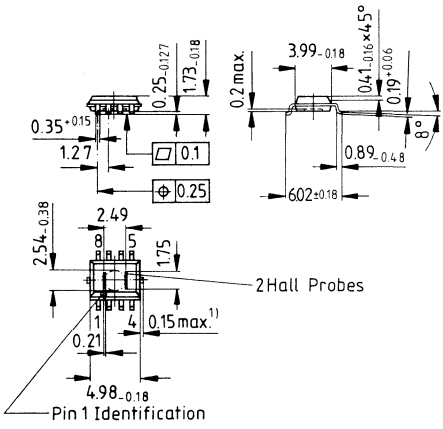
Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4920 F)



Miniature Plastic Dual-in-Line Package, P-DSO-8 (SMD) Small Outlines
(e.g. TLE 4910 G)



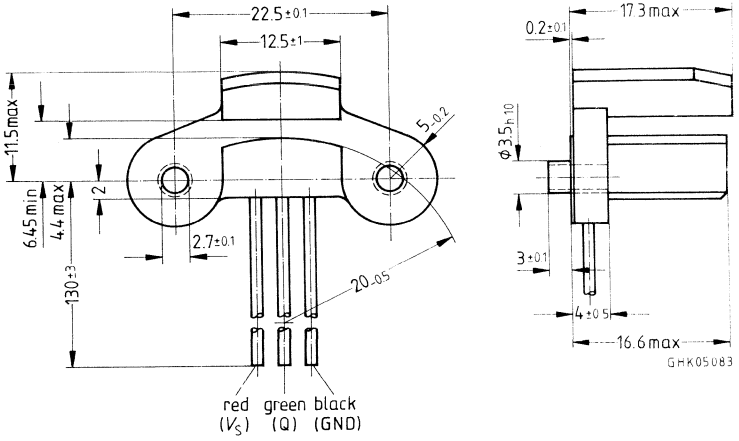
Miniature Plastic Dual-in-Line Package, P-DSO-8 (SMD) Small Outlines
(e.g. TLE 4920 G)



Note: Packages not listed here are on request.

SMD = Surface Mounted Device

Special Package



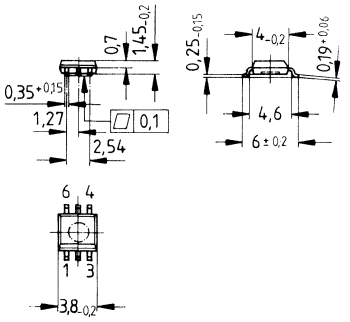
Approx. weight 8.5 g

Dimensions in mm

Note: Packages not listed here are on request.

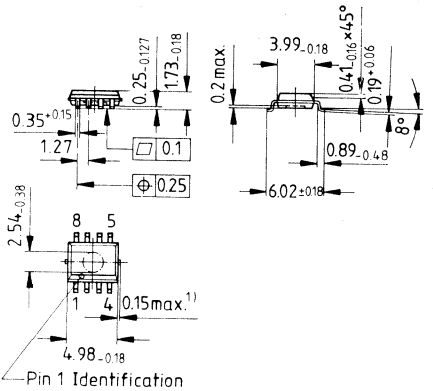
Package Outlines

Miniature Plastic Dual-in-Line Package,
P-DSO-6 (SMD) Small Outlines
24 A 6 DIN 41870 T16



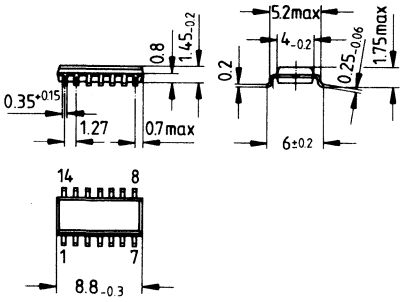
Approx. weight 0.1 g

Miniature Plastic Dual-in-Line Package,
P-DSO-8 (SMD) Small Outlines
24 A DIN 41870 T16



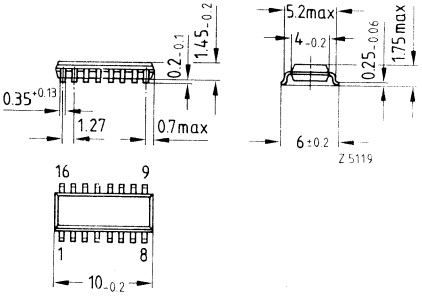
Approx. weight 0.15 g

Miniature Plastic Dual-in-Line Package,
P-DSO-14 (SMD) Small Outlines
24 A 14 DIN 41870 T16



Approx. weight 0.2 g

Miniature Plastic Dual-in-Line Package,
P-DSO-16 (SMD) Small Outlines
24 B16 DIN 41870

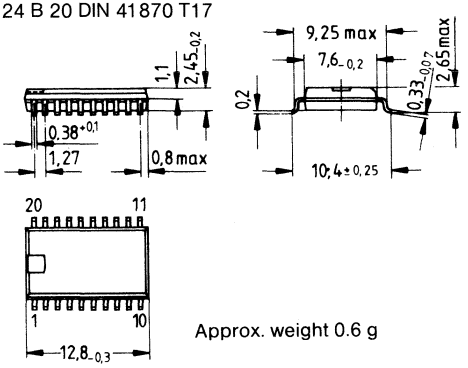


Dimensions in mm

Note: Packages not listed here are on request.

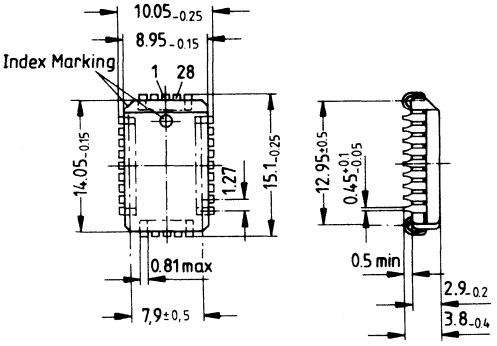
SMD = Surface Mounted Device

Miniature Plastic Dual-in-Line Package, P-DSO-20 (SMD) Small Outlines
24 B 20 DIN 41870 T17

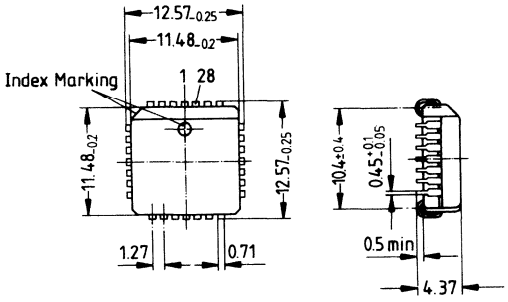


Approx. weight 0.6 g

Plastic-Leaded Chip Carrier, PL-CC-28-R (SMD)



Plastic-Leaded Chip Carrier, PL-CC-28 (SMD)

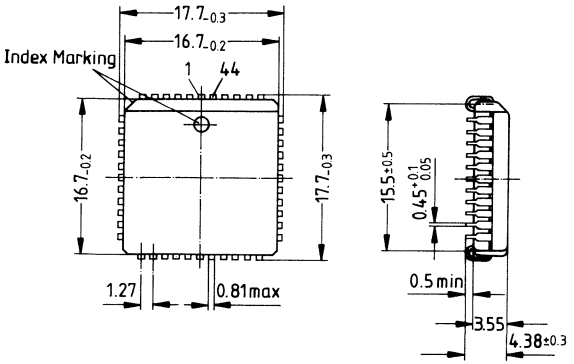


Dimensions in mm

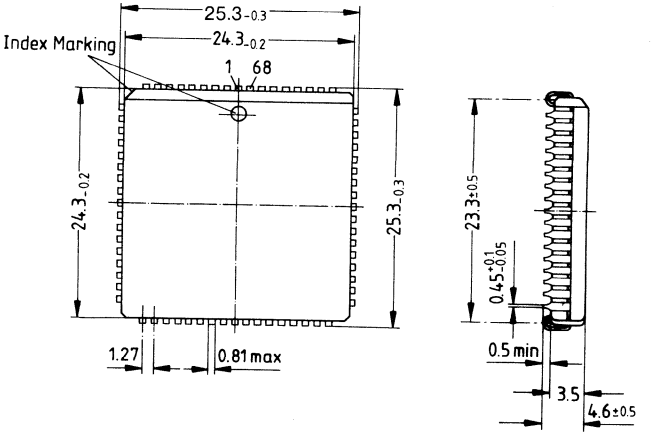
Note: Packages not listed here are on request.

SMD = Surface Mounted Device

Plastic-Leaded Chip Carrier, PL-CC-44 (SMD)



Plastic-Leaded Chip Carrier, PL-CC-68 (SMD)



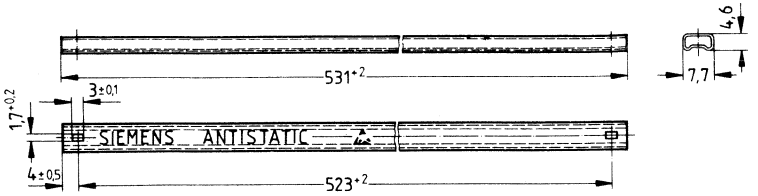
Dimensions in mm

Note: Packages not listed here are on request.

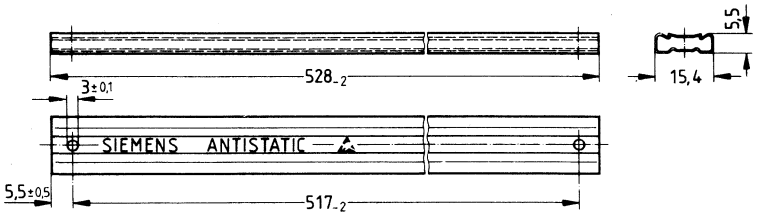
SMD = Surface Mounted Device

Packaging Tubes

Packages: P-DSO-6; 8; 14; P-MIP-6-G; 8-G



Packages: P-DSO-16; P-DSO-20



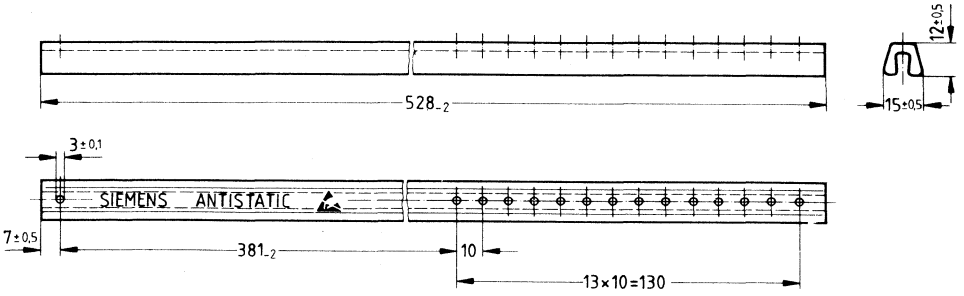
Dimensions in mm

Note: Packages not listed here are on request.

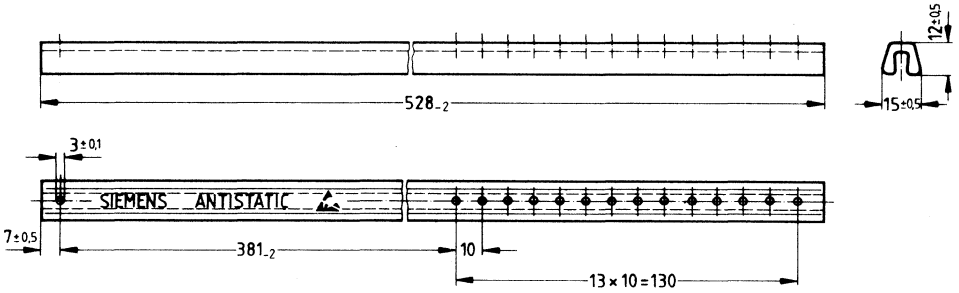
ESD-Protection Packing

Packaging Tubes

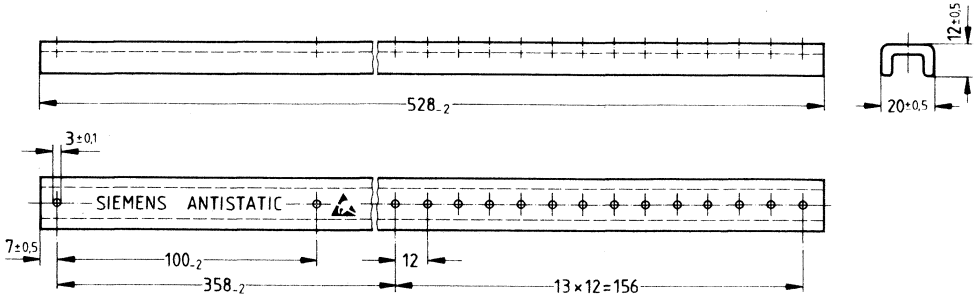
Packages: P-DIP-4; 6; 8; 14; 16; 18; 20



Packages: C-DIP-14; 16; 18; 20



Packages: C-DIP-24; 28; 40; 48

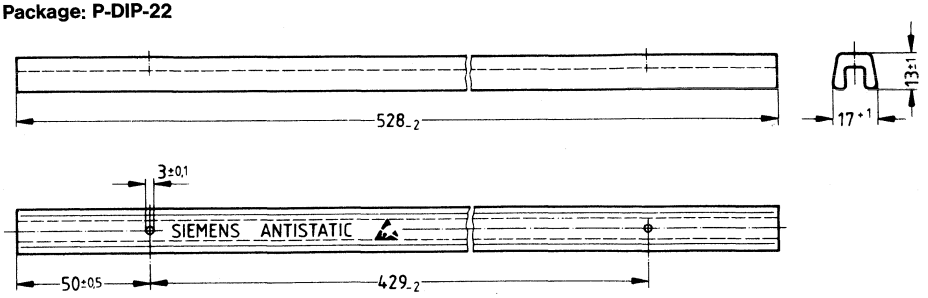


Dimensions in mm

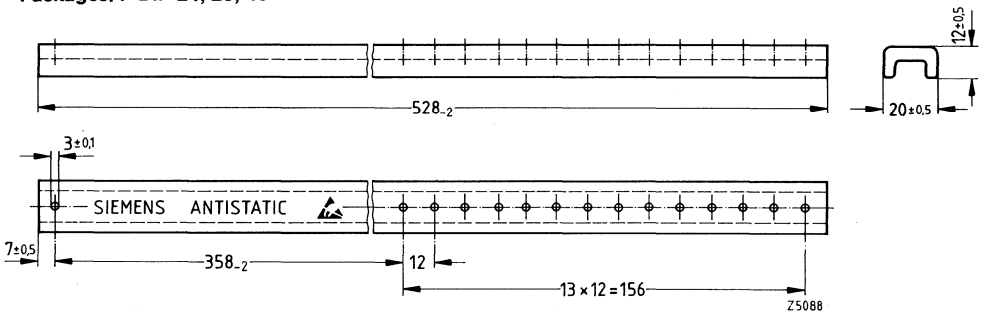
Note: Packages not listed here are on request.

Packaging Tubes

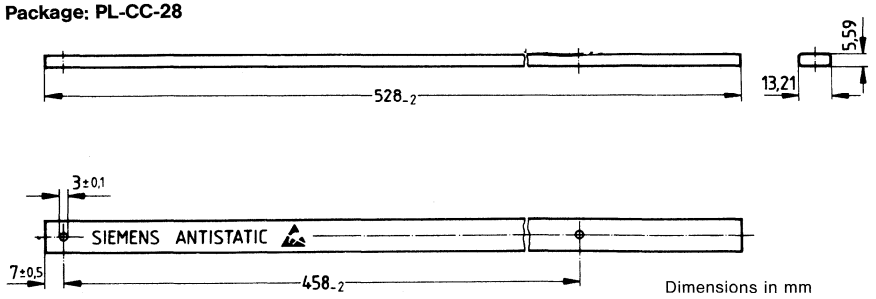
Package: P-DIP-22



Packages: P-DIP-24; 28; 40



Package: PL-CC-28



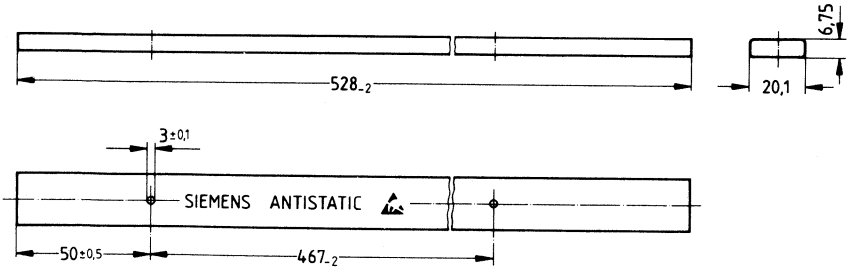
Dimensions in mm

Note: Packages not listed here are on request.

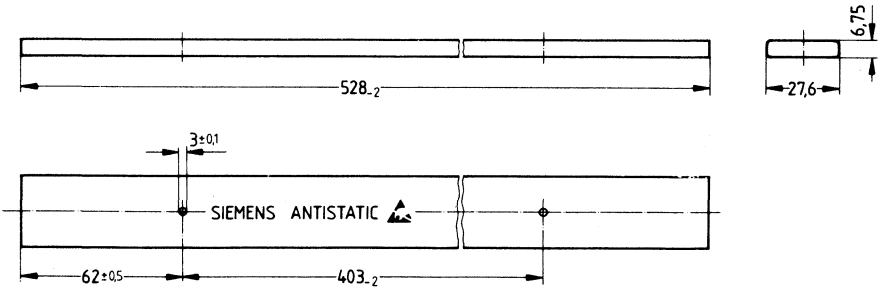
ESD-Protection Packing

Packaging Tubes

Package: PL-CC-44



Package: PL-CC-68



Dimensions in mm

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ICs für professionelle Schaltnetzteile (SNTs)	B1-B3919	
TDA 4918/4919 eine neue Generation von Schaltnetzteil-Bausteinen	B114-B6085	
New Generation of Control ICs for Switched-Mode Power Supplies	B114-B6085-X-X-7600	
IC für Induktive Näherungsschalter	B114-B6331-X-X-7400	
ICs for Inductive Proximity Switches		
Produktschriften/Product Information	B112-B6025	
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Notes

Notes

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2	Schwellenwertschalter, Komparatoren, Stromüberwachungs-IC	Threshold Switches, Comparators, Current Monitoring IC
3	Schaltnetzteile, 5 V Spannungsregler	Switched-Mode Power Supplies, 5 V Low-Drop Voltage Regulators
4	Treiber und Interfaceschaltungen Transistor Arrays	Drivers and Interface Circuits, Transistor Arrays
5	Thyristor und Triacansteuerungen	Control ICs for Thyristors and Triacs
6	A/D Umsetzer, Schnelle Datenakquisition	A/D Converters, High-Speed Data Acquisition
7	Zeitgeberschaltungen	Timer ICs
8	Tongeberschaltungen	Audible Signal ICs
9	Leistungs-OP, Leistungsbrücken, Spezielle Motoransteuerungen	Power Op Amps, DC Motor Drivers, Special Control ICs
0	Intelligente Leistungsschalter, Relaistreiber	Intelligent Low-Side and High-Side Switches Relay Drivers
1	ICs für Sensoranwendungen, Hall-IC, Näherungsschalter	ICs for Sensors, Hall-Effect ICs, Proximity Switches
2	Spezielle Speicher	Special Memories
3	Sonstige ICs	Miscellaneous ICs
4	Gehäusebauformen Bereich Halbleiter – Anschriften Literaturhinweise	Package Outlines Semiconductor Group – Addresses Information on Literature

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